Description
The 8V19N490-24 is a fully integrated FemtoClock® NG jitter attenuator and clock synthesizer designed as a high-performance clock solution for conditioning and frequency/phase management of wireless base station radio equipment boards. The device is optimized to deliver excellent phase noise performance as required in GSM, WCDMA, LTE, and LTE-A radio board implementations. The device supports JESD204B subclass 0 and 1 clocks.

A two-stage PLL architecture supports both jitter attenuation and frequency multiplication. The first stage PLL is the jitter attenuator and uses an external VCXO for best possible phase noise characteristics. The second stage PLL locks on the VCXO-PLL output signal and synthesizes the target frequency.

The device supports the clock generation of high-frequency clocks from the selected VCO and low-frequency synchronization signals (SYSREF). SYSREF signals are internally synchronized to the clock signals. Delay functions exist for achieving alignment and controlled phase delay between system reference and clock signals and to align/delay individual output signals. The four redundant inputs are monitored for activity. Four selectable clock switching modes are provided to handle clock input failure scenarios. Auto-lock, individually programmable output frequency dividers, and phase adjustment capabilities are added for flexibility.

The device is configured through a 3-wire SPI interface and reports lock and signal loss status in internal registers and via a lock detect (LOCK) output. Internal status bit changes can also be reported via the nINT output. The 8V19N490-24 is ideal for driving converter circuits in wireless infrastructure, radar/imaging, and instrumentation/medical applications. The device is a member of the high-performance clock family from IDT.

Typical Applications
- Wireless infrastructure applications: GSM, WCDMA, LTE, LTE-A
- Ideal clock driver for jitter-sensitive ADC and DAC circuits
- Low-phase noise clock generation
- Ethernet line cards
- Radar and imaging
- Instrumentation and medical

Features
- High-performance clock RF-PLL with support for JESD204B
- Optimized for low-phase noise: -150dBc/Hz (800kHz offset; 245.76MHz clock)
- Integrated phase noise of 80fs RMS typical (12kHz–20MHz)
- Dual-PLL architecture
- First PLL stage with external VCXO for clock jitter attenuation
- Second PLL with internal FemtoClock NG PLL: 2457.6MHz
- Six output channels with a total of 19 outputs, organized in:
  - Four JESD204B channels (device clock and SYSREF output) with two, four and six outputs
  - One clock channel with two outputs
  - One VCXO output
- Configurable integer clock frequency dividers
- Supported clock output frequencies include: 2457.6, 1228.8, 614.4, 491.52, 307.2, 153.6, and 122.88MHz
- Low-power LVPECL/LVDS outputs support configurable signal amplitude, DC and AC coupling and LVPECL, LVDS line terminations techniques
- Phase delay circuits:
  - Clock phase delay with 256 steps of 407ps and a range of 0 to 103.760ns
  - Individual SYSREF phase delay with 8 steps of 203ps
  - Additional individual SYSREF fine phase delay with 25ps steps
  - Global SYSREF signal delay with 256 steps of 407ps and a range of 0 to 103.760ns
- Redundant input clock architecture with four inputs, including:
  - Input activity monitoring
  - Manual and automatic, fault-triggered clock selection modes
  - Priority controlled clock selection
  - Digital holdover and hitless switching
  - Differential inputs accept LVDS and LVPECL signals
- SYSREF generation modes include internal and external trigger mode for JESD204B
- Supply voltage: 3.3V
- SPI and control I/O voltage: 1.8V/3.3V (selectable)
- Package: 11 × 11mm 100-CABGA
- Temperature range: -40°C to +85°C
Block Diagram

Figure 1. Block Diagram (f_{VCO} = 2457.6MHz)
Ball Map

Figure 2. Ball Map for 11 × 11 × 1.2mm 100-CABGA Package with 1mm Ball Pitch (Bottom View)

Pin Descriptions

Table 1. Pin Descriptions [a]

<table>
<thead>
<tr>
<th>Ball</th>
<th>Name</th>
<th>Type[b]</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F7</td>
<td>CLK_0</td>
<td>Input (PD)</td>
<td>Device clock 0 inverting and non-inverting differential clock input. Inverting input is biased to V_{DD, V}/2 by default when left floating. Compatible with LVPECL, LVDS and LVCMOS signals.</td>
</tr>
<tr>
<td>G7</td>
<td>nCLK_0</td>
<td>Input PD/PU</td>
<td></td>
</tr>
<tr>
<td>G6</td>
<td>nCLK_1</td>
<td>Input PD/PU</td>
<td>Device clock 1 inverting and non-inverting differential clock input. Inverting input is biased to V_{DD, V}/2 by default when left floating. Compatible with LVPECL, LVDS and LVCMOS signals.</td>
</tr>
</tbody>
</table>
Table 1. Pin Descriptions (Cont.)[^a]

<table>
<thead>
<tr>
<th>Ball</th>
<th>Name</th>
<th>Type[^b]</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F5</td>
<td>CLK_2</td>
<td>Input (PD)</td>
<td>Device clock 2 inverting and non-inverting differential clock input. Inverting input is biased to (V_{DD}/2) by default when left floating. Compatible with LVPECL, LVDS and LVCMOS signals.</td>
</tr>
<tr>
<td>G5</td>
<td>nCLK_2</td>
<td>Input PD/PU</td>
<td></td>
</tr>
<tr>
<td>F4</td>
<td>CLK_3</td>
<td>Input (PD)</td>
<td>Device clock 3 inverting and non-inverting differential clock input. Inverting input is biased to (V_{DD}/2) by default when left floating. Compatible with LVPECL, LVDS and LVCMOS signals.</td>
</tr>
<tr>
<td>G4</td>
<td>nCLK_3</td>
<td>Input PD/PU</td>
<td></td>
</tr>
<tr>
<td>A9, A10</td>
<td>QCLK_A0, nQCLK_A0</td>
<td>Output</td>
<td>Differential clock output A0 (Channel A). Configurable LVPECL/LVDS style and amplitude.</td>
</tr>
<tr>
<td>C9, C10</td>
<td>QCLK_A2, nQCLK_A2</td>
<td>Output</td>
<td>Differential clock output A2 (Channel A). Configurable LVPECL/LVDS style and amplitude.</td>
</tr>
<tr>
<td>G9, G10</td>
<td>QREF_A0, nQREF_A0</td>
<td>Output</td>
<td>Differential SYSREF/clock output REF_A0 (Channel A). LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.</td>
</tr>
<tr>
<td>F9, F10</td>
<td>QREF_A1, nQREF_A1</td>
<td>Output</td>
<td>Differential SYSREF/clock output REF_A1 (Channel A). LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.</td>
</tr>
<tr>
<td>E9, E10</td>
<td>QREF_A2, nQREF_A2</td>
<td>Output</td>
<td>Differential SYSREF/clock output REF_A2 (Channel A). LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.</td>
</tr>
<tr>
<td>A2, A1</td>
<td>QCLK_B0, nQCLK_B0</td>
<td>Output</td>
<td>Differential clock output B0 (Channel B). Configurable LVPECL/LVDS style and amplitude.</td>
</tr>
<tr>
<td>A5, A4</td>
<td>QREF_B0, nQREF_B0</td>
<td>Output</td>
<td>Differential SYSREF/clock output REF_B0 (Channel B). LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.</td>
</tr>
<tr>
<td>B5, B4</td>
<td>QREF_B1, nQREF_B1</td>
<td>Output</td>
<td>Differential SYSREF/clock output REF_B1 (Channel B). LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.</td>
</tr>
<tr>
<td>J2, J1</td>
<td>QCLK_C0, nQCLK_C0</td>
<td>Output</td>
<td>Differential clock output C0 (Channel C). Configurable LVPECL/LVDS style and amplitude.</td>
</tr>
<tr>
<td>K2, K1</td>
<td>QCLK_C1, nQCLK_C1</td>
<td>Output</td>
<td>Differential clock output C1 (Channel C). Configurable LVPECL/LVDS style and amplitude.</td>
</tr>
<tr>
<td>F2, F1</td>
<td>QREF_C0, nQREF_C0</td>
<td>Output</td>
<td>Differential SYSREF/clock output REF_C0 (Channel C). LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.</td>
</tr>
<tr>
<td>G2, G1</td>
<td>QREF_C1, nQREF_C1</td>
<td>Output</td>
<td>Differential SYSREF/clock output REF_C1 (Channel C). LVDS style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.</td>
</tr>
<tr>
<td>D2, D1</td>
<td>QCLK_D, nQCLK_D</td>
<td>Output</td>
<td>Differential clock output D (Channel D). Configurable LVPECL/LVDS style and amplitude.</td>
</tr>
</tbody>
</table>

[^a]: Table continues on the next page.
[^b]: Types: Input (PD) = Inverting and non-inverting differential clock input. Input PD/PU = Inverting input is biased to \(V_{DD}/2\) by default when left floating. Compatibility with LVPECL, LVDS and LVCMOS signals.
<table>
<thead>
<tr>
<th>Ball</th>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>K9, K10</td>
<td>QCLK_E0, nQCLK_E0</td>
<td>Output</td>
<td>Differential clock output E0. Configurable LVPECL/LVDS style and amplitude.</td>
</tr>
<tr>
<td>J9, J10</td>
<td>QCLK_E1, nQCLK_E1</td>
<td>Output</td>
<td>Differential clock output E1. Configurable LVPECL/LVDS style and amplitude.</td>
</tr>
<tr>
<td>C7, D7</td>
<td>QOSC, nQOSC</td>
<td>Output</td>
<td>Differential VCXO-PLL clock outputs. Configurable LVPECL/LVDS style and amplitude.</td>
</tr>
<tr>
<td>C8</td>
<td>nINT</td>
<td>Output</td>
<td>Status output pin for signaling internal changed conditions. Selectable 1.8/3.3V LVCMOS interface levels.</td>
</tr>
<tr>
<td>G8</td>
<td>LOCK</td>
<td>Output</td>
<td>PLL lock detect status output for both PLLs. Selectable 1.8/3.3V LVCMOS interface levels.</td>
</tr>
<tr>
<td>F3</td>
<td>EXT_SYS</td>
<td>Input (PD)</td>
<td>External SYSREF pulse trigger input. Selectable 1.8V/3.3V LVCMOS interface levels.</td>
</tr>
<tr>
<td>E8</td>
<td>SDAT</td>
<td>Input/Output (PU)</td>
<td>Serial Control Port SPI Mode Data Input and Output. Selectable 1.8V/3.3V LVCMOS interface levels. 3.3V tolerant when set to 1.8V and set to input.</td>
</tr>
<tr>
<td>E5</td>
<td>SCLK</td>
<td>Input (PD)</td>
<td>Serial Control Port SPI Mode Clock Input. Selectable 1.8V/3.3V LVCMOS interface levels. 3.3V tolerant when set to 1.8V.</td>
</tr>
<tr>
<td>E4</td>
<td>nCS</td>
<td>Input (PU)</td>
<td>Serial Control Port SPI Chip Select Input. Selectable 1.8V/3.3V LVCMOS interface levels. 3.3V tolerant when set to 1.8V.</td>
</tr>
<tr>
<td>C5</td>
<td>SELSV</td>
<td>Input (PD)</td>
<td>SPI interface voltage select. 3.3V LVCMOS interface levels. For control input and SPI interface voltage selection (see Table 25).</td>
</tr>
<tr>
<td>J5</td>
<td>CR0</td>
<td>Analog</td>
<td>Internal VCO regulator bypass capacitor. Use a 4.7 µF capacitor between the CR0 and the VDD_LCF (K4) terminals.</td>
</tr>
<tr>
<td>A6</td>
<td>LFV</td>
<td>Output</td>
<td>VCXO-PLL charge pump output. Connect to the loop filter for the external VCXO.</td>
</tr>
<tr>
<td>A7</td>
<td>OSC</td>
<td>Input (PD)</td>
<td>VCXO non-inverting and inverting differential clock input. Inverting input is biased to ( V_{DD, V} / 2 ) by default when left floating. Compatible with LVPECL, LVDS and LVCMOS signals.</td>
</tr>
<tr>
<td>B7</td>
<td>nOSC</td>
<td>Input PD/PU</td>
<td>Loop filter/charge pump output for the FemtoClock NG NG PLL. Connect to the external loop filter.</td>
</tr>
<tr>
<td>K6</td>
<td>LFF</td>
<td>Output</td>
<td>Ground return path pin for the VCO loop filter.</td>
</tr>
<tr>
<td>F8</td>
<td>RES_CAL</td>
<td>Analog</td>
<td>Connect a 2.8 kΩ (1%) resistor to GND for output current calibration.</td>
</tr>
<tr>
<td>A8, C1, C2, C3, C6, D6, D8, E1, E2, E6, E7, H3, H4, H5, H6, H8, H9, H10, J3, J6, J7, J8, K3</td>
<td>GND</td>
<td>Power</td>
<td>Ground supply voltage (GND) and ground return path. Connect to board GND (0V).</td>
</tr>
<tr>
<td>D10</td>
<td>VDD_QCLKA</td>
<td>Power</td>
<td>Positive supply voltage (3.3V) for the QCLK_A[2:0] outputs.</td>
</tr>
</tbody>
</table>
## Principles of Operation

### Overview

The 8V19N490-24 generates low-phase noise, synchronized clock and SYSREF output signals locked to an input reference frequency. The device contains two PLLs with configurable frequency dividers. The first PLL (VCXO-PLL, suffix V) uses an external VCXO as the oscillator and provides jitter attenuation. The external loop filter is used to set the VCXO-PLL bandwidth frequency in conjunction with internal parameters. The second, low-phase noise PLL (FemtoClock NG, suffix F) multiplies the VCXO-PLL frequency to 2457.6MHz. The FemtoClock NG PLL is completely internal and provides a central timing reference point for all output signals. From this point, fully synchronous dividers generate the output frequencies and the internal timing references for JESD204B support.

The device supports the generation of SYSREF pulses synchronous to the clock signals. There are five channels consisting of clock and/or SYSREF outputs. The clock outputs are configurable with support for LVPECL or LVDS formats and a variable output amplitude. Clock and SYSREF offer adjustable phase delay functionality. Individual outputs and channels and unused circuit blocks support powered-down states for operating at lower power consumption. The register map, accessible through SPI interface with read-back capability controls the main device settings and delivers device status information. For redundancy purpose, there are two selectable reference frequency inputs and a configurable switch logic with priority-controlled auto-selection and holdover support.

### Table 1. Pin Descriptions (Cont.)

<table>
<thead>
<tr>
<th>Ball</th>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9</td>
<td>VDD_QREFA</td>
<td>Power</td>
<td>Positive supply voltage (3.3V) for the QREF_A[2:0] outputs.</td>
</tr>
<tr>
<td>A3</td>
<td>VDD_QCLKB</td>
<td>Power</td>
<td>Positive supply voltage (3.3V) for the QCLK_B[2:0] outputs.</td>
</tr>
<tr>
<td>B3</td>
<td>VDD_QREFB</td>
<td>Power</td>
<td>Positive supply voltage (3.3V) for the QREF_B[2:0] outputs.</td>
</tr>
<tr>
<td>H1</td>
<td>VDD_QCLKC</td>
<td>Power</td>
<td>Positive supply voltage (3.3V) for the QCLK_C[1:0] outputs.</td>
</tr>
<tr>
<td>H2</td>
<td>VDD_QREFC</td>
<td>Power</td>
<td>Positive supply voltage (3.3V) for the QREF_C[1:0] outputs.</td>
</tr>
<tr>
<td>D3</td>
<td>VDD_QCLKD</td>
<td>Power</td>
<td>Positive supply voltage (3.3V) for the QCLK_D outputs.</td>
</tr>
<tr>
<td>C4</td>
<td>VDD_QREFD</td>
<td>Power</td>
<td>Positive supply voltage (3.3V) for the QREF_D outputs.</td>
</tr>
<tr>
<td>K8</td>
<td>VDD_QCLKE</td>
<td>Power</td>
<td>Positive supply voltage (3.3V) for the QCLK_E[1:0] outputs.</td>
</tr>
<tr>
<td>E3</td>
<td>VDD_SPI</td>
<td>Power</td>
<td>Positive supply voltage (3.3V) for the SPI interface.</td>
</tr>
<tr>
<td>G3</td>
<td>VDD_INP</td>
<td>Power</td>
<td>Positive supply voltage (3.3V) for the differential inputs (CLK0 to CLK3).</td>
</tr>
<tr>
<td>J4</td>
<td>VDD_LCV</td>
<td>Power</td>
<td>Positive supply voltage (3.3V).</td>
</tr>
<tr>
<td>K4</td>
<td>VDD_LCF</td>
<td>Power</td>
<td>Positive supply voltage (3.3V).</td>
</tr>
<tr>
<td>K7</td>
<td>VDD_CPF</td>
<td>Power</td>
<td>Positive supply voltage (3.3V) for internal FemtoClock NG circuits.</td>
</tr>
<tr>
<td>B8</td>
<td>VDD_OSC</td>
<td>Power</td>
<td>Positive supply voltage (3.3V) for OSC, nOSC input and QOSC, nQOSC output.</td>
</tr>
<tr>
<td>B6</td>
<td>VDD_CP</td>
<td>Power</td>
<td>Positive supply voltage (3.3V) for internal VCXO_PLL circuits.</td>
</tr>
<tr>
<td>H7</td>
<td>VDD_SYNC</td>
<td>Power</td>
<td>Positive supply voltage (3.3V).</td>
</tr>
</tbody>
</table>

[a] For essential information on power supply filtering, see Power Supply Design and Recommend Application Schematics.

[b] Pull-up (PU) and pull-down (PD) resistors are indicated in parentheses. For values, see Table 44.
Phase-Locked Loop Operation

Frequency Generation

Table 2 displays the available frequency dividers for clock generation. The dividers must be set by the user to match input, VCXO and VCO frequency, and to achieve frequency and phase lock on both PLLs. The frequency of the external VCXO is selected by the user; the internal VCO frequency is set to 2457.6MHz. Example divider configurations for typical wireless infrastructure applications are shown in Table 3.

Table 2. PLL Operation and Divider Values

<table>
<thead>
<tr>
<th>Divider</th>
<th>Range</th>
<th>Operation for $f_\text{VCO} = 2457.6\text{MHz}$</th>
<th>Jitter Attenuation, Dual-PLL with Deterministic Input-to-Output Delay (BYPV = 0, BYPF = 1)</th>
<th>Jitter Attenuation, Dual-PLL (BYPV = 0, BYPF = 0)</th>
<th>Frequency Synthesis (VCXO-PLL Bypassed, BYPV = 1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCXO-PLL Pre-Divider $P_V$</td>
<td>$+1...+4095$ (12 bit)</td>
<td>Input clock frequency:</td>
<td>$f_{\text{CLK}} = P_V \times \frac{f_{\text{VCXO}}}{P_F} \times \frac{M_F}{M_{V0} \times M_{V1}}$</td>
<td>$f_{\text{CLK}} = f_{\text{VCXO}} \times \frac{P_V}{M_{V0}}$</td>
<td>$f_{\text{CLK}} = f_{\text{VCO}} \times \frac{P_V \times P_F}{M_F}$</td>
</tr>
<tr>
<td>VCXO-PLL Feedback Divider $M_{V0}$</td>
<td>$+1...+4095$ (12 bit)</td>
<td>VCXO frequency:</td>
<td>$f_{\text{VCXO}} = f_{\text{VCO}} \times \frac{P_F}{M_F}$</td>
<td>$f_{\text{VCXO}}$</td>
<td>$M_{V0}$ and $M_{V1}$ settings are not applicable to PLL operation.</td>
</tr>
<tr>
<td>PLL Feedback Divider $M_{V1}$</td>
<td>$+4...+511$ (9 bit)</td>
<td>$P_F$: Set $P_F$ to 0.5 in above equation if the frequency doubler is engaged by setting $FDF = 1$.</td>
<td>$f_{\text{CLK}} = f_{\text{VCXO}} \times \frac{P_V}{M_{V0}}$</td>
<td>$f_{\text{CLK}} = f_{\text{VCO}} \times \frac{P_V \times P_F}{M_F}$</td>
<td>$M_{V0}$ and $M_{V1}$ settings are not applicable to the PLL operation.</td>
</tr>
<tr>
<td>FemtoClock NG Pre-Divider $P_F$</td>
<td>$+1...+63$ (6 bit)</td>
<td>Output frequency:</td>
<td>$f_{\text{OUT}} = \frac{f_{\text{VCO}}}{N_X}$</td>
<td>$f_{\text{CLK}} = f_{\text{VCXO}} \times \frac{P_V}{M_{V0}}$</td>
<td>$f_{\text{CLK}} = f_{\text{VCO}} \times \frac{P_V \times P_F}{M_F}$</td>
</tr>
<tr>
<td>FemtoClock NG Feedback Dividers $M_F$</td>
<td>$+8...+511$ (9 bit)</td>
<td>$P_F$: Set $P_F$ to 0.5 in above equation if the frequency doubler is engaged by setting $FDF = 1$.</td>
<td>$f_{\text{CLK}} = f_{\text{VCXO}} \times \frac{P_V}{M_{V0}}$</td>
<td>$f_{\text{CLK}} = f_{\text{VCO}} \times \frac{P_V \times P_F}{M_F}$</td>
<td>$M_{V0}$ and $M_{V1}$ settings are not applicable to the PLL operation.</td>
</tr>
<tr>
<td>Output Divider $N_X$ ($x = A, B, C, D, E$)</td>
<td>$+1...+160$</td>
<td>Output frequency:</td>
<td>$f_{\text{OUT}} = \frac{f_{\text{VCO}}}{N_X}$</td>
<td>$f_{\text{CLK}} = f_{\text{VCXO}} \times \frac{P_V}{M_{V0}}$</td>
<td>$f_{\text{CLK}} = f_{\text{VCO}} \times \frac{P_V \times P_F}{M_F}$</td>
</tr>
<tr>
<td>SYSREF Divider $N_S$ ($N_S = 16...+5120$; ${2, 4} \times {2, 4, 8, 16} \times {2, 3, 4, 5}$)</td>
<td>$+16...+5120$</td>
<td>SYSREF frequency/rate:</td>
<td>$f_{\text{SYSREF}} = \frac{f_{\text{VCO}}}{N_S}$</td>
<td>$f_{\text{CLK}} = f_{\text{VCXO}} \times \frac{P_V}{M_{V0}}$</td>
<td>$f_{\text{CLK}} = f_{\text{VCO}} \times \frac{P_V \times P_F}{M_F}$</td>
</tr>
</tbody>
</table>

[a] For input monitoring, configure $M_{V1}$ as described in Monitoring and LOS of Input Signal.

[b] For SYSREF operation, configure SYNC[6:0] as described in Synchronizing SYSREF and Clock Output Dividers.
VCXO-PLL

The prescaler $P_V$ and the VCXO-PLLs feedback divider $M_{V0}$ and $M_{V1}$ require configuration to match the input frequency to the VCXO-frequency. The BYPF setting allows to route the VCXO-PLLs feedback path through the $M_{V0}$ divider. Alternatively, the feedback path is routed through the second PLL and both the $M_{V0}$ and $M_{V1}$ feedback divider. $M_{V0}$ has a divider value range of 12 bit; $M_{V1}$ has 9 bit. The feedback path through the second PLL, in combination with the divider setting $P_F = \div 1$, is the preferred setting for achieving deterministic delay from the clock input to the outputs.

Multiple divider settings are available to enable support for input frequencies of e.g., 245.76MHz, 122.88MHz, 61.44MHz and 30.72MHz and the VCXO-frequencies of 122.88MHz, 61.44MHz, 38.4MHz, 30.72MHz, and 245.76MHz. In addition, the range of available input and feedback dividers allows to adjust the phase detector frequency independent of the input and VCXO frequencies. In general, the phase detector may be set into the range from 120kHz to the input reference frequency. The VCXO-PLL charge pump current is controllable via registers and can be set in 50µA steps from 50µA to 1.6mA. The VCXO-PLL may be bypassed: the FemtoClock NG PLL locks to the pre-divider input frequency.

**Table 3. Example Configurations for $f_{VCXO} = 122.88\text{MHz}^{[a]}$**

<table>
<thead>
<tr>
<th>Input Frequency (MHz)</th>
<th>VCXO-PLL Divider Settings</th>
<th>$f_{PFD}$ (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$P_V$ $M_{V0}$</td>
<td></td>
</tr>
<tr>
<td>245.76</td>
<td>32 16</td>
<td>7.68</td>
</tr>
<tr>
<td></td>
<td>256 128</td>
<td>0.96</td>
</tr>
<tr>
<td></td>
<td>1024 1024</td>
<td>0.12</td>
</tr>
<tr>
<td>122.88</td>
<td>16 16</td>
<td>7.68</td>
</tr>
<tr>
<td></td>
<td>128 128</td>
<td>0.96</td>
</tr>
<tr>
<td></td>
<td>1024 1024</td>
<td>0.12</td>
</tr>
</tbody>
</table>

[a] BYPF = 0.

**Table 4. Example Configurations for $f_{VCXO} = 38.4\text{MHz}^{[a]}$**

<table>
<thead>
<tr>
<th>Input Frequency (MHz)</th>
<th>VCXO-PLL Divider Settings</th>
<th>$f_{PFD}$ (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$P_V$ $M_{V0}$</td>
<td></td>
</tr>
<tr>
<td>245.76</td>
<td>32 5</td>
<td>7.68</td>
</tr>
<tr>
<td></td>
<td>128 20</td>
<td>1.92</td>
</tr>
<tr>
<td></td>
<td>512 80</td>
<td>0.48</td>
</tr>
<tr>
<td></td>
<td>2048 320</td>
<td>0.12</td>
</tr>
<tr>
<td>122.88</td>
<td>16 5</td>
<td>7.68</td>
</tr>
<tr>
<td></td>
<td>64 20</td>
<td>1.92</td>
</tr>
<tr>
<td></td>
<td>256 80</td>
<td>0.48</td>
</tr>
<tr>
<td></td>
<td>1048 320</td>
<td>0.12</td>
</tr>
</tbody>
</table>

[a] BYPF = 0.
This PLL locks to the output signal of the VCXO-PLL (BYPV = 0). It requires configuration of the frequency doubler FDF or the pre-divider P_F and the feedback divider M_F to match the VCXO-PLL frequency to the VCO frequency of 2457.6MHz. This PLL is internally configured to high-bandwidth. Best phase noise is typically achieved by engaging the internal frequency doubler (FDF = 1). If engaged, the signal from the first PLL stage is doubled in frequency, increasing the phase detector frequency of the FemtoClock NG PLL. Enabling the frequency doubler disables the frequency pre-divider P_F. If the frequency doubler is not used (FDF = 0), the P_F pre-divider has to be configured. Typically P_F is set to +1 to keep the phase detector frequency as high as possible. Set P_F to other divider values to achieve specific frequency ratios (1 to 19.2, 1 to 76.8, etc.) between first and second PLL stage.

**Table 5. VCXO-PLL Bypass Settings**

<table>
<thead>
<tr>
<th>BYPV</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>VCXO-PLL operation.</td>
</tr>
<tr>
<td>1</td>
<td>VCXO-PLL bypassed and disabled. The reference clock for the FemtoClock NG PLL is the input clock divided by the pre-divider P_V. The input clock selection must be set to manual by the user. Clock switching and holdover are not defined. The device will not attenuate input jitter. No external VCXO component and loop filter required.</td>
</tr>
</tbody>
</table>

**Table 6. PLL Feedback Path Settings**

<table>
<thead>
<tr>
<th>BYPF</th>
<th>Operation[a]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>VCXO-PLL feedback path through the M_V0 divider. FemtoClock NG feedback path uses the M_F divider.</td>
</tr>
<tr>
<td>1</td>
<td>VCXO-PLL feedback path through the M_{V1} × M_V0 dividers. FemtoClock NG feedback path uses the M_F divider. Preferred setting for achieving deterministic delay from input to the outputs.</td>
</tr>
</tbody>
</table>

[a] Regardless of the selected internal feedback path, the M_{V1} divider should be set to match its internal output frequency to the input reference frequency: the M_{V1} output signal is the internal reference for input loss-of-signal detect.

**FemtoClock NG PLL**

This PLL locks to the output signal of the VCXO-PLL (BYPV = 0). It requires configuration of the frequency doubler FDF or the pre-divider P_F and the feedback divider M_F to match the VCXO-PLL frequency to the VCO frequency of 2457.6MHz. This PLL is internally configured to high-bandwidth. Best phase noise is typically achieved by engaging the internal frequency doubler (FDF = 1). If engaged, the signal from the first PLL stage is doubled in frequency, increasing the phase detector frequency of the FemtoClock NG PLL. Enabling the frequency doubler disables the frequency pre-divider P_F. If the frequency doubler is not used (FDF = 0), the P_F pre-divider has to be configured. Typically P_F is set to +1 to keep the phase detector frequency as high as possible. Set P_F to other divider values to achieve specific frequency ratios (1 to 19.2, 1 to 76.8, etc.) between first and second PLL stage.

**Table 7. Frequency Doubler**

<table>
<thead>
<tr>
<th>FDF</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Frequency doubler off. P_F divides clock signal from VCXO-PLL or input (in bypass).</td>
</tr>
<tr>
<td>1</td>
<td>Frequency doubler on. Signal from VCXO-PLL or input (in bypass) is doubled in frequency. P_F divider has no effect.</td>
</tr>
</tbody>
</table>
Channel Frequency Divider

The device supports five independent channels A to E. Each channel has a frequency divider N \( x \) (\( x = A \) to \( E \)) that divides the VCO frequency to the output frequency. Each divider be individually set to a value in the range of +1 to +160. For typical divider values (see Table 9). For the complete set of supported divider values (see Table 28).

Table 8. Example PLL Configurations

<table>
<thead>
<tr>
<th>VCXO-Frequency (MHz)</th>
<th>FemtoClock NG Divider Settings</th>
<th>Output Frequency (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>122.88</td>
<td>FDF x2 PF M_F N_x[a]</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 2 4 5 8 10</td>
<td>2457.6 1228.8 614.4 491.52 307.6 245.76</td>
</tr>
<tr>
<td></td>
<td>16 20</td>
<td>153.6 122.88</td>
</tr>
<tr>
<td>122.88</td>
<td>FDFPF M_F N_x[a]</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 2 4 5 8 10</td>
<td>2457.6 1228.8 614.4 491.52 307.6 245.76</td>
</tr>
<tr>
<td></td>
<td>16 20</td>
<td>153.6 122.88</td>
</tr>
</tbody>
</table>

[a] \( x = A \) to \( E \).

Table 9. Integer Frequency Divider Settings

<table>
<thead>
<tr>
<th>Channel Divider N ( x )^[a]</th>
<th>Output Clock Frequency (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>f(_{VCO} ) = 2457.6 (MHz)</td>
<td></td>
</tr>
<tr>
<td>+1</td>
<td>2457.6</td>
</tr>
<tr>
<td>+2</td>
<td>1228.8</td>
</tr>
<tr>
<td>+4</td>
<td>614.4</td>
</tr>
<tr>
<td>+5</td>
<td>491.52</td>
</tr>
<tr>
<td>+8</td>
<td>307.2</td>
</tr>
<tr>
<td>+10</td>
<td>245.76</td>
</tr>
<tr>
<td>+16</td>
<td>153.6</td>
</tr>
<tr>
<td>+20</td>
<td>122.88</td>
</tr>
<tr>
<td>+30</td>
<td>81.92</td>
</tr>
<tr>
<td>+32</td>
<td>76.8</td>
</tr>
<tr>
<td>+40</td>
<td>61.44</td>
</tr>
<tr>
<td>+50</td>
<td>49.152</td>
</tr>
<tr>
<td>+60</td>
<td>40.96</td>
</tr>
<tr>
<td>+64</td>
<td>38.4</td>
</tr>
</tbody>
</table>
Redundant Inputs

The four inputs are compatible with LVDS and LVPECL signal formats, and also support single-ended LVCMOS signals. For applicable input interface circuits, see Application Information.

Monitoring and LOS of Input Signal

The four inputs of the device are individually monitored for activity. Inactivity is defined by a static input signal.

The clock input monitors compare the device input frequency ($f_{CLK}$) to the frequency of the VCO divided by $M_{V1}$ (regardless of the internal feedback path using or not using $M_{V1}$). A clock input is declared invalid with the corresponding LOS (Loss-of-input signal) indicator bit set after three consecutive missing clock edges. For correct operation of the LOS detect circuit, $M_{V1}$ must be powered on by setting $PD_{_MV1} = 0$.

The $M_{V1}$ divider must be set so that the LOS detect reference frequency matches the input frequency. For instance, if the input frequency is 245.76MHz, $M_{V1}$ should be set to $÷10$: The VCO frequency of 2457.6MHz divided by 10 equals the input frequency of 245.76MHz. For an input frequency of 122.88MHz, set $M_{V1}$ to $÷20$. Failure to set $M_{V1}$ to match the input frequency will result in added latency to the LOS circuit (if, $f_{VCO} ÷ M_{V1} < f_{CLK}$) or false LOS indication (if, $f_{VCO} ÷ M_{V1} > f_{CLK}$). The minimum frequency that the circuit can monitor is: $f_{VCO} / M_{V1(\text{MAX})} = 4.81\text{MHz}$. In applications with a lower input frequency than 4.81MHz, disable the monitor to trigger the status flags by setting $BLOCK_{_LOR} = 1$.

If differential input signals are applied, the input will also detect an LOS condition in case of a zero differential input voltage.

Input Re-Validation

A clock input is declared valid and the corresponding LOS status bit is reset after the clock input signal returns for user-configurable number of consecutive input periods. This re-validation of the selected input clock is controlled by the CNTV setting (verification pulse counter).

<table>
<thead>
<tr>
<th>Channel Divider N[a]</th>
<th>Output Clock Frequency (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$÷80$</td>
<td>30.72</td>
</tr>
<tr>
<td>$÷100$</td>
<td>24.576</td>
</tr>
<tr>
<td>$÷120$</td>
<td>20.48</td>
</tr>
<tr>
<td>$÷128$</td>
<td>19.2</td>
</tr>
<tr>
<td>$÷160$</td>
<td>15.36</td>
</tr>
</tbody>
</table>

[a] $x$ = A to E.
Clock Selection

The device supports four input selection modes: manual, short-term holdover, and two automatic switch modes. The modes are described in the following table.

### Table 10. Clock Selection Settings

<table>
<thead>
<tr>
<th>Mode</th>
<th>Description</th>
<th>Application</th>
</tr>
</thead>
<tbody>
<tr>
<td>Manual nM/A[1:0] = 00</td>
<td>Input selection follows user configuration of SEL[1:0]. Selection is never changed by the internal state machine. A failing reference clock will cause an LOS event and the PLL will unlock if the failing clock is selected. Re-validation of the selected input clock will result in the PLL to re-lock on that input clock.</td>
<td>Startup and external selection control</td>
</tr>
<tr>
<td>Automatic nM/A[1:0] = 01</td>
<td>Input selection follows LOS status by user preset input switch priorities. A failing input clock will cause an LOS event for that clock input. If the selected clock has an LOS event, the device will immediately initiate a clock fail-over switch. The switch target is determined by pre-set input priorities. No valid clock scenario: If no valid input clocks exist, the device will not attempt to switch and will not enter the holdover state. The PLL is not locked. Re-validation of any input clock that is not the selected clock will result in the PLL to attempt to lock on that input clock. For additional information see, Revertive Switching.</td>
<td>Multiple inputs with qualified clock signals</td>
</tr>
<tr>
<td>Shot-term Holdover nM/A[1:0] = 10</td>
<td>Input selection follows user-configuration of SEL[1:0]. Selection is never changed by the internal state machine. A failing reference clock will cause an LOS event. If the selected reference fails, the device will enter holdover immediately. Re-validation of the selected input clock is controlled by the CNTV setting. A successful re-validation will result in the PLL to re-lock on that input clock. For additional information see, Short-Term Holdover.</td>
<td>Single reference</td>
</tr>
<tr>
<td>Automatic with Holdover nM/A[1:0] = 11</td>
<td>Input selection follows LOS status by user preset input priorities. Each failing input clock will cause an LOS event for that clock input. If the selected clock detects an LOS event, the device will go into holdover and the hold-off down-counter (CNTH) starts. The device initiates a clock fail-over switch after expiration of the hold-off counter. The switch target is determined by the preset input priorities. No valid clock scenario: If no valid input clocks exist, the device will not attempt to switch and will remain in the holdover state. Re-validation of any input clock will result in the PLL to attempt to lock on that input clock. For additional information see, Automatic with Holdover (nM/A[1:0] = 11), and Revertive Switching.</td>
<td>Multiple inputs</td>
</tr>
</tbody>
</table>
**Holdover**
In holdover state, the output frequency and phase is derived from an internal, digital value based on previous frequency and phase information. Holdover characteristics are defined in Table 51.

**Input Priorities**
Configurable settings encompass four selectable priorities with the range 0 (lowest priority) to 3 (highest priority). The user can change the input priorities at any time. In the automatic switch modes, input priority changes may cause immediate input selection changes.

**Hold-off Counter**
A configurable down-counter applicable to the “Automatic with holdover” selection mode. The purpose of this counter is a deferred, user-configurable, input switch after an LOS event. The hold-off counter is triggered by a transition of ST_REF upon detection of an LOS event. The counter expires when a zero-transition occurs; this triggers a new reference clock selection. The counter is clocked by the frequency-divided VCXO-PLL signal. The CNTR setting determines the hold-off counter frequency divider and the CNTH setting the start value of the hold-off counter. For instance, set CNTR to a value of $+131072$ to achieve $937.5\text{Hz}$ (or a period of $1.066\text{ms}$ at $f_{\text{VCXO}} = 122.88\text{MHz}$): the 8-bit CNTH counter is clocked by 937.5Hz and the user configurable hold-off period range is 0ms ($\text{CNTH} = 0x00$) to 272ms ($\text{CNTH} = 0xFF$). After the counter expires, it reloads automatically from the CNTH SPI register. After the LOS status bit ($\text{LS_CLK}_n$) for the corresponding input $\text{CLK}_n$ has been cleared by the user, the input is enabled for generating a new LOS event.

The CNTR counter is only clocked if the device is configured in the clock selection mode, *Automatic with holdover*, and the selected reference clock experiences an LOS event. Otherwise, the counter is automatically disabled (not clocked).

**Revertive Switching**
Revertive switching is applicable only to the two automatic switch modes shown in Table 10. When revertive switching is enabled, re-validation of any non-selected input clock(s) will cause a new input selection according to the user-preset input priorities (revertive switch). An input switch is only done if the re-validated input has a higher priority than the currently selected reference clock.

When revertive switching is disabled, re-validation of a non-selected input clock has no impact on the clock selection. Default setting is revertive switching disabled.

**Short-Term Holdover**
If an LOS event is detected on the reference clock designated by the SEL[1:0] bits:
1. Holdover begins immediately.
2. ST_REF, LS_REF go low immediately.
3. No transitions will occur of the active REF clock; ST_SEL[1:0] does not change.
4. The hold-off countdown is not active.

When the designated reference clock resumes and has met the programmed validation count of consecutive rising edges:
1. Holdover turns off.
2. ST_SEL[1:0] does not change.
3. ST_REF returns to 1.

LS_REF can be cleared by an SPI write of 1 to that register.
Automatic with Holdover (nM/A[1:0] = 11)

If an LOS event is detected on the active reference clock:
1. Holdover begins immediately.
2. Corresponding ST_REF and LS_REF go low immediately.
3. Hold-off countdown begins immediately.

During this time, all clocks continue to be monitored and their respective ST_CLK, LS_CLK flags are active. LOS events will be indicated on ST_CLK, LS_CLK when they occur.

If the active reference clock resumes and is validated during the hold-off countdown:
1. Its ST_CLK status flag will return high and the LS_CLK is available to be cleared by an SPI write of 1 to that register bit.
2. No transitions will occur of the active REF clock; ST_SEL[1:0] does not change. LS_REF can be cleared by an SPI write of 1 to that register.
3. Revertive bit has no effect during this time (whether 0 or 1).

When the hold-off countdown reaches zero.

If the active reference has resumed and has been validated during the countdown, it will maintain being the active reference clock:
1. ST_SEL1:0 does not change.
2. ST_REF returns to 1.
3. LS_REF can be cleared by an SPI write of 1 to that register.
4. Holdover turns off and the VCXO-PLL attempts to lock to the active reference clock

If the active reference has not resumed, but another (sorted by next priority) clock input CLK_n is validated, then:
1. ST_SEL1:0 changes to the new active reference.
2. ST_REF returns to 1.
3. LS_REF can be cleared by an SPI write of 1 to that register.
4. Holdover turns off.

If there is no validated CLK:
1. ST_SEL1:0 does not change.
2. ST_REF remains low.
3. LS_REF cannot be cleared by an SPI write of 1 to that register.
4. Holdover remains active.

Revertive capability returns if REVS = 1.
VCXO-PLL Lock Detect (LOLV)

The VCXO-PLL lock detect circuit uses the signal phase difference at the phase detector as loss-of-lock criteria. Loss-of-lock is reported if the actual phase difference is larger than a configurable phase window set by the \( \Phi_{MV0} \) and \( \Phi_{PV} \) configuration bits. Configuration of the width window allows for a application-specific loss-of-lock reporting. A loss-of-lock state is reported through the nST_LOLV and nLS_LOLV status bit (see Table 22).

**Loss-of-Lock Window Description**

The selected clock input signal is the reference signal (CLK) for lock detection. The rising edge of CLK defines the reference point \( t_0 \). \( \Phi_{PV} \) configures the start of the lock window \( t_B \) (which occurs before \( t_0 \)) and \( \Phi_{MV0} \) configures the end of the window \( t_E \) (which occurs after \( t_0 \)). The width of the lock window is defined by \( t_E - t_B \). The VCXO-PLL declares lock when the rising edge of the feedback signal (FB) is within this window, otherwise the PLL reports loss-of-lock.

**Figure 3. Lock Detect Window**

![Figure 3. Lock Detect Window](image)

**Table 11. \( t_B \) and \( t_E \) Calculation**

<table>
<thead>
<tr>
<th>Operation</th>
<th>Jitter Attenuation, Dual-PLL with deterministic Input-to-Output Delay (BYPV = 0, BYPF = 1)</th>
<th>Jitter Attenuation, Dual-PLL (BYPV = 0, BYPF = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_B )</td>
<td>[ t_B = \frac{2^{\Phi_{PV}} - 1}{f_{CLK}} ]</td>
<td></td>
</tr>
<tr>
<td>( t_E )</td>
<td>[ t_E = \frac{(2^{\Phi_{MV0}} - 1) \times M_{V1}}{f_{VCO}} ]</td>
<td>[ t_E = \frac{2^{\Phi_{MV0}} - 1}{f_{VCXO}} ]</td>
</tr>
</tbody>
</table>

**Figure 3** shows that \( \Phi_{PV} \) configures the begin and \( \Phi_{MV0} \) the end of the window in integer multiples of PLL input and feedback periods. Both \( \Phi_{PV} \) and \( \Phi_{MV0} \) use three configuration bits with valid settings from 010 to 111 (2 to 7, decimal). This range allows configuring both \( t_B \) and \( t_E \) from 3 to 127 periods of the input signal (\( T_{IN} \)) and the feedback signal (\( T_{FB} \)), respectively, is implied.
Loss-of-Lock Window Configuration Example

With given \( P_V \), \( M_{V0} \), and \( M_{V1} \) divider values, select the corresponding \( \Phi_{PV} \) and \( \Phi_{MV0} \) settings from Table 12 and apply the \( \Phi_{PV} \) and \( \Phi_{MV0} \) values to the \( \Phi_{PV}[1:0] \) and \( \Phi_{MV0}[1:0] \) registers. Table 12 shows the lock window calculation formulas. For instance, if an input frequency of 245.76MHz and a \( P_V \) divider of 128 is desired, set \( \Phi_{PV}[1:0] \) to a binary value of 100 (decimal 4). This results in \( t_B = 61.035ns \) (15 periods of 4.069ns). With a VCXO-PLL (BYPF = 0) and a VCXO frequency of 122.88MHz and \( M_{V0} = 64 \), select 011 (decimal 3) resulting in \( t_E = 56.96ns \) (7 periods of 8.138ns) and an overall lock detect window of \( t_E - t_B = 56.96ns + 61.035ns = 118.001ns \). The user may select a smaller lock detect window. For instance, a \( P_V \) divider of 128 allows to set \( \Phi_{PV}[1:0] \) to 010, 011 or 100 (decimal 2 to 4). Correspondingly, a \( M_{V0} \) divider of 64 allows \( \Phi_{MV0}[1:0] \) settings from 010 to 011 (decimal 2 to 3). With smaller settings, the lock detect window size is reduced exponentially.

\( \Phi_{PV}[1:0] = 000 \) will set \( t_B \) to \( 0.5 \times T_{REF} \), and \( \Phi_{PV}[1:0] = 001 \) will set \( t_B \) to \( 1.5 \times T_{REF} \).
\( \Phi_{MV0}[1:0] = 000 \) will set \( t_E \) to \( 0.5 \times T_{REF} \), and \( \Phi_{MV0}[1:0] = 001 \) will set \( t_E \) to \( 1.5 \times T_{REF} \).

<table>
<thead>
<tr>
<th>( P_V ) Divider Value</th>
<th>( \Phi_{PV}[1:0] ) Setting</th>
<th>( M_{V0} ) Divider Value</th>
<th>( \Phi_{MV0}[1:0] ) Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>1–31</td>
<td>N/A</td>
<td>1–31</td>
<td>N/A</td>
</tr>
<tr>
<td>32–63</td>
<td>010</td>
<td>32–63</td>
<td>010</td>
</tr>
<tr>
<td>64–127</td>
<td>( \leq 011 )</td>
<td>64–127</td>
<td>( \leq 011 )</td>
</tr>
<tr>
<td>128–255</td>
<td>( \leq 100 )</td>
<td>128–255</td>
<td>( \leq 100 )</td>
</tr>
<tr>
<td>256–511</td>
<td>( \leq 101 )</td>
<td>256–511</td>
<td>( \leq 101 )</td>
</tr>
<tr>
<td>512–1023</td>
<td>( \leq 110 )</td>
<td>512–1023</td>
<td>( \leq 110 )</td>
</tr>
<tr>
<td>1024 and higher</td>
<td>( \leq 111 )</td>
<td>1024 and higher</td>
<td>( \leq 111 )</td>
</tr>
</tbody>
</table>

FemtoClock NG Loss-of-Lock (LOLF)

FemtoClock NG-PLL loss-of-lock is signaled through the nST_LOLF (momentary) and nLS_LOLF (sticky, resettable) status bits and can reported as hardware signal on the LOCK output as well as an interrupt signal on the nINT output.
Channel, Output, and JESD204B Logic

Channel
Each of the four channels, A to D, consists of one to three clock outputs, and one associated to three SYSREF outputs. Each SYSREF output in a channel can be individually configured to generate JESD204B (SYSREF) signals or copy the clock signal of that channel. The fifth channel (E) consists of two clock outputs without SYSREF support in that channel.

If JESD204B/SYSREF operation is assigned to a QREF output, the channel logic controls the outputs: outputs automatically turn on and off in a SYSREF sequence. QREF outputs configured to clock operation can have individually configured output states.

Table 13. Channel Configuration[a]

<table>
<thead>
<tr>
<th>MUX_r</th>
<th>0</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Description</td>
<td>Clock Configuration</td>
<td>JESD204B</td>
</tr>
<tr>
<td>QCLK_y</td>
<td>Clock signal</td>
<td>Clock signal</td>
</tr>
<tr>
<td>QREF_r</td>
<td></td>
<td>SYSREF/JESD204B</td>
</tr>
<tr>
<td>Frequency Divider</td>
<td>QCLK_y and QREF_r: N_x</td>
<td>QCLK_y: N_x</td>
</tr>
<tr>
<td></td>
<td></td>
<td>QREF_r: N_S (Global to all QREF_r)</td>
</tr>
<tr>
<td>Phase Delay</td>
<td>QCLK_y and QREF_r: ( \Phi_{CLK_x} )</td>
<td>QCLK_y: ( \Phi_{CLK_x} )</td>
</tr>
<tr>
<td></td>
<td>( \Phi_{REF_r} ) settings do not apply</td>
<td>QREF_r: ( \Phi_{REF_r} )</td>
</tr>
<tr>
<td>Power-down</td>
<td>Per output</td>
<td>Per channel</td>
</tr>
<tr>
<td>Output Enable</td>
<td>Per output</td>
<td>Per output</td>
</tr>
</tbody>
</table>

[a] \( x = A \) to \( E \)
\( y = A0, A1, A2, B0, B1, C0, C1, D, E0, E1; \)
\( r = A0, A1, A2, B0, B1, C0, C1, D. \)
## Differential Outputs

### Table 14. Output Features

<table>
<thead>
<tr>
<th>Output</th>
<th>Style</th>
<th>Amplitude[^a]</th>
<th>Disable</th>
<th>Power-down</th>
<th>Termination</th>
</tr>
</thead>
<tbody>
<tr>
<td>QCLK_y, QREF_r (Clock)</td>
<td>LVPECL</td>
<td>250–1000mV 4 steps</td>
<td>Yes</td>
<td>Yes</td>
<td>50Ω to V_T</td>
</tr>
<tr>
<td></td>
<td>LVDS</td>
<td></td>
<td></td>
<td></td>
<td>100Ω differential[^b]</td>
</tr>
<tr>
<td>QREF_r (SYSREF)</td>
<td>LVDS</td>
<td>500mV A[1:0] = 01</td>
<td>Controlled by SYSREF[^c]</td>
<td>100Ω differential[^b]</td>
<td></td>
</tr>
<tr>
<td>QOSC</td>
<td>LVPECL</td>
<td>250–750mV 3 steps</td>
<td>Yes</td>
<td>Yes</td>
<td>50Ω to V_T</td>
</tr>
<tr>
<td></td>
<td>LVDS</td>
<td></td>
<td></td>
<td></td>
<td>100Ω differential[^b]</td>
</tr>
</tbody>
</table>

[^a]: Amplitudes are measured single-endedly. Differential amplitudes supported are 500mV, 1000mV, 1500mV and 2000mV.
[^b]: AC coupling and DC coupling supported.
[^c]: State of SYSREF outputs is controlled by an internal SYSREF state machine.

### Table 15. Individual Clock Output Settings[^a]

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Off</td>
<td>100Ω differential or no termination</td>
<td>Off</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>X</td>
<td>XX</td>
<td>On</td>
<td>100Ω differential (LVDS)</td>
<td>Disable (logic low)</td>
<td>250</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>00</td>
<td>Off</td>
<td>50Ω to V_T (LVPECL)</td>
<td>Enable</td>
<td>1000</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0</td>
<td>00</td>
<td>On</td>
<td>50Ω to V_T = V_DD_V - 1.50V (LVPECL)</td>
<td>Enable</td>
<td>250</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>01</td>
<td>Off</td>
<td>50Ω to V_T = V_DD_V - 1.75V (LVPECL)</td>
<td>Enable</td>
<td>500</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>10</td>
<td>On</td>
<td>50Ω to V_T = V_DD_V - 2.00V (LVPECL)</td>
<td>Enable</td>
<td>750</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>11</td>
<td>Off</td>
<td>50Ω to V_T = V_DD_V - 2.25V (LVPECL)</td>
<td>Enable</td>
<td>1000</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>11</td>
<td>On</td>
<td>50Ω to V_T = V_DD_V - 2.50V (LVPECL)</td>
<td>Enable</td>
<td>1000</td>
</tr>
</tbody>
</table>

[^a]: Applicable to clock outputs: QCLK\_y and QREF\_r outputs in clock mode (MUX\_r = 0).
[^b]: Power-down modes are available for the individual channels A-E and the outputs QCLK\_y (A0 to E1).
[^c]: Output enable is supported on each individual QCLK\_y and QREF\_r output.
[^d]: Output amplitude control is supported on each individual QCLK\_y and QREF\_r output.
Table 16. Individual SYSREF Output Settings[a]

<table>
<thead>
<tr>
<th>PD</th>
<th>STYLE</th>
<th>EN</th>
<th>nBIAS</th>
<th>A[1:0]</th>
<th>Output Power</th>
<th>Termination</th>
<th>State</th>
<th>Amplitude (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Off</td>
<td>Off</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>01</td>
<td>On[b]</td>
<td>100Ω differential (LVDS)</td>
<td>Disable (logic low)</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>X</td>
<td>1</td>
<td>XX</td>
<td>X</td>
<td>50Ω to V_T = V_DD_V − 1.50V (LVPECL)</td>
<td>Enable</td>
<td>500</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>01</td>
<td>X</td>
<td>50Ω to V_T = V_DD_V − 1.00V (LVPECL)</td>
<td>Disable (logic low)</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>50Ω to V_T = V_DD_V − 2.00V (LVPECL)</td>
<td>Enable</td>
<td>500</td>
</tr>
</tbody>
</table>

[a] Applicable QREF_r outputs when configured as SYSREF output (MUX_r = 1).

[b] Output amplitude should be set to a 500mV swing (A[1:0] to 01) by SPI. SYSREF output states are controlled by an internal state machine. An internal SYSREF event will automatically turn SYSREF outputs on. After the event, outputs are automatically turned off. Setting nBIAS = 1 will bias powered-off outputs to the LVDS midpoint voltage.

[c] Output (both Q, and nQ) bias the line to the differential signal cross-point voltage. Available if output is AC-coupled and set to LVDS style.

Table 17. QOSC (VCXO-PLL Output) Settings

<table>
<thead>
<tr>
<th>nPD</th>
<th>STYLE</th>
<th>A[1:0]</th>
<th>Output Power</th>
<th>Termination</th>
<th>Amplitude (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Off</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>00</td>
<td>On</td>
<td>100Ω differential (LVDS)</td>
<td>250</td>
</tr>
<tr>
<td></td>
<td></td>
<td>01</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>10</td>
<td></td>
<td></td>
<td>500</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11</td>
<td></td>
<td></td>
<td>750</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>00</td>
<td></td>
<td>50Ω to V_T = V_DD_V − 1.50V (LVPECL)</td>
<td>250</td>
</tr>
<tr>
<td></td>
<td></td>
<td>01</td>
<td></td>
<td>50Ω to V_T = V_DD_V − 1.75V (LVPECL)</td>
<td>500</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>11</td>
<td></td>
<td>50Ω to V_T = V_DD_V − 2.00V (LVPECL)</td>
<td>750</td>
</tr>
</tbody>
</table>

Table 18. QREF_r Setting for JESD204B Applications

<table>
<thead>
<tr>
<th>BIAS_TYPE</th>
<th>nBIAS_r</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

QREF_r Outputs (LVDS, 500mV Amplitude)

<table>
<thead>
<tr>
<th>Initial</th>
<th>During SYSREF Event</th>
<th>SYSREF Completed</th>
<th>Application</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static low</td>
<td>Start switching for the number of configured SYSREF pulses</td>
<td>Released to static low (QREF = L, nQREF_r = H)</td>
<td>QREF_r DC coupled</td>
</tr>
<tr>
<td>Static LVDS crosspoint level (QREF = nQREF_r = VOS)</td>
<td>Start switching for the number of configured SYSREF pulses</td>
<td>Released to static LVDS crosspoint level (QREF = nQREF_r = VOS)</td>
<td>QREF_r AC coupled</td>
</tr>
</tbody>
</table>

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Output Phase-Delay
Output phase delay is independently supported on both clock and SYSREF outputs.

Table 19. Delay Circuit Settings[a]

<table>
<thead>
<tr>
<th>Delay Circuit</th>
<th>Unit</th>
<th>Steps</th>
<th>Range (ns)</th>
<th>Alignment[b]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock $\Phi_{CLK_x}$</td>
<td>$\frac{1}{f_{VCO}} = 407\text{ps}$</td>
<td>256</td>
<td>$0 – 103.760$</td>
<td>Incident rising clock edges are aligned, independent of the divider $N_x$ across channels</td>
</tr>
<tr>
<td>SYSREF $\Phi_{REF_r}$</td>
<td>Coarse delay: $\frac{1}{2f_{VCO}} = 203\text{ps}$</td>
<td>8</td>
<td>$0 – 1.424$</td>
<td>SYSREF rising edge is aligned to the incident rising clock edge across channels</td>
</tr>
<tr>
<td></td>
<td>Fine delay: 0ps, 25ps, 50ps, 75ps, 85ps, 110ps, 135ps, 160ps</td>
<td>8</td>
<td>$0 – 0.160$</td>
<td></td>
</tr>
<tr>
<td>SYSREF (Global) $\Phi_{REF_S}$</td>
<td>$\frac{1}{f_{VCO}} = 407\text{ps}$</td>
<td>256</td>
<td>$0 – 103.760$</td>
<td>Global alignment of SYSREF signals</td>
</tr>
</tbody>
</table>

[a] Supports $\geq 12$ SYSREF rising edge stops within a device clock period of $1017\text{ps}$ (983.04MHz), $2.034\text{ns}$ (491.52MHz), $4.096\text{ns}$ (245.76MHz), and $8.137\text{ns}$ (122.88MHz), respectively. Clock output inversion supported by setting phase delay to a 180° setting.

[b] Default configuration (all delay settings = 0). $\Phi_{REF_r}$ coarse delay values are exact, fine delay value vary over PVT by $\pm 20\%$.

Configuration for JESD204B Operation

Synchronizing SYSREF and Clock Output Dividers
The SYNC[6:0] divider controls the release of SYSREF pulses at coincident QCLK_y clock edges. For SYSREF operation, set the SYNC divider value to the least common multiple of the clock divider values $N_x$ ($x = A$ to $E$). For instance, if $N_A = N_B = +2$, $N_C = N_D = +3$, $N_E = +4$, set the SYNC divider to $+12$.

SYSREF Generation
A SYSREF event is the generation of one or more consecutive pulses on the QREF outputs. An event can be triggered by SPI commands or by a signal-transition on the EXT_SYS input. The number of SYSREF pulses generated is programmable from 1 to 255. The SYSREF signal can also be programmed to be continuous. The SYSREF pulse rate is configurable to the frequencies shown in Table 20. SYSREF output pulses are aligned to coincident rising clock edges of the clock outputs QCLK_y. Device settings for phase alignment between QCLK_y and QREF_r outputs is detailed in the section, QCLK to QREF Phase Alignment. The following SYSREF pulse generation modes are available and configurable by SPI:
- Counted pulse mode: 1 to 255 pulses are generated by the device. SYSREF activity stops automatically after the transmission of the selected number of pulses and the QREF output powers down.
- Continuous mode. The SYSREF signal is a clock signal.
The generation of SYSREF pulses is configured by SPI commands and is available after the initial setup of output clock divider and QREF phase delay stages. A SYSREF event will automatically turn on the SYSREF outputs. After the event, SYSREF outputs are automatically turned off (power-down). SYSREF outputs with the nBIAS bit set high will bias the outputs at the LVDS crosspoint voltage level (requires BIAS_TYPE = 1).

Table 20. SYSREF Generation[a]

<table>
<thead>
<tr>
<th>SRO</th>
<th>NS</th>
<th>SYSREF Operation (fSYSREF)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>fVCO = 2457.6MHz</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td>Counted pulse mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(Use the SRPC register to configure the number of generated SYSREF pulses)</td>
</tr>
<tr>
<td>0</td>
<td>+64</td>
<td>38.4</td>
</tr>
<tr>
<td>0</td>
<td>+96</td>
<td>25.6</td>
</tr>
<tr>
<td>0</td>
<td>+128</td>
<td>19.2</td>
</tr>
<tr>
<td>0</td>
<td>+192</td>
<td>12.8</td>
</tr>
<tr>
<td>0</td>
<td>+256</td>
<td>9.6</td>
</tr>
<tr>
<td>0</td>
<td>+384</td>
<td>6.4</td>
</tr>
<tr>
<td>0</td>
<td>+512</td>
<td>4.8</td>
</tr>
<tr>
<td>0</td>
<td>+768</td>
<td>3.2</td>
</tr>
<tr>
<td>0</td>
<td>+1024</td>
<td>2.4</td>
</tr>
<tr>
<td>0</td>
<td>+2048</td>
<td>1.2</td>
</tr>
<tr>
<td>0</td>
<td>+4096</td>
<td>0.6</td>
</tr>
<tr>
<td>0</td>
<td>+5120</td>
<td>0.48</td>
</tr>
<tr>
<td>1</td>
<td>+64</td>
<td>38.4</td>
</tr>
<tr>
<td>1</td>
<td>+96</td>
<td>25.6</td>
</tr>
<tr>
<td>1</td>
<td>+128</td>
<td>19.2</td>
</tr>
<tr>
<td>1</td>
<td>+192</td>
<td>12.8</td>
</tr>
<tr>
<td>1</td>
<td>+256</td>
<td>9.6</td>
</tr>
<tr>
<td>1</td>
<td>+384</td>
<td>6.4</td>
</tr>
<tr>
<td>1</td>
<td>+512</td>
<td>4.8</td>
</tr>
<tr>
<td>1</td>
<td>+768</td>
<td>3.2</td>
</tr>
<tr>
<td>1</td>
<td>+1024</td>
<td>2.4</td>
</tr>
<tr>
<td>1</td>
<td>+2048</td>
<td>1.2</td>
</tr>
<tr>
<td>1</td>
<td>+4096</td>
<td>0.6</td>
</tr>
<tr>
<td>1</td>
<td>+5120</td>
<td>0.48</td>
</tr>
</tbody>
</table>

[a] SRO and SRPC are global settings.
Internal SYSREF Generation

SYSREF generation is set to internal (SRG = 0). The SRO setting defines if SYSREF pulses are counted or continuous and the NS[6:0] divider sets the frequency. In counted pulse mode, the SRPC register contains the number of pulses to generate. Any number from 1 to 255 pulses may be generated. SYSREF pulses are generated upon completion of the SPI command RS (SYSREF release). Setting RS activates the SYSREF outputs, loads the number of pulses from the SRPC register and starts the generation of SYSREF pulses synchronized to the incident edge of the clock signals. After the programmed number of pulses are generated, SYSREF outputs will go into logic low state or bias the output voltage to the static LVDS crosspoint level (see Table 18 for settings and details). In continuous mode, SYSREF is a clock signal and the content of the SRPC signal is ignored.

External SYSREF Generation

SYSREF generation is set to external (SRG = 1): SYSREF pulses are generated in response to the detection of a rising edge at the EXT_SYS input. The EXT_SYS input rising edge releases SYSREF pulses. Both SRO and SRPC register settings apply as in internal SYSREF generation mode for generating single shot and repetitive SYSREF output signals. Set RS = 1 to prepare for SYSREF generation; the generation of SYSREF pulses is triggered by a rising edge at EXT_SYS pin.

QCLK to QREF (SYSREF) Phase Alignment

Figure 4 and Table 21 show how to achieve output phase alignment between the QCLK_y clock and the QREF_r SYSREF outputs. Output phase will be different for different N_x dividers. For a given example in Figure 4, the closest (smallest phase error) output alignment is achieved by setting the clock phase delay register $\Phi_{QCLK_y}$ to 0x00, the coarse SYSREF output phase delay register $\Phi_{REF_x}$ to 0x01, fine SYSREF delay to $\Phi_{REF_F_r} = 1$ and the global $\Phi_{REF_S}$ delay register to 0x29. With a SYSREF phase delay setting of $\Phi_{REF_x} = 0x01$, $\Phi_{REF_F_r} = 0$, the QREF_r output phase is in advance of the QCLK_y phase, which is applicable in JESD204B application. Phase delay settings and propagation delays are dependent on the clock and SYSREF frequency dividers, but independent of the SYSREF generation mode (SRG = 0 or SRG = 1). Recommended phase delay setting for several device configurations are shown in Table 21.
Figure 4. QCLK to QREF Phase Alignment

Table 21. Recommended Delay Settings for Closest Clock-SYSREF Output Phase Alignment

<table>
<thead>
<tr>
<th>Divider Configuration</th>
<th>$\Phi_{CLK_y}$</th>
<th>$\Phi_{REF_r}$</th>
<th>$\Phi_{REF_r,F}$</th>
<th>$\Phi_{REF_S}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$N_{A-E} = +3$</td>
<td>0x00</td>
<td>0x01</td>
<td>1</td>
<td>0x29</td>
</tr>
<tr>
<td>$N_S = +384$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$N_{A-E} = +3$, $N_S = +384$</td>
<td>0x00</td>
<td>0x01</td>
<td>1</td>
<td>0x29</td>
</tr>
<tr>
<td>$N_{A-E} = +8$</td>
<td>0x00</td>
<td>0x03</td>
<td>1</td>
<td>0x00</td>
</tr>
<tr>
<td>$N_S = +384$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

[a] QCLK and QREF outputs are aligned on the incident edge.
Deterministic Phase Relationship and Phase Alignment

Input to output delay is deterministic when the device is configured as dual PLL with the BYPV = 0, BYPF = 1 (PLL feedback path through $M_{V0} \times M_{V1}$). Refer to the application note AN-952: 8V19N480/490 Design Guide for JESD204B Output Phase Alignment and Termination for additional information on phase alignment, termination and coupling techniques.

Status Conditions & Interrupts

The device has an interrupt output to signal changes in status conditions. The devices have several conditions that can indicate faults and status changes in the operation of the device. These are shown in Table 22, and can be monitored directly in the status registers. Status bits (named: ST_condition) are read-only and reflect the momentary device status at the time of read-access. Several status bits are also copied into latched bit positions (named: LS_condition). The latched version is controlled by the corresponding fault and status conditions and remains set (“sticky”) until reset by the user by writing “1” to the status register bit. The reset of the status condition only has an effect if the corresponding fault condition is removed, otherwise, the status bit will set again. Setting a status bit on several latched registers can be programmed to generate an interrupt signal (nINT) via settings in the Interrupt Enable bits (named: IE_condition). A setting of “0” in any of these bits will mask the corresponding latched status bits from affecting the interrupt status pin. Setting all IE bits to 0 has the effect of disabling interrupts from the device. Interrupts are cleared by resetting the appropriate bit(s) in the latched register after the underlying fault condition has been resolved. When all valid interrupt sources have been cleared in this manner, this will release the nINT output until the next unmasked fault.

Table 22. Status Bit Functions

<table>
<thead>
<tr>
<th>Status Bit</th>
<th>Latched</th>
<th>Description</th>
<th>Status if Bit is:</th>
<th>Interrupt Enable Bit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>ST_CLK_0</td>
<td>LS_CLK_0</td>
<td>CLK 0 input status</td>
<td>Active</td>
<td>LOS</td>
</tr>
<tr>
<td>ST_CLK_1</td>
<td>LS_CLK_1</td>
<td>CLK 1 input status</td>
<td>Active</td>
<td>LOS</td>
</tr>
<tr>
<td>ST_CLK_2</td>
<td>LS_CLK_2</td>
<td>CLK 2 input status</td>
<td>Active</td>
<td>LOS</td>
</tr>
<tr>
<td>ST_CLK_3</td>
<td>LS_CLK_3</td>
<td>CLK 3 input status</td>
<td>Active</td>
<td>LOS</td>
</tr>
<tr>
<td>nST_LOLV</td>
<td>nLS_LOLV</td>
<td>VCXO-PLL Loss-of-lock</td>
<td>Locked</td>
<td>Loss-of-lock</td>
</tr>
<tr>
<td>nST_LOLF[a]</td>
<td>nLS_LOLF</td>
<td>FemtoClock NG-PLL Loss-of-lock</td>
<td>Locked</td>
<td>Loss-of-lock</td>
</tr>
<tr>
<td>nST_HOLD</td>
<td>nLS_HOLD</td>
<td>Holdover</td>
<td>Not in holdover</td>
<td>Device in holdover</td>
</tr>
<tr>
<td>ST_VCOF</td>
<td>—</td>
<td>FemtoClock NG VCO calibration</td>
<td>Not completed</td>
<td>Completed</td>
</tr>
<tr>
<td>ST_SEL[1:0]</td>
<td>—</td>
<td>Clock input selection</td>
<td>00 = CLK_0</td>
<td>01 = CLK_1</td>
</tr>
<tr>
<td>ST_REF</td>
<td>LS_REF</td>
<td>PLL reference status</td>
<td>Valid reference</td>
<td>Reference lost[b]</td>
</tr>
</tbody>
</table>

[a] If the VCXO-PLL is bypassed by setting BYPV = 1, VCXO-PLL lock status is blocked from affecting the LOCK pin.

[b] Manual and short-term holdover mode: 0 indicates if the reference selected by SEL[1:0] is lost, 1 if not lost.

Automatic with holdover mode: 0 indicates the reference is lost and while still in holdover, or no valid CLK[3:0].

Automatic mode: 0 indicates no valid CLK[3:0].
Device Startup, Reset, and Synchronization

At startup, an internal POR (power-on reset) resets the device and sets all register bits to their default value. The device forces the VCXO control voltage at the LFV pin to half of the power supply voltage to center the VCXO-frequency. In the default configuration the QCLK_y and QREF_r outputs are disabled at startup.

Recommended Configuration Sequence

1. (Optional) set the value of the CPOL register bit to define the SPI read mode, so that SPI settings can be validated by subsequent SPI read accesses.

2. Configure all PLL settings, output divider and delay circuits as well as other device configurations:
   a. BYPF and BYPV for the desired PLL operation mode and configure the PLL dividers P_V, M_V0, M_V1, M_F and P_F as required to achieve PLL lock (see Table 2 for details).
   b. VCXO-PLL lock detect window by configuring the phase settings \( \Phi_{\text{MV0}} \) and \( \Phi_{\text{PV}} \).
   c. Charge pump currents for both PLLs (CPV[4:0] and CPF[4:0]) and POLV for the desired VCXO polarity.
   d. (optional) OSVEN and OFFSET[4:0] for the VCXO-PLL static phase offset.
   e. Channel dividers (see Table 8).
   f. MUX_r for the desired operation of the QREF_r outputs.
   g. QCLK_y, QREF_r and QOSC output features such as desired output power-down state, style and amplitude.
   h. Desired input selection and monitoring modes: this involves nM/A[1:0] and SEL[1:0] for input selection. In any of the automatic modes, configure PRIO[1:0]_n and REVS. Configure the CNTH[7:0], CNTR[1:0] counters for the desired holdover characteristics and DIV4_VAL, CNTV[1:0] for input revalidation if applicable to the operation mode.
   i. Individual \( \Phi_{\text{CLK}_X} \) and \( \Phi_{\text{REF}_r} \) registers and the global delay \( \Phi_{\text{REF}_S} \) register for the desired phase delay between clock and SYSREF outputs; (see QCLK to QREF (SYSREF) Phase Alignment).
   j. Interrupt enable configuration bits IE_status_condition, as desired for fault reporting on the nINT output.

3. For SYSREF operation:
   a. Configure the N_S and SYNC divider as described in, Synchronizing SYSREF and Clock Output Dividers.
   b. Configure the SYSREF registers SRG, SRO and SRPC[7:0] according to the desired SYSREF operation.

4. Set the initialization bit INIT_CLK. This will initiate all divider and delay circuits and synchronize them to each other. The INIT_CLK bit will self-clear.

5. Set both the RELOCK bit and PB_CAL bit. This step should not be combined with the previous step (setting INIT_CLK) in a multi SPI-byte register access. Both bits will self-clear.

6. Clear the FVCV bit to release the VCXO control voltage and VCXO-PLL will attempt to lock to the input clock signal starting from its center frequency.

7. Clear the status flags.

<table>
<thead>
<tr>
<th>Table 23. LOCK Output Function</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Status Bit (PLL)</strong></td>
</tr>
<tr>
<td>Locked[a]</td>
</tr>
<tr>
<td>Not locked</td>
</tr>
<tr>
<td>Not locked</td>
</tr>
<tr>
<td>Not locked</td>
</tr>
</tbody>
</table>

[a] If the VCXO-PLL is bypassed by setting BYPV = 1, VCXO-PLL lock status is blocked from affecting the LOCK pin.
8. At this point, the basic configuration of the registers 0x00 to 0x73 should be completed and the SPI transfer ended (set nCS to high level).

9. In a separate SPI write access, enable the outputs as desired by accessing the output-enable registers 0x74 and 0x76.

10. For SYSREF operation, see Step 9, **SYSREF Frequency Divider, Delay and Starting/Re-Starting SYSREF Pulse Sequences**.

Reserved registers and registers in the address range 0x78 to 0xFF should not be used. Do not write into any registers in the 0x78 to 0xFF range.

**Changing Frequency Dividers and Phase Delay Values**

**Clock Frequency Divider and Delay**

The following procedure has to be applied for a change of a clock divider and phase delay value \( N_{A-E} \) and \( \Phi_{CLKA-E} \):

1. (Optional) set the value of the CPOL register to define the SPI read mode, so that SPI settings can be validated by subsequent SPI read accesses.

2. (Optional) disable the outputs whose frequency divider or delay value is changed.

3. Configure the \( N_{A-E} \) dividers and the delay circuits \( \Phi_{CLKA-E} \) to the desired new values.

4. (Optional) configure the SYNC divider if required for synchronization between clock and SYSREF signals.

5. Set the initialization bit INIT_CLK. This will initiate all divider and delay circuits and synchronize them to each other. The INIT_CLK bit will self-clear. During this initialization step, all QCLK\(_y\) and QREF\(_r\) outputs are reset to the logic low state.

6. Set the RELOCK bit. This step should not be combined with the setting INIT_CLK in a multi SPI-byte register access. Bit will self-clear.

7. (Optional) enable the outputs whose frequency divider was changed.

**SYSREF Frequency Divider, Delay and Starting/Re-Starting SYSREF Pulse Sequences**

The following procedure has to be applied for a change of a SYSREF divider and phase delay value \( N_S \) and \( \Phi_{REF_S} \):

1. (Optional) set the value of the CPOL register to define the SPI read mode, so that SPI settings can be validated by subsequent SPI read accesses.

2. (Optional) disable the outputs whose frequency divider or delay value is changed.

3. Configure any \( N_S \) divider and any delay circuits \( \Phi_{REF_S} \) to their desired new values.

4. Configure the SYNC divider if required for synchronization between clock and SYSREF signals.

5. Set the initialization bit INIT_CLK. This will initiate all divider and delay circuits and synchronize them to each other. The INIT_CLK bit will self-clear. During this initialization step, all QCLK\(_y\) and QREF\(_r\) outputs are reset to the logic low state.

6. Set the RELOCK bit. This step should not be combined with the setting INIT_CLK in a multi SPI-byte register access. Bit will self-clear.

7. Set the SRO bit to counted pulse mode, or to continue pulse mode, as desired.

8. (Optional) enable the outputs whose frequency divider was changed.

9. For SYSREF operation, set the RS bit to start (or re-start) generating the configured number of SYSREF pulses.
   a. In internal SYSREF generation mode (SRG = 0) the SYSREF pulses are generated as a result of setting the RS bit. Set RS for each repeated SYSREF generation.
   b. In external SYSREF mode the SYSREF pulses are generated at the next rising edge of the EXT_SYS input. Set RS before each rising edge at the EXT_SYS input.
**SPI Interface**

The device has a 3-wire serial control port capable of responding as a slave in an SPI configuration to allow read and write access to any of the internal registers for device programming or read back. The SPI interface consists of the SCLK (clock), SDAT (serial data input and output), and nCS (chip select) pins. A data transfer consists any integer multiple of 8 bits and is always initiated by the SPI master on the bus. Internal register data is organized in SPI bytes of 8 bit each.

If nCS is at logic high, the SDAT data I/O is in high-impedance state and the SPI interface of the device is disabled.

In a write operation, data on SDAT will be clocked in on the rising edge of SCLK. In a read operation, data on SDAT will be clocked out on the falling or rising edge of SCLK depending on the CPOL setting (CPOL = 0: output data changes on the falling edge, CPOL = 1: output data changes on the rising edge).

**Starting a data transfer** requires nCS to set and hold at logic low level during the entire transfer. Setting nCS = 0 will enable the SPI interface with SDAT in data input mode. The master must initiate the first 8-bit transfer. The first bit presented to the slave is the direction bit R/nW (1 = Read, 0 = Write) and the following seven bits are the address bits A[0:6] pointing to an internal register in the address space 0 to 127. Data is presented with the LSB (least significant bit) first.

**Read operation** from an internal register: A read operation starts with an 8 bit transfer from the master to the slave: SDAT is clocked on the rising edge of SCLK. The first bit is the direction bit R/nW which must be to “1” to indicate a read transfer, followed by seven address bits A[0:6]. After the first 8 bits are clocked into SDAT, the SDAT I/O changes to output: The register content addressed by A[0:6] is loaded into the shift register and the next eight SCLK falling (CPOL = 1) clock cycles will then present the loaded register data on the SDAT output and transfer these to the master. Transfers must be completed by de-asserting nCS after any multiple 8 of SCLK cycles. If nCS is de-asserted at any other number of SCLKs, the SPI behavior is undefined. SPI byte (8 bit) and back-to-back read transfers of multiple registers are supported with an address auto-increment. During multiple transfers, nCS must stay at logic low level and SDAT will present multiple registers (A), (A +1), (A +2), etc. with each eight SCLK cycles. During SPI Read operations, the user may continue to hold nCS low and provide further bytes of data for up to a total of 127 bytes in a single block read.

**Write operation** to a device register: During a write transfer, an SPI master transfers one or more bytes of data into the internal registers of the device. A write transfer starts by asserting nCS to low logic level. The first bit presented by the master must set the direction bit R/nW to 0 (Write) and the seven address bits A[0:6] must contain the 7-bit register address. Bits D0 to D7 contain 8 bit of payload data, which is written into the register addressed by A[0:6] at the end of a 8-bit write transfer. Multiple, subsequent register transfers from the master to the slave are supported by holding nCS asserted at logic low level during write transfers. The 7 bit register address will auto-increment. Transfers must be completed by de-asserting nCS after any multiple eight of SCLK cycles. If nCS is de-asserted at any other number of SCLKs, the SPI behavior is undefined.

**End of transfer**: After nCS is de-asserted to logic “1”, the SPI bus is available to transfers to other slaves on the SPI bus. The READ (Figure 5) and WRITE (Figure 6) diagrams display the transfer of two bytes of data from and into registers.

**Registers 0x78 to 0xFF**. Registers in the address range 0x78 to 0xFF should not be used. Do not write into any registers in the 0x78 to 0xFF range.
Figure 5. Logic Diagram: READ Data from Registers for CPOL = 0 and CPOL = 1

Figure 6. Logic Diagram: WRITE Data into Registers

Table 24. SPI Read / Write Cycle Timing Parameters

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Condition</th>
<th>Minimum</th>
<th>Maximum</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>fSCLK</td>
<td>SCLK Frequency</td>
<td></td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>tS1</td>
<td>Setup Time, nCS (falling) to SCLK (rising)</td>
<td></td>
<td>5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tS2</td>
<td>Setup Time, SDAT (input) to SCLK (rising)</td>
<td></td>
<td>5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tS3</td>
<td>Setup Time, nCS (rising) to SCLK (rising)</td>
<td></td>
<td>5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tH1</td>
<td>Hold Time, SCLK (rising) to SDAT (input)</td>
<td></td>
<td>5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tH2</td>
<td>Hold Time, SCLK (falling) to nCS (rising)</td>
<td></td>
<td>5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tPD1F</td>
<td>Propagation Delay, SCLK (falling) to SDAT</td>
<td>CPOL = 0</td>
<td>12</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tPD1R</td>
<td>Propagation Delay, SCLK (rising) to SDAT</td>
<td>CPOL = 1</td>
<td>12</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tPD2</td>
<td>Propagation Delay, nCS to SDAT (disable)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Figure 7. SPI Timing Diagram

Table 25. Serial Interface Logic Voltage

<table>
<thead>
<tr>
<th>SELSV</th>
<th>SPI Interface (SCLK, SDAT, nCS, EXT_SYS) Logic Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 (default)</td>
<td>1.8V</td>
</tr>
<tr>
<td>1</td>
<td>3.3V</td>
</tr>
</tbody>
</table>
## Register Descriptions

### List of Registers

#### Table 26. Configuration Registers

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00–0x01</td>
<td>PLL Frequency Divider: $\Phi_{MV}, M_{V0}$</td>
</tr>
<tr>
<td>0x02–0x03</td>
<td>PLL Frequency Divider: $M_{V1}, BYPF$</td>
</tr>
<tr>
<td>0x04–0x05</td>
<td>VCXO-PLL Control: Frequency Divider, $\Phi_{PV}, P_{V}$</td>
</tr>
<tr>
<td>0x06–0x07</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x08–0x09</td>
<td>PLL Frequency Divider $M_{F}$</td>
</tr>
<tr>
<td>0x0A</td>
<td>VCXO-PLL Control BYPV</td>
</tr>
<tr>
<td>0x0B</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x0C</td>
<td>PLL Frequency Divider: $P_{F}, FDF$</td>
</tr>
<tr>
<td>0x0D–0x0F</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x10–0x12</td>
<td>VCXO-PLL Control, output state QOSC</td>
</tr>
<tr>
<td>0x13</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x14</td>
<td>Input Selection Mode Priority</td>
</tr>
<tr>
<td>0x15</td>
<td>Input Selection Mode Switching</td>
</tr>
<tr>
<td>0x16</td>
<td>Input Selection Mode CNTH</td>
</tr>
<tr>
<td>0x17</td>
<td>Input Selection Mode: CNTR, CNTV</td>
</tr>
<tr>
<td>0x18</td>
<td>SYSREF Control: divider, PD</td>
</tr>
<tr>
<td>0x19</td>
<td>SYSREF Control SYNC</td>
</tr>
<tr>
<td>0x1A</td>
<td>SYSREF Control SRPC</td>
</tr>
<tr>
<td>0x1B</td>
<td>SYSREF Control $\Phi_{REF, S}$</td>
</tr>
<tr>
<td>0x1C</td>
<td>SYSREF Control SRG, SRO</td>
</tr>
<tr>
<td>0x1D–0x1F</td>
<td>PLL Control</td>
</tr>
<tr>
<td>0x20–0x22</td>
<td>Channel A</td>
</tr>
<tr>
<td>0x23</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x24</td>
<td>Output State QCLK_A0</td>
</tr>
<tr>
<td>0x25</td>
<td>Output State QCLK_A1</td>
</tr>
<tr>
<td>0x26</td>
<td>Output State QCLK_A2</td>
</tr>
<tr>
<td>0x27</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x28</td>
<td>QREF_A0: delay, MUX</td>
</tr>
<tr>
<td>0x29</td>
<td>QREF_A1: delay, MUX</td>
</tr>
<tr>
<td>0x2A</td>
<td>QREF_A2: delay, MUX</td>
</tr>
<tr>
<td>0x2B</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x2C</td>
<td>Output State QREF_A0</td>
</tr>
<tr>
<td>Register Address</td>
<td>Register Description</td>
</tr>
<tr>
<td>------------------</td>
<td>---------------------------------------</td>
</tr>
<tr>
<td>0x2D</td>
<td>Output State QREF_A1</td>
</tr>
<tr>
<td>0x2E</td>
<td>Output State QREF_A2</td>
</tr>
<tr>
<td>0x2F</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x30–0x32</td>
<td>Channel B</td>
</tr>
<tr>
<td>0x33</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x34</td>
<td>Output State QCLK_B0</td>
</tr>
<tr>
<td>0x35</td>
<td>Output State QCLK_B1</td>
</tr>
<tr>
<td>0x36–0x37</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x38</td>
<td>QREF_B0: delay, MUX</td>
</tr>
<tr>
<td>0x39</td>
<td>QREF_B1: delay, MUX</td>
</tr>
<tr>
<td>0x3A–0x3B</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x3C</td>
<td>Output State QREF_B0</td>
</tr>
<tr>
<td>0x3D</td>
<td>Output State QREF_B1</td>
</tr>
<tr>
<td>0x3E–0x3F</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x40–0x42</td>
<td>Channel C</td>
</tr>
<tr>
<td>0x43</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x44</td>
<td>Output State QCLK_C0</td>
</tr>
<tr>
<td>0x45</td>
<td>Output State QCLK_C1</td>
</tr>
<tr>
<td>0x46–0x47</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x48</td>
<td>QREF_C0: delay, MUX</td>
</tr>
<tr>
<td>0x49</td>
<td>QREF_C1: delay, MUX</td>
</tr>
<tr>
<td>0x4A–0x4B</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x4C</td>
<td>Output State QREF_C0</td>
</tr>
<tr>
<td>0x4D</td>
<td>Output State QREF_C1</td>
</tr>
<tr>
<td>0x4E–0x4F</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x50–0x52</td>
<td>Channel D</td>
</tr>
<tr>
<td>0x53</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x54</td>
<td>Output State QCLK_D</td>
</tr>
<tr>
<td>0x55–0x57</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x58</td>
<td>QREF_D: delay, MUX</td>
</tr>
<tr>
<td>0x59–0x5B</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x5C</td>
<td>Output State QREF_D</td>
</tr>
<tr>
<td>0x5D–0x5F</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x60–0x62</td>
<td>Channel E</td>
</tr>
<tr>
<td>0x63</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
Register Descriptions

This section contains all addressable registers, sorted by function, followed for a detailed description of each bit field for each register. Several functional blocks with multiple instances in this device have individual registers controlling their settings, but since the registers have an identical format and bit meaning, they are described only once, with an additional table to indicate their addresses and default values. All writable register fields will come up with a default values as indicated in the factory defaults column unless altered by values loaded from non-volatile storage during the initialization sequence.

Fixed read-only bits will have defaults as indicated in their specific register descriptions. Read-only status bits will reflect valid status of the conditions they are designed to monitor once the internal power-up reset has been released. Unused registers and bit positions are Reserved. Reserved bit fields may be used for internal debug test and debug functions.

Channel and Clock Output Registers

The content of the channel register and clock output registers set the channel state, the clock divider, the QCLK output state and clock phase delay.

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x64</td>
<td>Output State QCLK_E0</td>
</tr>
<tr>
<td>0x65</td>
<td>Output State QCLK_E1</td>
</tr>
<tr>
<td>0x66–0x67</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x68–0x69</td>
<td>Interrupt Enable</td>
</tr>
<tr>
<td>0x6A–0x6B</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x6C</td>
<td>Status (Latched)</td>
</tr>
<tr>
<td>0x6D</td>
<td>Status (Momentary)</td>
</tr>
<tr>
<td>0x6E</td>
<td>Status (Latched)</td>
</tr>
<tr>
<td>0x6F</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x70</td>
<td>SYSREF Control RS</td>
</tr>
<tr>
<td>0x71–0x73</td>
<td>General Control</td>
</tr>
<tr>
<td>0x74–0x75</td>
<td>Output State QCLK</td>
</tr>
<tr>
<td>0x76</td>
<td>Output State QREF</td>
</tr>
<tr>
<td>0x77</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x78–0x7A</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x7B</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x7C–0x7F</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x80–0xFF</td>
<td>Reserved</td>
</tr>
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</table>

Table 26. Configuration Registers (Cont.)
### Table 27. Channel and Clock Output Register Bit Field Locations

<table>
<thead>
<tr>
<th>Register Address</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x20: Channel A</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x30: Channel B</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x40: Channel C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x50: Channel D</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x60: Channel E</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>0x21: Channel A</td>
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<td></td>
<td></td>
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<td></td>
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</tr>
<tr>
<td>0x31: Channel B</td>
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</tr>
<tr>
<td>0x41: Channel C</td>
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<td></td>
</tr>
<tr>
<td>0x51: Channel D</td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x61: Channel E</td>
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</tr>
<tr>
<td>0x22: Channel A</td>
<td></td>
<td></td>
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<td></td>
<td>PD_A</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>0x32: Channel B</td>
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<td></td>
<td></td>
<td></td>
<td>PD_B</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x42: Channel C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PD_C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x52: Channel D</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PD_D</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x62: Channel E</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PD_E</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x24: QCLK_A0</td>
<td>PD_A</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>STYLE_A0</td>
<td>A_A0[1:0]</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>0x25: QCLK_A1</td>
<td>PD_A1</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>STYLE_A1</td>
<td>A_A1[1:0]</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>0x26: QCLK_A2</td>
<td>PD_A2</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>STYLE_A2</td>
<td>A_A2[1:0]</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>0x28: QCLK_B0</td>
<td>PD_B0</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>STYLE_B0</td>
<td>A_B0[1:0]</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>0x29: QCLK_B1</td>
<td>PD_B1</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>STYLE_B1</td>
<td>A_B1[1:0]</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>0x2A: QCLK_C0</td>
<td>PD_C0</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>STYLE_C0</td>
<td>A_C0[1:0]</td>
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<td></td>
</tr>
<tr>
<td>0x2B: QCLK_C1</td>
<td>PD_C1</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>STYLE_C1</td>
<td>A_C1[1:0]</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>0x2C: QCLK_D</td>
<td>PD_D</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>STYLE_D</td>
<td>A_D[1:0]</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>0x2E: QCLK_E0</td>
<td>PD_E0</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>STYLE_E0</td>
<td>A_E0[1:0]</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>0x2F: QCLK_E1</td>
<td>PD_E1</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>STYLE_E1</td>
<td>A_E1[1:0]</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>0x74</td>
<td>EN_QCLK_A0</td>
<td>EN_QCLK_A1</td>
<td>EN_QCLK_A2</td>
<td>EN_QCLK_B0</td>
<td>EN_QCLK_B1</td>
<td>EN_QCLK_C0</td>
<td>EN_QCLK_C1</td>
<td>EN_QCLK_D</td>
</tr>
<tr>
<td>0x75</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>EN_QCLK_E1</td>
<td>EN_QCLK_E0</td>
<td></td>
</tr>
<tr>
<td>Bit Field Name</td>
<td>Field Type</td>
<td>Default (Binary)</td>
<td>Description</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>---------------</td>
<td>------------</td>
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<td>-------------</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>N_x[7:0]</td>
<td>R/W</td>
<td>0000 0100</td>
<td>Output Frequency Divider N:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>N_x[7:0]</td>
<td>Divider Value</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0000 0000</td>
<td>+1</td>
<td>0100 0011</td>
<td>+10</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0000 0000</td>
<td>+2</td>
<td>0100 0100</td>
<td>+12</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0000 0001</td>
<td>+3</td>
<td>0100 0110</td>
<td>+16</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0000 0010</td>
<td>+4</td>
<td>0100 1011</td>
<td>+20</td>
<td></td>
<td></td>
</tr>
<tr>
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<td></td>
<td></td>
<td>0000 0011</td>
<td>+5</td>
<td>0100 1100</td>
<td>+24</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>0000 0100</td>
<td>+6</td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td>0000 0110</td>
<td>+8</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>0101 0011</td>
<td>+30</td>
<td>0101 1011</td>
<td>+40</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0100 1110</td>
<td>+32</td>
<td>0101 0110</td>
<td>+48</td>
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<td></td>
<td></td>
<td>0101 0100</td>
<td>+36</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>0110 0011</td>
<td>+50</td>
<td>0110 0100</td>
<td>+60</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0101 1110</td>
<td>+64</td>
<td></td>
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<tr>
<td></td>
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<td></td>
<td>0101 1111</td>
<td>+72</td>
<td>0110 0110</td>
<td>+80</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0110 1110</td>
<td>+96</td>
<td>0111 1011</td>
<td>+100</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0111 1100</td>
<td>+120</td>
<td>0111 1110</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0111 0110</td>
<td>+128</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>0111 1110</td>
<td>+160</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PD_x</td>
<td>R/W</td>
<td>0</td>
<td>0 = Channel x is powered-up.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 = Channel x is powered-down.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PD_y</td>
<td>R/W</td>
<td>0</td>
<td>0 = Output QCLK_y is powered-up.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 = Output QCLK_y is powered-down.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ΦCLK_x[7:0]</td>
<td>R/W</td>
<td>0000 0000</td>
<td>CLK_x Phase Delay:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>ΦCLK_x[7:0]</td>
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<td></td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>Delay in ps = ΦCLK_x × 407ps (256 steps):</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0000 0000 = 0ps</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>...</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1111 1111 = 103.760ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Table 28. Channel and Clock Output Register Descriptions[^a] (Cont.)

<table>
<thead>
<tr>
<th>Bit Field Name</th>
<th>Field Type</th>
<th>Default (Binary)</th>
<th>Description</th>
</tr>
</thead>
</table>
| A_y[1:0]       | R/W        | 00               | QCLK_y Output Amplitude
|                |            |                  | Setting for STYLE = 0 (LVDS) | Setting for STYLE = 1 (LVPECL) |
|                |            | A[1:0] = 00: 250mV |
|                |            | A[1:0] = 01: 500mV |
|                |            | A[1:0] = 10: 750mV |
|                |            | A[1:0] = 11:1000mV |
|                |            | Termination: 100Ω across |
|                |            | Termination: 50Ω to VT |
| STYLE_y        | R/W        | 0                | QCLK_y Output Format: |
|                |            | 0 = Output is LVDS (requires an LVDS 100Ω output termination). |
|                |            | 1 = Output is LVPECL (requires an LVPECL 50Ω output termination of the specified recommended termination voltage). |
| EN_y           | R/W        | 0                | QCLK_y Output Enable: |
|                |            | 0 = QCLK_y Output is disabled at the logic low state. |
|                |            | 1 = QCLK_y Output is enabled. |

[^a] x = A, B, C, D, E; y = A0, A1, A2, B0, B1, C0, C1, D, E0, E1; r = A0, A1, A2, B0, B1, C0, C1, D.
QREF Output State Registers

The content of the output registers set the output frequency and divider, several output states, the power state, the output style and amplitude.

Table 29. QREF Output State Register Bit Field Locations

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Bit Field Location</th>
<th>Bit Location</th>
<th>Bit Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x28: QREF_A0</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
</tr>
<tr>
<td>0x29: QREF_A1</td>
<td>Reserved</td>
<td>∅REF_F[1:0]_A0</td>
<td>MUX_A0</td>
</tr>
<tr>
<td>0x2A: QREF_A2</td>
<td></td>
<td>∅REF_F[1:0]_A1</td>
<td>MUX_A1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>∅REF_F[1:0]_A2</td>
<td>MUX_A2</td>
</tr>
<tr>
<td>0x38: QREF_B0</td>
<td>Reserved</td>
<td>∅REF_F[1:0]_B0</td>
<td>MUX_B0</td>
</tr>
<tr>
<td>0x39: QREF_B1</td>
<td></td>
<td>∅REF_F[1:0]_B1</td>
<td>MUX_B1</td>
</tr>
<tr>
<td>0x48: QREF_C0</td>
<td>Reserved</td>
<td>∅REF_F[1:0]_C0</td>
<td>MUX_C0</td>
</tr>
<tr>
<td>0x49: QREF_C1</td>
<td></td>
<td>∅REF_F[1:0]_C1</td>
<td>MUX_C1</td>
</tr>
<tr>
<td>0x58: QREF_D</td>
<td>Reserved</td>
<td>∅REF_F[1:0]_D</td>
<td>MUX_D</td>
</tr>
<tr>
<td>0x2C: QREF_A0</td>
<td></td>
<td>Reserved</td>
<td>∅REF_D[2:0]</td>
</tr>
<tr>
<td>0x2D: QREF_A1</td>
<td></td>
<td>Style_A0</td>
<td></td>
</tr>
<tr>
<td>0x2E: QREF_A2</td>
<td></td>
<td>Style_A1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Style_A2</td>
<td></td>
</tr>
<tr>
<td>0x3C: QREF_B0</td>
<td></td>
<td>nBIAS_B0</td>
<td></td>
</tr>
<tr>
<td>0x3D: QREF_B1</td>
<td></td>
<td>nBIAS_B1</td>
<td></td>
</tr>
<tr>
<td>0x4C: QREF_C0</td>
<td></td>
<td>nBIAS_C0</td>
<td></td>
</tr>
<tr>
<td>0x4D: QREF_C1</td>
<td></td>
<td>nBIAS_C1</td>
<td></td>
</tr>
<tr>
<td>0x5C: QREF_D</td>
<td></td>
<td>nBIAS_D</td>
<td></td>
</tr>
<tr>
<td>0x76</td>
<td>EN_QREF_A0</td>
<td>EN_QREF_A1</td>
<td>EN_QREF_A2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>EN_QREF_B0</td>
<td>EN_QREF_B1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>EN_QREF_C0</td>
<td>EN_QREF_C1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>EN_QREF_D</td>
<td></td>
</tr>
</tbody>
</table>

[a] x = A, B, C, D, E;
   y = A0, A1, A2, B0, B1, C0, C1, D, E0, E1;
   r = A0, A1, A2, B0, B1, C0, C1, D.
<table>
<thead>
<tr>
<th>Bit Field Name</th>
<th>Field Type</th>
<th>Default (Binary)</th>
<th>Description</th>
</tr>
</thead>
</table>
| MUX\_r        | R/W        | 1                | 0 = QREF\_r output signal source is the channel’s clock signal.  
1 = QREF\_r output signal source is the centrally generated SYSREF signal. |
| \(\Phi_{REF\_r}[2:0]\) | R/W        | 000              | SYSREF Coarse Phase Delay:  
\(\Phi_{REF\_r}[2:0]\)  
Delay in ps = \(\Phi_{REF\_r}[2:0]\) \(\times\) 203ps (8 steps):  
000 = 0ps  
…  
111 = 1.424ns |
| \(\Phi_{REF\_F[2:0]}\_r\) | R/W        | 000              | SYSREF Fine Phase Delay:  
\(\Phi_{REF\_F[2:0]}\_r\)  
Insert a SYSREF fine phase delay in ps (8 steps) in addition to the delay value in:  
\(\Phi_{REF\_r}[2:0]\)  
000 = 0ps  
001 = 25ps  
010 = 50ps  
011 = 75ps  
100 = 85ps  
101 = 110ps  
110 = 135ps  
111 = 160ps |
| nBIAS\_r      | R/W        | 0                | QREF\_r Output Bias Voltage:  
0 = Output is not voltage biased.  
1 = Output is biased to the LVDS cross-point voltage if BIAS\_TYPE (register 0x19, bit 7) is set to 1. Bit has no effect if BIAS\_TYPE = 0.  
Output bias = 1 requires AC coupling and LVDS style on the corresponding output. |
### QREF Output State Register Descriptions[^a] (Cont.)

<table>
<thead>
<tr>
<th>Bit Field Name</th>
<th>Field Type</th>
<th>Default (Binary)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A_{r}[1:0]</td>
<td>R/W</td>
<td>00</td>
<td>QREF_{r} Output Amplitude</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Setting for STYLE_{r} = 0 (LVDS)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Setting for STYLE_{r} = 1 (LVPECL)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>A[1:0] = 00: 250mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>A[1:0] = 01: 500mV</td>
</tr>
<tr>
<td>PD_{r}</td>
<td>R/W</td>
<td>0</td>
<td>QREF_{r} Output Power-down:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 = Output is powered-up.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 = Output is powered-down. STYLE, EN and A[1:0] settings have no effect.</td>
</tr>
<tr>
<td>STYLE_{r}</td>
<td>R/W</td>
<td>0</td>
<td>QREF_{r} Output Format:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 = Output is LVDS (requires an LVDS 100Ω output termination).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 = Output is LVPECL (requires an LVPECL 50Ω output termination to the specified recommended termination voltage).</td>
</tr>
<tr>
<td>EN_{r}</td>
<td>R/W</td>
<td>0</td>
<td>QREF_{r} Output Enable:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 = Output is disabled at the logic low state.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 = Output is enabled.</td>
</tr>
</tbody>
</table>

[^a]: x = A, B, C, D, E; y = A0, A1, A2, B0, B1, C0, C1, D, E0, E1; r = A0, A1, A2, B0, B1, C0, C1, D.
## PLL Frequency Divider Registers

### Table 31. PLL Frequency Divider Register Bit Field Locations

<table>
<thead>
<tr>
<th>Register Address</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td></td>
<td></td>
<td></td>
<td>PV[2:0]</td>
<td>PD_MV1</td>
<td></td>
<td></td>
<td>MAV0[11:8]</td>
</tr>
<tr>
<td>0x01</td>
<td></td>
<td></td>
<td></td>
<td>MAV0[7:0]</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x02</td>
<td></td>
<td></td>
<td></td>
<td>MAV1[7:0]</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x03</td>
<td>MAV1[8]</td>
<td></td>
<td></td>
<td>MAV1[8]</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x04</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x05</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PV[7:0]</td>
</tr>
<tr>
<td>0x08</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x09</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>MF[8]</td>
</tr>
<tr>
<td>0x0C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x1F</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>VCO_SEL</td>
</tr>
</tbody>
</table>

- **ΦM**: Phase adjustment
- **PV**: Phase voltage
- **MV**: Main voltage
- **MF**: Master frequency
- **PF**: Phase frequency
- **VCO_SEL**: VCO selection
- **Reserved**: Not used or reserved for future use.
Table 32. PLL Frequency Divider Register Descriptions

<table>
<thead>
<tr>
<th>Bit Field Name</th>
<th>Field Type</th>
<th>Default (Binary)</th>
<th>Description</th>
</tr>
</thead>
</table>
| MV0[11:0]      | R/W        | 1100 0000 0000   | VCXO-PLL Feedback-Divider: 
The value of the frequency divider (binary coding). Range: ÷1 to ÷4095 |
| MV1[8:0]       | R/W        | 0 0110 0000      | PLL Feedback-Divider: 
The value of the frequency divider (binary coding). Range: ÷4 to ÷511 |
| PD_MV1         | R/W        | 0                | PLL Feedback-Divider MV1 Power-down/Disabled: 
0 = MV1 Divider is enabled. 
1 = MV1 Divider is powered down and disabled. 
Disabled MV1 to save power consumption in configurations not using the input clock monitors. |
| PV[11:0]       | R/W        | 1100 0000 0000   | VCXO-PLL Input Frequency Pre-Divider: 
The value of the frequency divider (binary coding). Range: ÷1 to ÷4095 |
Table 32. PLL Frequency Divider Register Descriptions (Cont.)

<table>
<thead>
<tr>
<th>Bit Field Name</th>
<th>Field Type</th>
<th>Default (Binary)</th>
<th>Description</th>
</tr>
</thead>
</table>
| MF[8:0]        | R/W        | 0 0001 1000      | FemtoClock NG Pre-Divider:  
The value of the frequency divider (binary coding).  
Value: ÷24  
Range: ÷8 to ÷511 |
| PF[5:0]        | R/W        | 00 0000          | FemtoClock NG Pre-Divider:  
The value of the frequency divider (binary coding).  
Value: Bypass  
Range: +1 to +63  
00 0000: PF is bypassed |
| FDF            | R/W        | 0                | Frequency Doubler:  
The input frequency of the FemtoClock NG PLL (2nd stage) is:  
Value: f_{VCXO} ÷ PF  
0 = The output signal of the BYPV multiplexer, divided by the PF divider.  
1 = The output signal of the BYPV multiplexer, doubled in frequency.  
Use this setting to improve phase noise. The PF divider has no effect if FDF = 1. |
| VCO_SEL        | R/W        | 0                | VCO Select: for 8v19n490-24, 8V19N490-19  
0 = Selects VCO-0, f_{VCO} = 2949.12 – 3072MHz  
1 = Selects VCO-1, f_{VCO} = 2400 – 2500MHz |
## VCXO-PLL Control Registers

### Table 33. VCXO-PLL Control Register Bit Field Locations

<table>
<thead>
<tr>
<th>Bit Field Location</th>
<th>Register Address</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>MV1[8]</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>ByPF</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0x0A</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>ByPV</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0x10</td>
<td>POLV</td>
<td>FVCV</td>
<td>Reserved</td>
<td></td>
<td></td>
<td>CPV[4:0]</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0x11</td>
<td>nPD_QOSC</td>
<td>STYLE_QOSC</td>
<td>OSVEN</td>
<td></td>
<td></td>
<td></td>
<td>OFFSET[4:0]</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0x12</td>
<td>Reserved</td>
<td>A_QOSC[1:0]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>CPF[4:0]</td>
<td></td>
</tr>
</tbody>
</table>

### Table 34. VCXO-PLL Control Register Descriptions

<table>
<thead>
<tr>
<th>Bit Field Name</th>
<th>Field Type</th>
<th>Default (Binary)</th>
<th>Description</th>
</tr>
</thead>
</table>
| BYPF          | R/W        | 0                | PLL Feedback Bypass:  
|               |            |                  | 0 = VCXO-PLL feedback divider: M V0  
|               |            |                  | 1 = VCXO-PLL feedback divider: M V0 × M V1 |
| BYPV          | R/W        | 0                | VCXO-PLL Bypass:  
|               |            |                  | 0 = VCXO-PLL is enabled.  
|               |            |                  | 1 = VCXO-PLL is disabled and bypassed. |
| POLV          | R/W        | 0                | VCXO Polarity:  
|               |            |                  | 0 = Positive polarity. Use for an external VCXO with a positive f(V C) characteristics.  
|               |            |                  | 1 = Negative polarity. Use for an external VCXO with a negative f(V C) characteristics. |
| FVCV          | R/W        | 1                | VCXO-PLL Force VC Control Voltage:  
|               |            |                  | 0 = Normal operation.  
|               |            |                  | 1 = Forces the voltage at the LFV control pin (VCXO input) to V DD V / 2. VCXO-PLL unlocks and the VCXO is forced to its mid-point frequency. FVCV = 1 is the default setting at startup to center the VCXO frequency. FVCV should be cleared after startup to enable the PLL to lock to the reference frequency. |
| CPV[4:0]      | R/W        | 1 1000 Value: 1.25mA | VCXO-PLL Charge-Pump Current:  
|               |            |                  | Controls the charge pump current I CPV of the VCXO-PLL. Charge pump current is the binary value of this register plus one multiplied by 50µA.  
|               |            |                  | I CPV = 50µA × (CPV[4:0] + 1)  
<p>|               |            |                  | CPV[4:0] = 00000 sets ICPV to the minimum current of 50µA. Maximum charge pump current is 1.6mA. Default setting is 1.25mA: ((24 + 1) × 50µA). |</p>
<table>
<thead>
<tr>
<th>Bit Field Name</th>
<th>Field Type</th>
<th>Default (Binary)</th>
<th>Description</th>
</tr>
</thead>
</table>
| nPD_QOSC      | R/W        | 0                | QOSC Power State:  
0 = Output QOSC is powered-down.  
1 = Output QOSC is powered-up. |
| STYLE_QOSC    | R/W        | 0                | QOSC Output Format:  
0 = Output is LVDS (requires an LVDS 100Ω output termination).  
1 = Output is LVPECL (requires an LVPECL 50Ω output termination of to the specified recommended termination voltage). |
| OSVEN         | R/W        | 0                | VCXO-PLL Offset Enable:  
0 = No offset.  
1 = Offset enabled. A static phase offset of OFFSET[4:0] is applied to the PFD of the VCXO-PLL. |
| OFFSET[4:0]   | R/W        | 0 0000           | VCXO-PLL Static Phase Offset:  
Controls the static phase detector offset of the VCXO-PLL. Phase offset is the binary value of this register multiplied by 0.9° of the PFD input signal (OFFSET[4:0] × fPFD ÷ 400).  
Maximum offset is 31 × 0.9° = 27.9°.  
Setting OFFSET to 0.0° eliminates the thermal noise of an offset current. If the VCXO-PLL input jitter period T Jitter exceeds the average input period: set OFFSET to a value larger than f PFD × T Jitter ÷ 400 to achieve a better charge pump linearity and lower in-band noise of the PLL. |
| CPF[4:0]      | R/W        | 1 1000           | FemtoClock NG-PLL Charge-Pump Current:  
Controls the charge pump current I CPF of the FemtoClock NG PLL. Charge pump current is the binary value of this register plus one multiplied by 200µA.  
I CPF = 200µA × (CPF[4:0] + 1)  
CPV[4:0] = 00000 sets I CPF to the minimum current of 200µA. Maximum charge pump current is 6.4mA. Default setting is 5.0mA: ((24+1) × 200µA). |
| A_QOSC[1:0]   | R/W        | 00               | QOSC Output Amplitude  
Setting for STYLE_r = 0 (LVDS)  
Setting for STYLE_r = 1 (LVPECL)  
| A[1:0] = 00: 250mV  |  
A[1:0] = 01: 500mV  |  
A[1:0] = 10: 500mV  |  
A[1:0] = 11: 750mV  |  
Termination: 100Ω across  
Termination: 50Ω to VT |
### Input Selection Mode Registers

#### Table 35. Input Selection Mode Register Bit Field Locations

<table>
<thead>
<tr>
<th>Register Address</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x14</td>
<td>PRIO_0[1:0]</td>
<td>PRIO_1[1:0]</td>
<td>PRIO_2[1:0]</td>
<td>PRIO_3[1:0]</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x15</td>
<td>Reserved</td>
<td>BLOCK_LOR</td>
<td>DIV4_VAL</td>
<td>REVS</td>
<td>nM/A[1:0]</td>
<td>SEL[1:0]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x16</td>
<td></td>
<td></td>
<td>CNTH[7:0]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x17</td>
<td>CNTR[1:0]</td>
<td>PD_CLK3</td>
<td>PD_CLK2</td>
<td>PD_CLK1</td>
<td>PD_CLK0</td>
<td>CNTV[1:0]</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### Table 36. Input Selection Mode Register Descriptions

<table>
<thead>
<tr>
<th>Bit Field Name</th>
<th>Field Type</th>
<th>Default (Binary)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PRIO_0[1:0]</td>
<td>R/W</td>
<td>CLK_0: 11</td>
<td>Controls the auto-selection priority of the clock input CLK_0 (n = 0…3). If multiple inputs have equal priority, the order within that priority is from CLK0 (highest) to CLK3 (lowest):</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CLK_1: 10</td>
<td>00 = Priority 0 (lowest)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CLK_2: 01</td>
<td>01 = Priority 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CLK_3: 00</td>
<td>10 = Priority 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11 = Priority 3 (highest)</td>
</tr>
<tr>
<td>DIV4_VAL</td>
<td>R/W</td>
<td>0</td>
<td>Pre-divider for CNTV[1:0]. Use the ÷4 pre-divider for input frequencies &gt;250MHz:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Value: +1</td>
<td>0 = ÷1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 = ÷4</td>
</tr>
<tr>
<td>REVS</td>
<td>R/W</td>
<td>0</td>
<td>Revertive Switching:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Value: off</td>
<td>The revertive input switching setting is only applicable to the two automatic selection modes shown in Table 10. If nM/A[1:0] = X0, the REVS setting has no meaning.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 = Disabled: Re-validation of a non-selected input clock has no impact on the clock selection.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 = Enabled: Re-validation of any non-selected input clock(s) will cause a new input selection according to the pre-set input priorities (revertive switch). An input switch is only done if the re-validated input has a higher priority than the current VCXO-PLL reference clock.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Default setting is revertive switching turned off.</td>
</tr>
</tbody>
</table>
In any of the manual selection modes (nM/A[1:0] = 00 or 10), the VCXO-PLL reference input is selected by SEL[1:0]. In any of the automatic selection modes, the VCXO-PLL reference input is selected by an internal state machine according to the input LOS states and the priorities in the input priority registers.

- 00 = Manual selection
- 01 = Automatic selection (no holdover)
- 10 = Short-term holdover
- 11 = Automatic selection with holdover


- 00 = CLK_0
- 01 = CLK_1
- 10 = CLK_2
- 11 = CLK_3

With a VCXO frequency of 122.88MHz and CNTR[1:0] = 10, the counter has a period of (1.066 ms × binary setting). After each zero-transition, the counter automatically re-loads to the setting in this register. The default setting is 136ms (VCXO = 122.88MHz: 1/122.88MHz × 2¹⁷ × 128).

<table>
<thead>
<tr>
<th>Bit Field Name</th>
<th>Field Type</th>
<th>Default (Binary)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>nM/A[1:0]</td>
<td>R/W</td>
<td>00</td>
<td>Reference Input Selection Mode: In any of the manual selection modes (nM/A[1:0] = 00 or 10), the VCXO-PLL reference input is selected by SEL[1:0]. In any of the automatic selection modes, the VCXO-PLL reference input is selected by an internal state machine according to the input LOS states and the priorities in the input priority registers. 00 = Manual selection 01 = Automatic selection (no holdover) 10 = Short-term holdover 11 = Automatic selection with holdover</td>
</tr>
<tr>
<td>SEL[1:0]</td>
<td>R/W</td>
<td>00</td>
<td>VCXO-PLL Input Reference Selection: Controls the selection of the VCXO-PLL reference input in the manual selection modes. In automatic selection modes (nM/A[1:0] = X1), SEL[1:0] has no meaning. 00 = CLK_0 01 = CLK_1 10 = CLK_2 11 = CLK_3</td>
</tr>
<tr>
<td>CNTH[7:0]</td>
<td>R/W</td>
<td>1000 0000</td>
<td>nMA[1:0] = 11 Automatic with holdover: Hold-off counter period. The device initiates a clock fail-over switch upon counter expiration (zero transition). The counters start to counts backwards after an LOS event is detected. The hold-off counter period is determined by the binary number of VCXO-PLL output pulses divided by CNTR[1:0]. With a VCXO frequency of 122.88MHz and CNTR[1:0] = 10, the counter has a period of (1.066 ms × binary setting). After each zero-transition, the counter automatically re-loads to the setting in this register. The default setting is 136ms (VCXO = 122.88MHz: 1/122.88MHz × 2¹⁷ × 128).</td>
</tr>
<tr>
<td>CNTR[1:0]</td>
<td>R/W</td>
<td>10</td>
<td>nMA[1:0] = 11 Automatic with Holdover: Reference Divider</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CNTR[1:0]</th>
<th>CNTH frequency (period; range)</th>
</tr>
</thead>
<tbody>
<tr>
<td>00 = f_VCXO + 2¹⁵</td>
<td>— 122.88MHz VCXO</td>
</tr>
<tr>
<td>01 = f_VCXO + 2¹⁶</td>
<td>1171Hz (0.853ms; 0–217.6ms)</td>
</tr>
<tr>
<td>10 = f_VCXO + 2¹⁷</td>
<td>937.5Hz (1.066ms; 0–272ms)</td>
</tr>
</tbody>
</table>
### Table 36. Input Selection Mode Register Descriptions (Cont.)

<table>
<thead>
<tr>
<th>Bit Field Name</th>
<th>Field Type</th>
<th>Default (Binary)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CNTV[1:0]</td>
<td>R/W</td>
<td>10 Value: 32</td>
<td>Controls the number of required consecutive, valid input reference pulses for clock re-validation on CLK_n (n = 0…3), in number of input periods. At an LOS event, the re-validation counter loads this setting from the register and counts down by one with every valid, consecutive input signal period. Missing input edges (for one input period) will cause this counter to re-load its setting. An input is re-validated when the counter transitions to zero and the corresponding LOS flag is reset.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>DIV4_VAL = 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00 = 2 (shortest possible)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01 = 16</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10 = 32</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11 = 64</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>DIV4_VAL = 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00 = 8 (shortest possible)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01 = 64</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10 = 128</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11 = 256</td>
</tr>
<tr>
<td>PD_CLK_3</td>
<td>R/W</td>
<td>0 Power-up/</td>
<td>Input CLK_n Power-down/ Disable:</td>
</tr>
<tr>
<td>PD_CLK_2</td>
<td></td>
<td>Enabled</td>
<td>0 = Input CLK_n is enabled.</td>
</tr>
<tr>
<td>PD_CLK_1</td>
<td></td>
<td></td>
<td>1 = Input CLK_n is powered-down and disabled.</td>
</tr>
<tr>
<td>PD_CLK_0</td>
<td></td>
<td></td>
<td>Disable individual Input CLK_n input to save power consumption in configurations not using the respective input and in manual switching or short-term holdover mode. Enable inputs CLK_n in configurations with automatic switching.</td>
</tr>
<tr>
<td>BLOCK_LOR</td>
<td>R/W</td>
<td>0 Value: Not</td>
<td>Block Loss-of-reference (input activity) Indicator:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>blocked</td>
<td>VCVXO-PLL Loss-of-lock signals nST_LOLV and nLS_LOLV are triggered by:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 = VCVXO-PLL Loss-of-lock or by inactivity of the selected reference clock.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 = Only VCVXO-PLL loss-of-lock.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>BLOCK_LOR = 1 will also block loss-of-reference from triggering a failure on the LOCK output pin.</td>
</tr>
</tbody>
</table>
SYSREF Control Registers

Table 37. SYSREF Control Register Bit Field Locations

<table>
<thead>
<tr>
<th>Register Address</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x18</td>
<td>PD_S</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>NS[6:0]</td>
</tr>
<tr>
<td>0x19</td>
<td>BIAS_TYPE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>SYNC[6:0]</td>
</tr>
<tr>
<td>0x1A</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>SRPC[7:0]</td>
</tr>
<tr>
<td>0x1B</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>REF_S[7:0]</td>
</tr>
<tr>
<td>0x1C</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>SRG</td>
</tr>
<tr>
<td>0x70</td>
<td>RS</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

Table 38. SYSREF Control Register Descriptions

<table>
<thead>
<tr>
<th>Bit Field Name</th>
<th>Field Type</th>
<th>Default (Binary)</th>
<th>Description</th>
</tr>
</thead>
</table>
| PD_S           | R/W        | 0                | SYSREF Global Power-down (including global delay \(\Phi_s\), SYSREF frequency divider NS):
|                |            |                  | 0 = SYSREF functional blocks are powered-up. |
|                |            |                  | 1 = SYSREF functional blocks are powered-down. |
| NS[6:0]        | R/W        | 010 11 11        | SYSREF Frequency Divider:
|                |            | Value: \(\div1280\) | The value of the frequency divider is set by the product of:
|                |            |                  | 0 = \(+2\) 00 = \(+2\) 00 = \(+2\) 00 = \(+2\) |
|                |            |                  | 1 = \(+4\) 01 = \(+4\) 01 = \(+3\) |
|                |            |                  | 10 = \(+8\) 10 = \(+8\) 10 = \(+4\) |
|                |            |                  | 11 = \(+16\) 11 = \(+16\) 11 = \(+5\) |

The SYSREF contains four serial dividers that can be individually controlled by NS[6], NS[5:4], NS[3:2] and NS[1:0], respectively. The total NS divider is the product of the four serial dividers. Example: to achieve a SYSREF divider value of \(+384 = (2) \times (4) \times (16) \times (3)\), set NS[6] = 0, NS[5:4] = 01, NS[3:2] = 11 and NS[1:0] = 01.

If a given output divider can be achieved by multiple NS[6:0] settings, use the highest possible divider in NS[1:0], then in NS[3:2], followed by NS[5:4] = 11 and then NS[6].
Table 38. SYSREF Control Register Descriptions (Cont.)

<table>
<thead>
<tr>
<th>Bit Field Name</th>
<th>Field Type</th>
<th>Default (Binary)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BIAS_TYPE</td>
<td>R/W</td>
<td>1</td>
<td>U</td>
</tr>
</tbody>
</table>
|                |            |                  | SYSREF Output Voltage Bias:
|                |            |                  | 0 = QREF_r outputs are in a low/high state when nBIAS_r is set to 1 or during a SYSREF event. |
|                |            |                  | 1 = QREF_r outputs are in a cross-point biased state when nBIAS_r is set to 1 or during a SYSREF event. |
| SYNC[6:0]      | R/W        | 00 00 001        | SYSREF Synchronizer divider value. This divider controls the release of SYSREF pulses at coincident QCLK clock edges. For SYSREF operation, set this divider value to the least common multiple of the clock divider values \(N_x (x = A \text{ to } E)\). |
|                |            |                  | For instance, if \(N_A = N_B = +2, N_C = N_D = +3, N_E = +4\) set the SYNC divider to +12. |
|                |            |                  | SYNC6 Description: |
|                |            |                  | 0: SYNC[6] = 0: output frequency divider set by SYNC[2:0]. |
|                |            |                  | SYNC[5:3] | SYNC[2:0] |
|                |            |                  | 000 = +2 | 000 = +2 |
|                |            |                  | 001 = +4 | 001 = +3 |
|                |            |                  | 010 = +6 | 010 = +4 |
|                |            |                  | 011 = +8 | 011 = +5 |
|                |            |                  | 100 = +4 | 100 = +6 |
|                |            |                  | 101 = +8 | 101 = +7 |
|                |            |                  | 110 = +12| 110 = +8 |
|                |            |                  | 111 = +16| 111 = +9 |
|                |            |                  | The frequency divider SYNC is composed of 2 serial dividers that can be individually controlled by the bit fields SYNC[5:3] and SYNC[2:0]. |
|                |            |                  | Set SYNC[6] = 0 to achieve an output divider in the range of \(\{2, 3, 4, 5, 6, 7, 8, 9\}\). |
|                |            |                  | Set SYNC[6] = 1 to achieve an output divider value of \(\{2, 4, 6, 8, 12,16\} \times \{2, 3, 4, 5, 6, 7, 8, 9\}\). |
|                |            |                  | For instance, the output divider of +32 = \(4 \times 8\) is set by SYNC[6:0] = 1001110. |
|                |            |                  | If a given output divider can be achieved by multiple SYNC[6:0] settings, a setting with SYNC[6] = 0 is preferred. If SNYC[6] = 1, the higher divider value should be configured with SYNC[2:0]. |
| SRPC[7:0]      | R/W        | 0000 0010        | SYSREF Pulse Count: |
|                |            | Value: 2         | Binary value of the number of SYSREF pulses generated and output at all enabled QREF outputs. |
|                |            |                  | Allows the generation of 1 to 255 pulses after each write access. |
|                |            |                  | Requires setting SRG = 0, and SRO = 0. |
### Table 38. SYSREF Control Register Descriptions (Cont.)

<table>
<thead>
<tr>
<th>Bit Field Name</th>
<th>Field Type</th>
<th>Default (Binary)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ΦREF_S[7:0]</strong></td>
<td>R/W</td>
<td>0000 0000</td>
<td>ΦREF_S global SYSREF Phase Delay. This setting affects all QREF_r outputs configured as SYSREF: ΦREF_S[7:0]</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Delay in ps = ΦREF_S × 407ps (256 steps): 0000 0000 = 0ps ... 1111 1111 = 103.760ns</td>
</tr>
<tr>
<td><strong>SRG</strong></td>
<td>R/W</td>
<td>0</td>
<td>SYSREF Pulse Generation: 0 = Internal SPI controlled SYSREF generation triggered by the RS bit. 1 = External controlled SYSREF generation using the EXT_SYS pin.</td>
</tr>
<tr>
<td><strong>SRO</strong></td>
<td>R/W</td>
<td>0</td>
<td>SYSREF Pulse Mode: 0 = Counted SYSREF pulse generation mode. Number of pulses is controlled by SRPC[7:0]. 1 = Continuous SYSREF pulse generation.</td>
</tr>
<tr>
<td><strong>RS</strong></td>
<td>W only Auto-Clear</td>
<td>X</td>
<td>Set RS = 1 to initiate the SYSREF pulse generation of SRPC-number of pulses. Powers up the SYSREF circuitry and releases the SYSREF pulse(s) as configured. RS = 1 also phase-aligns the QREF outputs to the QCLK outputs and adds the programmed delay values into the QREF paths. RS auto-clears in SYSREF counted pulse mode (if SRO = 0): SRG = 0 (internal generation): Each setting of RS initiates SYSREF pulse(s). SRG = 1 (external generation): Set RS = 1 to prepare SYSREF generation triggered by a rising edge at the EXT_SYS pin.</td>
</tr>
</tbody>
</table>
# Status Registers

## Table 39. Status Register Bit Field Locations

<table>
<thead>
<tr>
<th>Bit Field Location</th>
<th>Register Address</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reserved</td>
<td>0x68</td>
<td>Reserved</td>
<td>Reserved</td>
<td>IE_LOLF</td>
<td>IE_LOLV</td>
<td>IE_CLK_3</td>
<td>IE_CLK_2</td>
<td>IE_CLK_1</td>
<td>IE_CLK_0</td>
</tr>
<tr>
<td>Reserved</td>
<td>0x69</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>IE_REF</td>
<td>IE_HOLD</td>
</tr>
<tr>
<td>Reserved</td>
<td>0x6C</td>
<td>Reserved</td>
<td>Reserved</td>
<td>nLS_LOLF</td>
<td>nLS_LOLV</td>
<td>LS_CLK_3</td>
<td>LS_CLK_2</td>
<td>LS_CLK_1</td>
<td>LS_CLK_0</td>
</tr>
<tr>
<td>ST_SEL[1:0]</td>
<td>0x6D</td>
<td>ST_SEL[1:0]</td>
<td>nST_LOLF</td>
<td>nST_LOLV</td>
<td>ST_CLK_3</td>
<td>ST_CLK_2</td>
<td>ST_CLK_1</td>
<td>ST_CLK_0</td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td>0x6E</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>LS_REF</td>
<td>nLS_HOLD</td>
</tr>
<tr>
<td>Reserved</td>
<td>0x6F</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>ST_VCOF</td>
<td>ST_REF</td>
<td>nST_HOLD</td>
</tr>
</tbody>
</table>

## Table 40. Status Register Descriptions[a]

<table>
<thead>
<tr>
<th>Bit Field Name</th>
<th>Field Type</th>
<th>Default (Binary)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IE_LOLF</td>
<td>R/W</td>
<td>0</td>
<td>Interrupt Enable for FemtoClock NG-PLL Loss-of-lock:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 = Disabled: Setting nLS_LOLF will not cause an interrupt on nINT.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 = Enabled: Setting nLS_LOLF will assert the nINT output (nINT = 0, interrupt).</td>
</tr>
<tr>
<td>IE_LOLV</td>
<td>R/W</td>
<td>0</td>
<td>Interrupt Enable for VCXO-PLL Loss-of-lock:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 = Disabled: Setting nLS_LOLV will not cause an interrupt on nINT.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 = Enabled: Setting nLS_LOLV will assert the nINT output (nINT = 0, interrupt).</td>
</tr>
<tr>
<td>IE_CLK_n</td>
<td>R/W</td>
<td>0</td>
<td>Interrupt Enable for CLK_n input Loss-of-signal:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 = Disabled: Setting LS_CLK_n will not cause an interrupt on nINT.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 = Enabled: Setting LS_CLK_n will assert the nINT output (nINT = 0, interrupt).</td>
</tr>
<tr>
<td>IE_REF</td>
<td>R/W</td>
<td>0</td>
<td>Interrupt Enable for LS_REF:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 = Disabled: any changes to LS_REF will not cause an interrupt on nINT.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 = Enabled: any changes to LS_REF will assert the nINT output (nINT = 0, interrupt).</td>
</tr>
<tr>
<td>IE_HOLD</td>
<td>R/W</td>
<td>0</td>
<td>Interrupt Enable for Holdover:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 = Disabled: Setting nLS_HOLD will not cause an interrupt on nINT.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 = Enabled: Setting nLS_HOLD will assert the nINT output (nINT = 0, interrupt).</td>
</tr>
<tr>
<td>nLS_LOLF</td>
<td>R/W</td>
<td>—</td>
<td>FemtoClock NG-PLL Loss-of-lock (latched status of nST_LOLF):</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Read 0 = ≥1 Loss-of-lock events detected after the last nLS_LOLF status latch clear.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Read 1 = No Loss-of-lock detected after the last nLS_LOLF status latch clear.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Write 1 = Clear status latch (clears pending nLS_LOLF interrupt).</td>
</tr>
<tr>
<td>Bit Field Name</td>
<td>Field Type</td>
<td>Default (Binary)</td>
<td>Description</td>
</tr>
<tr>
<td>----------------</td>
<td>------------</td>
<td>------------------</td>
<td>-------------</td>
</tr>
</tbody>
</table>
| nLS_LOLV       | R/W        | —                | VCXO-PLL Loss-of-lock (latched status of nST_LOLV):  
Read 0 = ≥1 Loss-of-lock events detected after the last nLS_LOLV status latch clear.  
Read 1 = No Loss-of-lock detected after the last nLS_LOLF status latch clear.  
Write 1 = Clear status latch (clears pending nLS_LOLV interrupt). |
| LS_CLK_n       | R/W        | —                | Input CLK_n Status (latched status of ST_CLK_n):  
Read 0 = ≥1 LOS events detected on CLK_n after the last LS_CLK_n status latch clear.  
Read 1 = No Loss-of-signal detected on CLK_n input after the last LS_CLK_n status latch clear.  
Write 1 = Clear LS_CLK_n status latch (clears pending LS_CLK_n interrupts on nINT). |
| ST_SEL[1:0]    | R          | —                | Input Selection (momentary):  
Reference Input Selection Status of the state machine. In any input selection mode, reflects the input selected by the state machine:  
00 = CLK_0  
01 = CLK_1  
10 = CLK_2  
11 = CLK_3 |
| nST_LOLF       | R          | —                | FemtoClock NG-PLL Loss-of-lock (momentary):  
Read 0 = Loss-of-lock event detected.  
Read 1 = No Loss-of-lock detected.  
A latched version of this status bit is available (nLS_LOLF). |
| nST_LOLV       | R          | —                | VCXO-PLL Loss-of-lock (momentary):  
Read 0 = Loss-of-lock event detected.  
Read 1 = No Loss-of-lock detected.  
A latched version of this status bit is available (nLS_LOLV). |
| ST_CLK_n       | R          | —                | Input CLK_n Status (momentary):  
0 = LOS detected on CLK_n.  
1 = No LOS detected, CLK_n input is active.  
Latched versions of these status bits are available (LS_CLK_n). |
| LS_REF         | R/W        | —                | PLL Reference Status (latched status of ST_REF):  
Read 0 = Reference is lost after the last LS_REF status latch clear.  
Read 1 = Reference is valid after the last LS_REF status latch clear.  
Write 1 = Clear LS_REF status latch (clears pending LS_REF interrupts on nINT). |
### Table 40. Status Register Descriptions[a] (Cont.)

<table>
<thead>
<tr>
<th>Bit Field Name</th>
<th>Field Type</th>
<th>Default (Binary)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>nLS_HOLD</td>
<td>R/W</td>
<td>—</td>
<td>Holdover Status Indicator (latched status of nST_HOLD):&lt;br&gt;Read 0 = VCXO-PLL has entered holdover state at least 1 time after the last nLS_HOLD status latch clear.&lt;br&gt;Read 1 = VCXO-PLL is (or attempts to) lock(ed) to an input clock.&lt;br&gt;Write 1 = Clear status latch (clears pending nLS_HOLD interrupt).</td>
</tr>
<tr>
<td>ST_VCOF</td>
<td>R</td>
<td>—</td>
<td>FemtoClock NG-PLL Calibration Status (momentary):&lt;br&gt;Read 0 = FemtoClock NG PLL auto-calibration is completed.&lt;br&gt;Read 1 = FemtoClock NG PLL calibration is active (not completed).</td>
</tr>
<tr>
<td>ST_REF</td>
<td>R</td>
<td>—</td>
<td>Input Reference Status:&lt;br&gt;0 = No input reference present.&lt;br&gt;1 = Input reference is present.</td>
</tr>
<tr>
<td>nST_HOLD</td>
<td>R</td>
<td>—</td>
<td>Holdover Status Indicator (momentary):&lt;br&gt;0 = VCXO-PLL in holdover state, not locked to any input clock.&lt;br&gt;1 = VCXO-PLL is (or attempts to) lock(ed) to input clock.&lt;br&gt;A latched version of this status bit is available (nLS_HOLD).</td>
</tr>
</tbody>
</table>

[a] CLKn = CLK0, CLK1, CLK2, CLK3.
# General Control Registers

## Table 41. General Control Register Bit Field Locations

<table>
<thead>
<tr>
<th>Bit Field Location</th>
<th>Register Address</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT_CLK</td>
<td>0x71</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>RELOCK</td>
<td>0x72</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>PB_CAL</td>
<td>0x73</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>CPOL</td>
</tr>
</tbody>
</table>

## Table 42. General Control Register Descriptions

<table>
<thead>
<tr>
<th>Bit Field Location</th>
<th>Bit Field Name</th>
<th>Field Type</th>
<th>Default (Binary)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT_CLK</td>
<td>W only</td>
<td>Auto-Clear</td>
<td>X</td>
<td>Set INIT_CLK = 1 to initialize divider functions. Required as part of the startup procedure.</td>
</tr>
<tr>
<td>RELOCK</td>
<td>W only</td>
<td>Auto-Clear</td>
<td>X</td>
<td>Setting this bit to 1 will force the FemtoClock NG PLL to re-lock.</td>
</tr>
<tr>
<td>PB_CAL</td>
<td>W only</td>
<td>Auto-Clear</td>
<td>X</td>
<td>Precision Bias Calibration: Setting this bit to 1 will start the calibration of an internal precision bias current source. The bias current is used as a reference for outputs configured as LVDS and as a reference for the charge pump currents. This bit will auto-clear after the calibration is completed. Set as part of the startup procedure.</td>
</tr>
<tr>
<td>CPOL</td>
<td>R/W</td>
<td></td>
<td>0</td>
<td>SPI Read Operation SCLK Polarity: 0 = Data bits on SDAT are output at the falling edge of SCLK edge. 1 = Data bits on SDAT are output at the rising edge of SCLK edge.</td>
</tr>
</tbody>
</table>
## Electrical Characteristics

### Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 8V19N490-24 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Table 43. Absolute Maximum Ratings**

<table>
<thead>
<tr>
<th>Item</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage, ( V_{DD_V} )</td>
<td>3.6V</td>
</tr>
<tr>
<td>Inputs</td>
<td>-0.5V to ( V_{DD_V} +0.5V )</td>
</tr>
<tr>
<td>Outputs, ( V_O ) (LVCMOS)</td>
<td>-0.5V to ( V_{DD_V} +0.5V )</td>
</tr>
<tr>
<td>Outputs, ( I_O ) (LVPECL)</td>
<td></td>
</tr>
<tr>
<td>Continuous Current</td>
<td>50mA</td>
</tr>
<tr>
<td>Surge Current</td>
<td>100mA</td>
</tr>
<tr>
<td>Outputs, ( I_O ) (LVDS)</td>
<td></td>
</tr>
<tr>
<td>Continuous Current</td>
<td>50mA</td>
</tr>
<tr>
<td>Surge Current</td>
<td>100mA</td>
</tr>
<tr>
<td>Input Termination Current, ( I_{VT} )</td>
<td>( \pm35mA )</td>
</tr>
<tr>
<td>Operating Junction Temperature, ( T_J )</td>
<td>125°C</td>
</tr>
<tr>
<td>Storage Temperature, ( T_{STG} )</td>
<td>-65°C to 150°C</td>
</tr>
<tr>
<td>ESD - Human Body Mode(^([a]))</td>
<td>2000V</td>
</tr>
<tr>
<td>ESD - Charged Device Mode(^([a]))</td>
<td>500V</td>
</tr>
</tbody>
</table>

\(^([a])\) According to JEDEC JS-001-2012/JESD22-C101.
### Input Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>C\textsubscript{IN}\textsuperscript{[a]}</td>
<td>Input Capacitance</td>
<td>OSC, nOSC</td>
<td></td>
<td>2</td>
<td>4</td>
<td>pF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Other inputs</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R\textsubscript{PU}</td>
<td>Input Pull-up Resistor</td>
<td>nOSC, SDAT, nCS, nCLK_[0:3]</td>
<td></td>
<td>51</td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td>R\textsubscript{PD}</td>
<td>Input Pull-down Resistor</td>
<td>EXT_SYS, CLK_[0:3], nCLK_[0:3], OSC, nOSC, SCLK, SELSV</td>
<td></td>
<td>51</td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td>R\textsubscript{OUT}</td>
<td>LVCMOS Output Impedance</td>
<td>nINT, LOCK</td>
<td></td>
<td>25</td>
<td></td>
<td>Ω</td>
</tr>
</tbody>
</table>

[a] Guaranteed by design.

### DC Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V\textsubscript{DD_V}</td>
<td>Core Supply Voltage</td>
<td></td>
<td>3.135</td>
<td>3.3</td>
<td>3.465</td>
<td>V</td>
</tr>
<tr>
<td>I\textsubscript{DD_V}</td>
<td>Total Power Supply Current</td>
<td></td>
<td>1415</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

### 8V19N490-24 Typical Power Supply DC Current Characteristics, $V\textsubscript{DD\_V} = 3.3V ± 5\%$, $T\textsubscript{A} = -40°C to +85°C$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Supply Pin Current</th>
<th>Test Case</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>— QCLK_y</td>
<td>Style</td>
<td>LVPECL</td>
<td>LVPECL</td>
<td>LVPECL</td>
<td>LVPECL</td>
<td>LVDS</td>
<td>LVDS</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td></td>
<td>State</td>
<td>On</td>
<td>On</td>
<td>On</td>
<td>On</td>
<td>On</td>
<td>On</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Amplitude</td>
<td>500</td>
<td>750</td>
<td>1000</td>
<td>250</td>
<td>500</td>
<td>750</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>— QREF_r</td>
<td>Style</td>
<td>LVDS</td>
<td>LVDS</td>
<td>LVDS</td>
<td>LVDS</td>
<td>LVDS</td>
<td>LVDS</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td></td>
<td>State</td>
<td>On</td>
<td>On</td>
<td>Off</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Amplitude</td>
<td>500</td>
<td>500</td>
<td>—</td>
<td>250</td>
<td>—</td>
<td>—</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>I\textsubscript{DD_CA}</td>
<td>Current through VDD_QCLKA pin</td>
<td></td>
<td>89</td>
<td>102.9</td>
<td>114.9</td>
<td>74.9</td>
<td>66.1</td>
<td>87.3</td>
<td>mA</td>
</tr>
<tr>
<td>I\textsubscript{DD_CB}</td>
<td>Current through VDD_QCLKB pin</td>
<td></td>
<td>78.8</td>
<td>89.4</td>
<td>98.2</td>
<td>67.9</td>
<td>55.5</td>
<td>68.7</td>
<td>mA</td>
</tr>
<tr>
<td>I\textsubscript{DD_CC}</td>
<td>Current through VDD_QCLKC pin</td>
<td></td>
<td>79.2</td>
<td>89.9</td>
<td>98.7</td>
<td>68.2</td>
<td>55.2</td>
<td>69</td>
<td>mA</td>
</tr>
<tr>
<td>I\textsubscript{DD_CD}</td>
<td>Current through VDD_QCLKD pin</td>
<td></td>
<td>49.1</td>
<td>54.4</td>
<td>59.1</td>
<td>45.9</td>
<td>37.3</td>
<td>44.2</td>
<td>mA</td>
</tr>
<tr>
<td>I\textsubscript{DD_CE}</td>
<td>Current through VDD_QCLKE pin</td>
<td></td>
<td>69.1</td>
<td>78</td>
<td>85.6</td>
<td>60.1</td>
<td>56.9</td>
<td>70.7</td>
<td>mA</td>
</tr>
</tbody>
</table>

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July 27, 2017
Table 46. 8V19N490-24 Typical Power Supply DC Current Characteristics, $V_{DD_V} = 3.3V \pm 5\%$, $T_A = -40°C$ to $+85°C^{[a]}$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Supply Pin Current</th>
<th>Test Case</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{DD_{RA}}$</td>
<td>Current through VDD_QREFA pin</td>
<td></td>
<td>75.2</td>
<td>75.1</td>
<td>2.3</td>
<td>53.3</td>
<td>2.3</td>
<td>2.3</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{DD_{RB}}$</td>
<td>Current through VDD_QREFB pin</td>
<td></td>
<td>49.8</td>
<td>49.7</td>
<td>1.6</td>
<td>35.2</td>
<td>1.6</td>
<td>1.6</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{DD_{RC}}$</td>
<td>Current through VDD_QREFC pin</td>
<td></td>
<td>50.4</td>
<td>50.4</td>
<td>1.6</td>
<td>35.8</td>
<td>1.6</td>
<td>1.6</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{DD_{RD}}$</td>
<td>Current through VDD_QREFD pin</td>
<td></td>
<td>25.6</td>
<td>26.0</td>
<td>0.8</td>
<td>18.2</td>
<td>0.8</td>
<td>0.8</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{DD_{INP}}$</td>
<td>Current through VDD_INP pin</td>
<td></td>
<td>76.9</td>
<td>76.9</td>
<td>77.2</td>
<td>76.8</td>
<td>82.9</td>
<td>82.9</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{DD_{SPI}}$</td>
<td>Current through VDD_SPI pin</td>
<td></td>
<td>6.0</td>
<td>6.1</td>
<td>6.3</td>
<td>4.4</td>
<td>6.2</td>
<td>6.2</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{DD_{OSC}}$</td>
<td>Current through VDD_OSC and VDD_CP pins</td>
<td></td>
<td>36.7</td>
<td>36.8</td>
<td>36.7</td>
<td>38.7</td>
<td>38.1</td>
<td>38.1</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{DD_{SYNC}}$</td>
<td>Current through VDD_SYNC pin</td>
<td></td>
<td>80.6</td>
<td>80.6</td>
<td>1.9</td>
<td>80.7</td>
<td>1.9</td>
<td>1.9</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{DD_{CPF}}$</td>
<td>Current through VDD_CPF pin</td>
<td></td>
<td>56.8</td>
<td>56.9</td>
<td>56.8</td>
<td>56.8</td>
<td>56.8</td>
<td>59.3</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{DD_{LCV}}$</td>
<td>Current through VDD_LCV pin</td>
<td></td>
<td>72.9</td>
<td>72.3</td>
<td>72.2</td>
<td>73.0</td>
<td>72.3</td>
<td>72.3</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{DD_{LCF}}$</td>
<td>Current through VDD_LCF pin</td>
<td></td>
<td>54.4</td>
<td>54.4</td>
<td>54.4</td>
<td>54.4</td>
<td>59.3</td>
<td>59.3</td>
<td>mA</td>
</tr>
<tr>
<td>$P_{TOT}$</td>
<td>Total Device Power Consumption</td>
<td></td>
<td>2.72</td>
<td>2.06</td>
<td>2.03</td>
<td>2.42</td>
<td>1.97</td>
<td>2.2</td>
<td>W</td>
</tr>
<tr>
<td>$P_{TOT, SYS}$</td>
<td>Total System Power Consumption$^{[b]}$</td>
<td></td>
<td>3.14</td>
<td>3.30</td>
<td>2.54</td>
<td>2.79</td>
<td>1.97</td>
<td>2.20</td>
<td>W</td>
</tr>
</tbody>
</table>

[a] Configuration: $f_{CLK}$ (input) = 122.88MHz, $f_{SYSREF} = 7.68MHz$, internal SYSREF generation (continuous), QA[2:0] = 245.76MHz, QB[1:0] = 245.76MHz, QC[1:0] = 245.76MHz, QD = 491.52MHz, QE[1:0] = 122.88MHz. QCLK_y outputs terminated according to amplitude settings. QREF_r outputs unterminated when SYSREF is turned off.

[b] Includes total device power consumption and the power dissipated in external output termination components.

Table 47. LVCMOS DC Characteristics, $V_{DD_V} = 3.3V \pm 5\%$, $T_A = -40°C$ to $+85°C$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>Input High Voltage</td>
<td>Control Input SE LV (3.3V logic)</td>
<td>2.0</td>
<td>$V_{DD_V}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input Low Voltage</td>
<td></td>
<td>-0.3</td>
<td>0.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>Input High Current</td>
<td>Input with pull-down resistor</td>
<td>$V_{DD_V} = 3.3V, V_{IN} = 3.3V$</td>
<td>150</td>
<td>$\mu A$</td>
<td></td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Input Low Current</td>
<td></td>
<td>$V_{DD_V} = 3.3V, V_{IN} = 0V$</td>
<td>-5</td>
<td>$\mu A$</td>
<td></td>
</tr>
</tbody>
</table>

SYSREF Trigger Input EXT_SYS (1.8V/3.3V selectable logic)

| $V_{IH}$ | Input High Voltage | 1.8V logic (SELV = 0) | 1.17 | $V_{DD_V}$ | V |
| $V_{IL}$ | Input Low Voltage | 3.3V logic (SELV = 1) | 2.0  | $V_{DD_V}$ | V |
|          |                   | 1.8V logic (SELV = 0) | -0.3 | 0.63 | V |
|          |                   | 3.3V logic (SELV = 1) | -0.3 | 0.8  | V |
Table 47. LVCMOS DC Characteristics, $V_{DD_V} = 3.3\, \text{V} \pm 5\%$, $T_A = -40\, ^\circ\text{C}$ to $+85\, ^\circ\text{C}$ (Cont.)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{IH}$</td>
<td>Input High Current</td>
<td>Input with pull-down resistor</td>
<td>$V_{DD_V} = 3.3, \text{V}, V_{IN} = 1.8, \text{V}$ or $3.3, \text{V}$</td>
<td>150</td>
<td>$\mu\text{A}$</td>
<td></td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Input Low Current</td>
<td>$V_{DD_V} = 3.3, \text{V}, V_{IN} = 0, \text{V}$</td>
<td>-5</td>
<td></td>
<td></td>
<td>$\mu\text{A}$</td>
</tr>
</tbody>
</table>

SPI Inputs SDAT (when input), SCLK, nCS (1.8V/3.3V selectable logic with input hysteresis)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_I$</td>
<td>Input Voltage</td>
<td></td>
<td>-0.3</td>
<td>$V_{DD_V}$</td>
<td>$V$</td>
<td></td>
</tr>
<tr>
<td>$V_{T+}$</td>
<td>Positive-going Input Threshold Voltage</td>
<td>1.8V logic (SELSV = 0)</td>
<td>0.660</td>
<td>1.350</td>
<td>$V$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.3V logic (SELSV = 1)</td>
<td>1.8–2.1</td>
<td></td>
<td>$V$</td>
<td></td>
</tr>
<tr>
<td>$V_T$</td>
<td>Negative-going Input Threshold Voltage</td>
<td>1.8V logic (SELSV = 0)</td>
<td>0.495</td>
<td>1.170</td>
<td>$V$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.3V logic (SELSV = 1)</td>
<td>0.75–0.97</td>
<td></td>
<td>$V$</td>
<td></td>
</tr>
<tr>
<td>$V_H$</td>
<td>Hysteresis Voltage</td>
<td>$V_{T+} - V_T$</td>
<td>0.165</td>
<td>0.780</td>
<td>$V$</td>
<td></td>
</tr>
</tbody>
</table>

SPI output DAT (when output), nINT, LOCK (1.8V/3.3V selectable logic)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OH}$</td>
<td>Output High Voltage</td>
<td>1.8V logic (SELSV = 0) $I_{OH} = -4, \text{mA}$</td>
<td>1.35</td>
<td></td>
<td>$V$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.3V logic (SELSV = 1) $I_{OH} = -4, \text{mA}$</td>
<td>2.4</td>
<td></td>
<td>$V$</td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output Low Voltage</td>
<td>1.8V logic (SELSV = 0) $I_{OL} = 4, \text{mA}$</td>
<td>0.45</td>
<td></td>
<td>$V$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.3V logic (SELSV = 1) $I_{OL} = 4, \text{mA}$</td>
<td>0.4</td>
<td></td>
<td>$V$</td>
<td></td>
</tr>
</tbody>
</table>

Table 48. Differential Input DC Characteristics, $V_{DD_V} = 3.3\, \text{V} \pm 5\%$, $T_A = -40\, ^\circ\text{C}$ to $+85\, ^\circ\text{C}$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{IH}$</td>
<td>Input High Current</td>
<td>Inputs with pull-down resistor$^{[a]}$</td>
<td>$V_{DD_V} = V_{IN} = 3.465, \text{V}$</td>
<td>150</td>
<td>$\mu\text{A}$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Pull-down/pull-up inputs$^{[b]}$</td>
<td></td>
<td>150</td>
<td>$\mu\text{A}$</td>
<td></td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Input Low Current</td>
<td>Inputs with pull-down resistor</td>
<td>$V_{DD_V} = 3.465, \text{V}, V_{IN} = 0, \text{V}$</td>
<td>-150</td>
<td></td>
<td>$\mu\text{A}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Pull-down/pull-up inputs$^{[b]}$</td>
<td></td>
<td>-150</td>
<td></td>
<td>$\mu\text{A}$</td>
</tr>
</tbody>
</table>

[a] Non-Inverting inputs: CLK_n, OSC.
[b] Inverting inputs: nCLK_n, nOSC.
Table 49. LVPECL DC Characteristics (QCLK_y, QREF_r, STYLE = 1), $V_{DD_V} = 3.3V \pm 5\%$, $T_A = -40°C$ to $+85°C$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OH}$</td>
<td>Output High Voltage$^a$</td>
<td>250mV amplitude setting</td>
<td>$V_{DD_V} - 0.975$</td>
<td>$V_{DD_V} - 0.875$</td>
<td>$V_{DD_V} - 0.774$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>500mV amplitude setting</td>
<td>$V_{DD_V} - 1.000$</td>
<td>$V_{DD_V} - 0.904$</td>
<td>$V_{DD_V} - 0.805$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>750mV amplitude setting</td>
<td>$V_{DD_V} - 1.100$</td>
<td>$V_{DD_V} - 0.937$</td>
<td>$V_{DD_V} - 0.829$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1000mV amplitude setting</td>
<td>$V_{DD_V} - 1.100$</td>
<td>$V_{DD_V} - 0.962$</td>
<td>$V_{DD_V} - 0.861$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output Low Voltage</td>
<td>250mV amplitude setting</td>
<td>$V_{DD_V} - 1.250$</td>
<td>$V_{DD_V} - 1.150$</td>
<td>$V_{DD_V} - 1.040$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>500mV amplitude setting</td>
<td>$V_{DD_V} - 1.540$</td>
<td>$V_{DD_V} - 1.420$</td>
<td>$V_{DD_V} - 1.131$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>750mV amplitude setting</td>
<td>$V_{DD_V} - 1.810$</td>
<td>$V_{DD_V} - 1.690$</td>
<td>$V_{DD_V} - 1.580$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1000mV amplitude setting</td>
<td>$V_{DD_V} - 2.090$</td>
<td>$V_{DD_V} - 1.960$</td>
<td>$V_{DD_V} - 1.840$</td>
<td>V</td>
</tr>
</tbody>
</table>

$^a$ Outputs terminated with $50\Omega$ to $V_{DD_V} - 1.5V$ (250mV amplitude setting), $V_{DD_V} - 1.75V$ (500mV amplitude setting), $V_{DD_V} - 2.0V$ (750mV amplitude setting), $V_{DD_V} - 2.25V$ (1000mV amplitude setting).

Table 50. LVDS DC Characteristics (QCLK_y, QREF_r, STYLE = 0), $V_{DD_V} = 3.3V \pm 5\%$, $T_A = -40°C$ to $+85°C$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OS}$</td>
<td>Offset Voltage$^a$</td>
<td>250mV amplitude setting</td>
<td>2.10</td>
<td>2.40</td>
<td>2.70</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>500mV amplitude setting</td>
<td>1.90</td>
<td>2.23</td>
<td>2.60</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>750mV amplitude setting</td>
<td>1.80</td>
<td>2.08</td>
<td>2.4</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1000mV amplitude setting</td>
<td>1.60</td>
<td>1.93</td>
<td>2.20</td>
<td>V</td>
</tr>
<tr>
<td>$\Delta V_{OS}$</td>
<td>$V_{OS}$ Magnitude Change</td>
<td></td>
<td></td>
<td></td>
<td>80</td>
<td>mV</td>
</tr>
</tbody>
</table>

$^a$ $V_{OS}$ changes with $V_{DD_V}$. 
## AC Characteristics

### Table 51. AC Characteristics, $V_{DD-V} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$[^a] [^b]  

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{VCO}$</td>
<td>VCO Frequency</td>
<td></td>
<td>2400</td>
<td>2457.6</td>
<td>2500</td>
<td>MHz</td>
</tr>
<tr>
<td>$f_{OUT}$</td>
<td>Output Frequency</td>
<td>QCLK$_y$, QREF$_r$ (lock)</td>
<td>N = +1</td>
<td>2457.6</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>QCLK$_y$, QREF$_r$ (lock)</td>
<td>N = +2</td>
<td>1228.8</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>QCLK$_y$, QREF$_r$ (clock)</td>
<td>N = +4</td>
<td>614.4</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>QCLK$_y$, QREF$_r$ (clock)</td>
<td>N = +4</td>
<td>614.4</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>QCLK$_y$, QREF$_r$ (clock)</td>
<td>N = +5</td>
<td>491.52</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>QCLK$_y$, QREF$_r$ (clock)</td>
<td>N = +8</td>
<td>307.2</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>QCLK$_y$, QREF$_r$ (clock)</td>
<td>N = +10</td>
<td>245.76</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>QCLK$_y$, QREF$_r$ (clock)</td>
<td>N = +20</td>
<td>122.88</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td>QREF$_r$(SYSREF)</td>
<td></td>
<td>0.480</td>
<td></td>
<td>38.4</td>
<td>MHz</td>
</tr>
<tr>
<td>$f_{CLK}$</td>
<td>Input Frequency</td>
<td>CLK$_n$</td>
<td>1.92[^c]</td>
<td>245.76</td>
<td>2000</td>
<td>MHz</td>
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<tr>
<td>$f_{VCXO}$</td>
<td>VCXO Frequency</td>
<td></td>
<td>30.72</td>
<td>122.88</td>
<td></td>
<td>MHz</td>
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<tr>
<td>$\Delta f_{dp}$</td>
<td>Static Frequency Error</td>
<td>$f_{CLK} = 0$ppb frequency deviation</td>
<td></td>
<td>0</td>
<td></td>
<td>ppb</td>
</tr>
<tr>
<td>$\Delta f_{rms}$</td>
<td>Dynamic Frequency Error RMS[^d]</td>
<td>$f_{CLK} = 0$ppb frequency deviation</td>
<td></td>
<td>0.5</td>
<td></td>
<td>ppb</td>
</tr>
<tr>
<td>$V_{IN}$</td>
<td>Input Voltage Amplitude[^e]</td>
<td>CLK$_n$, OSC/nOSC</td>
<td>0.15</td>
<td>1.2</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{DIFF_{IN}}$</td>
<td>Differential Input Voltage Amplitude[^e,][^f]</td>
<td>CLK$_n$, OSC/nOSC</td>
<td>0.3</td>
<td>2.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{CMR}$</td>
<td>Common Mode Input Voltage</td>
<td>QCLK$_y$, QREF$_r$(clock)</td>
<td>1.0</td>
<td></td>
<td>$V_{DD-V} - (V_{IN} / 2)$</td>
<td>V</td>
</tr>
<tr>
<td>odc</td>
<td>Output Duty Cycle</td>
<td>QCLK$_y$, QREF$_r$(clock)</td>
<td>45</td>
<td>50</td>
<td>55</td>
<td>%</td>
</tr>
<tr>
<td>$t_R / t_F$</td>
<td>Output Rise/Fall Time, Differential</td>
<td>LVPECL, QCLK$_y$, QREF$_r$</td>
<td>20% to 80%</td>
<td>250</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVDS, QCLK$_y$, QREF$_r$</td>
<td>20% to 80%</td>
<td>250</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SYSREF, LVDS, QREF$_r$</td>
<td>20% to 80%</td>
<td>250</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVCMOS outputs</td>
<td>20% – 80%</td>
<td>1</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>
Table 51. AC Characteristics, $V_{DD-V} = 3.3\,\text{V} \pm 5\%$, $T_A = -40^\circ\text{C} \text{ to } +85^\circ\text{C}$ [a] [b] (Cont.)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{Q(PP)}$</td>
<td>LVPECL Output Voltage Swing, Peak-to-peak; (see Table 54)</td>
<td>250mV amplitude</td>
<td>2457.6MHz 491.52MHz</td>
<td>260</td>
<td>mV</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>500mV amplitude</td>
<td>2457.6MHz 491.52MHz</td>
<td>90</td>
<td>mV</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>750mV amplitude</td>
<td>2457.6MHz 491.52MHz</td>
<td>700</td>
<td>mV</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>1000mV amplitude</td>
<td>2457.6MHz 491.52MHz</td>
<td>860</td>
<td>mV</td>
<td></td>
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<tr>
<td></td>
<td>LVPECL Differential Output Voltage Swing, Peak-to-peak; 2457.6MHz; (see Table 54)</td>
<td>250mV amplitude</td>
<td>2457.6MHz 491.52MHz</td>
<td>520</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>500mV amplitude</td>
<td>2457.6MHz 491.52MHz</td>
<td>980</td>
<td>mV</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>750mV amplitude</td>
<td>2457.6MHz 491.52MHz</td>
<td>1400</td>
<td>mV</td>
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<tr>
<td></td>
<td></td>
<td>1000mV amplitude</td>
<td>2457.6MHz 491.52MHz</td>
<td>1720</td>
<td>mV</td>
<td></td>
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<tr>
<td>$V_{OD}$</td>
<td>LVDS Output Voltage Swing, Peak-to-peak; 2457.6MHz; (see Table 54)</td>
<td>250mV amplitude</td>
<td>2457.6MHz 491.52MHz</td>
<td>165</td>
<td>mV</td>
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<td></td>
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<td>500mV amplitude</td>
<td>2457.6MHz 491.52MHz</td>
<td>340</td>
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<td></td>
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<td>750mV amplitude</td>
<td>2457.6MHz 491.52MHz</td>
<td>470</td>
<td>mV</td>
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<td></td>
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<td>1000mV amplitude</td>
<td>2457.6MHz 491.52MHz</td>
<td>660</td>
<td>mV</td>
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<td></td>
<td>LVDS Differential Output Voltage Swing, Peak-to-peak; 2457.6MHz; (see Table 54)</td>
<td>250mV amplitude</td>
<td>2457.6MHz 491.52MHz</td>
<td>330</td>
<td>mV</td>
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<td></td>
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<td>500mV amplitude</td>
<td>2457.6MHz 491.52MHz</td>
<td>680</td>
<td>mV</td>
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<td></td>
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<td>750mV amplitude</td>
<td>2457.6MHz 491.52MHz</td>
<td>940</td>
<td>mV</td>
<td></td>
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<td></td>
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<td>1000mV amplitude</td>
<td>2457.6MHz 491.52MHz</td>
<td>1220</td>
<td>mV</td>
<td></td>
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<tr>
<td>$\Delta t_{PD}$</td>
<td>Propagation Delay Variation between Reference Input and any QCLK_y Output</td>
<td></td>
<td>-200</td>
<td>+200</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>Symbol</td>
<td>Parameter Description</td>
<td>Test Conditions</td>
<td>Minimum</td>
<td>Typical</td>
<td>Maximum</td>
<td>Units</td>
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<td>----------------------------------------------------------------------------------------</td>
<td>----------------------------------</td>
<td>---------</td>
<td>---------</td>
<td>---------</td>
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</tr>
<tr>
<td>tsk(o)</td>
<td>Output Skew; Note:1, 2, 3</td>
<td>QCLK_y Same N divider</td>
<td></td>
<td>100</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>QCLK_y Any N divider, incident rising edge</td>
<td></td>
<td>100</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>QREF_r (clock)</td>
<td></td>
<td>100</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>QREF_r (SYSREF)</td>
<td>100</td>
<td>150</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>QREF_r (clock) to QCLK_y</td>
<td></td>
<td>100</td>
<td>150</td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>QREF_r (SYSREF) to QCLK_y</td>
<td></td>
<td>100</td>
<td>150</td>
<td>ps</td>
</tr>
<tr>
<td>ΔΦ</td>
<td>Output Isolation between any Neighboring Clock Output</td>
<td>fOUT = 1228.8MHz</td>
<td>75</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>fOUT = 491.52MHz</td>
<td>65</td>
<td>90</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>fOUT = 245.76MHz</td>
<td>70</td>
<td>90</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>ΔΦ</td>
<td>Output Isolation between any QCLK_y, QREF_r (SYSREF) Output</td>
<td>Both SYSREF and clock signals active</td>
<td>50</td>
<td>90</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>tD, LOS</td>
<td>LOS State Detected (measured in input reference periods)</td>
<td>fCLK = 122.88MHz fCLK = 245.76MHz</td>
<td>2</td>
<td>3</td>
<td></td>
<td>TIN</td>
</tr>
<tr>
<td>tD, LOCK</td>
<td>PLL Lock Detect</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>tD, RES</td>
<td>PLL Lock Residual Time Error</td>
<td>Refer to PLL lock detect tD,LOCK Reference point: final value of clock output phase after all phase transitions settled</td>
<td></td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>ΔfHOLD</td>
<td>Holdover Accuracy</td>
<td>Maximum frequency deviation during a holdover duration of 200ms and after the clock re-validate event</td>
<td></td>
<td>±0.5</td>
<td>±5</td>
<td>ppm</td>
</tr>
</tbody>
</table>

Table 51. AC Characteristics, VDD_V = 3.3V ±5%, TA = -40°C to +85°C[8][9] (Cont.)

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Table 51. AC Characteristics, V_{DD-V} = 3.3V ±5%, T_{A} = -40°C to +85°C[a] [b] (Cont.)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_{D, RES-H}</td>
<td>Holdover Residual Error</td>
<td>Measured 50ms after the reference clock re-appeared in a holdover scenario. Reference point: final value of clock output phase after all phase transitions settled.</td>
<td>±8.138 ns</td>
<td></td>
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</tr>
<tr>
<td>t_{H}</td>
<td>Hold Time</td>
<td>EXT_SYS to CLK_n[m]</td>
<td>2.5 ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_{S}</td>
<td>Setup Time</td>
<td>EXT_SYS to CLK_n[m]</td>
<td>0 ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_{W}</td>
<td>Pulse Width</td>
<td>EXT_SYS[m]</td>
<td>4 ns</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] VCXO-PLL bandwidth = 100Hz.

[c] Minimum input frequency for the loss the input reference detector is f_{VCO}/M_{V1}(maximum).

[d] RMS frequency error, measured at any QCLK_y output, caused by Gaussian noise. Weighted with a 1ms low pass time window filter.

[e] V_{IL} should not be less than -0.3V and V_{IH} should not be greater than V_{DD-V}.

[f] Common Mode Input Voltage is defined as the cross-point voltage.

[g] LVPECL outputs terminated with 50Ω to V_{DD-V} – 1.5V (250mV amplitude setting), V_{DD-V} – 1.75V (500mV amplitude setting), V_{DD-V} – 2.0V (750mV amplitude setting), V_{DD-V} – 2.25V (1000mV amplitude setting).

[h] LVDS outputs terminated 100Ω across terminals.

[i] This parameter is defined in accordance with JEDEC standard 65.

[j] Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.

[k] Align QCLK_y to QREF_r outputs according to Recommended Delay Settings for Closest Clock-SYSREF Output Phase Alignment.

[l] SYSREF frequencies: 30.72MHz, 15.36MHz, 7.68MHz.

[m] SYSREF External trigger mode, BYPV = 0, BYPF = 1 (PLL feedback through M_{V0} and M_{V1}), P_{V0} = +1024, M_{V0} = +1024, M_{V1} = +12, N_{S} = +384, SYNC = +12, f_{IN} = 245.76MHz (see Figure 8).
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>δjit(Ø)</td>
<td>Clock RMS Phase Jitter (Random), 491.52MHz</td>
<td>Integration Range: 1kHz – 76.8MHz 75 fs Integration Range: 12kHz – 20MHz 57 fs</td>
<td>75</td>
<td></td>
<td></td>
<td>/fs</td>
</tr>
<tr>
<td>ΦN(10)</td>
<td>Clock Single-side Band Phase Noise  2457.6MHz 10Hz offset</td>
<td>10Hz offset  -58  dBC/Hz</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ΦN(100)</td>
<td></td>
<td>100Hz offset -87 dBC/Hz</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>ΦN(500)</td>
<td></td>
<td>500Hz offset from carrier -106 dBC/Hz</td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>ΦN(1k)</td>
<td></td>
<td>1kHz offset from carrier -111 dBC/Hz</td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>ΦN(10k)</td>
<td></td>
<td>10kHz offset from carrier -115 dBC/Hz</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ΦN(60k)</td>
<td></td>
<td>60kHz offset from carrier -119 dBC/Hz</td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>ΦN(100k)</td>
<td></td>
<td>1kHz offset from carrier -121 dBC/Hz</td>
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</tr>
<tr>
<td>ΦN(200k)</td>
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<td>200kHz offset from carrier -124 dBC/Hz</td>
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<tr>
<td>ΦN(800k)</td>
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<td>800kHz offset from carrier -135 dBC/Hz</td>
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<td></td>
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<td></td>
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<tr>
<td>ΦN(5M)</td>
<td></td>
<td>5MHz offset from carrier -150 dBC/Hz</td>
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<td></td>
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<tr>
<td>ΦN(≥10M)</td>
<td></td>
<td>≥10MHz offset from carrier and noise floor -151 dBC/Hz</td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>ΦN(10)</td>
<td>Clock Single-side Band Phase Noise  491.52MHz 10Hz offset</td>
<td>10Hz offset -71  dBC/Hz</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ΦN(100)</td>
<td></td>
<td>100Hz offset -102 dBC/Hz</td>
<td></td>
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<tr>
<td>ΦN(500)</td>
<td></td>
<td>500Hz offset from carrier -120 dBC/Hz</td>
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<td></td>
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<tr>
<td>ΦN(1k)</td>
<td></td>
<td>1kHz offset from carrier -126 dBC/Hz</td>
<td></td>
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<td></td>
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<tr>
<td>ΦN(10k)</td>
<td></td>
<td>10kHz offset from carrier -129 dBC/Hz</td>
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<tr>
<td>ΦN(60k)</td>
<td></td>
<td>60kHz offset from carrier -133 dBC/Hz</td>
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<tr>
<td>ΦN(100k)</td>
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<td>1kHz offset from carrier -134 dBC/Hz</td>
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</tr>
<tr>
<td>ΦN(200k)</td>
<td></td>
<td>200kHz offset from carrier -137 dBC/Hz</td>
<td></td>
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<tr>
<td>ΦN(800k)</td>
<td></td>
<td>800kHz offset from carrier -148 dBC/Hz</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ΦN(5M)</td>
<td></td>
<td>5MHz offset from carrier -156 dBC/Hz</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ΦN(≥10M)</td>
<td></td>
<td>≥10MHz offset from carrier and noise floor -157 dBC/Hz</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Symbol</td>
<td>Parameter</td>
<td>Test Conditions</td>
<td>Minimum</td>
<td>Typical</td>
<td>Maximum</td>
<td>Units</td>
</tr>
<tr>
<td>------------</td>
<td>----------------------------------</td>
<td>--------------------------</td>
<td>---------</td>
<td>---------</td>
<td>---------</td>
<td>-----------</td>
</tr>
<tr>
<td>( \Phi_N(10) )</td>
<td>Clock Single-side Band Phase Noise</td>
<td>245.76MHz 10Hz offset</td>
<td>-78</td>
<td>-59</td>
<td></td>
<td>dBc/Hz</td>
</tr>
<tr>
<td>( \Phi_N(100) )</td>
<td></td>
<td>100Hz offset</td>
<td>-107</td>
<td>-91</td>
<td></td>
<td>dBc/Hz</td>
</tr>
<tr>
<td>( \Phi_N(500) )</td>
<td></td>
<td>500Hz offset from carrier</td>
<td>-126</td>
<td>-112</td>
<td></td>
<td>dBc/Hz</td>
</tr>
<tr>
<td>( \Phi_N(1k) )</td>
<td></td>
<td>1kHz offset from carrier</td>
<td>-132</td>
<td>-118</td>
<td></td>
<td>dBc/Hz</td>
</tr>
<tr>
<td>( \Phi_N(10k) )</td>
<td></td>
<td>10kHz offset from carrier</td>
<td>-135</td>
<td>-129</td>
<td></td>
<td>dBc/Hz</td>
</tr>
<tr>
<td>( \Phi_N(60k) )</td>
<td></td>
<td>60kHz offset from carrier</td>
<td>-139</td>
<td>-129</td>
<td></td>
<td>dBc/Hz</td>
</tr>
<tr>
<td>( \Phi_N(100k) )</td>
<td></td>
<td>100kHz offset from carrier</td>
<td>-141</td>
<td>-134</td>
<td></td>
<td>dBc/Hz</td>
</tr>
<tr>
<td>( \Phi_N(200k) )</td>
<td></td>
<td>200kHz offset from carrier</td>
<td>-144</td>
<td>-135</td>
<td></td>
<td>dBc/Hz</td>
</tr>
<tr>
<td>( \Phi_N(800k) )</td>
<td></td>
<td>800kHz offset from carrier</td>
<td>-153</td>
<td>-150</td>
<td></td>
<td>dBc/Hz</td>
</tr>
<tr>
<td>( \Phi_N(5M) )</td>
<td></td>
<td>5MHz offset from carrier</td>
<td>-159</td>
<td>-153</td>
<td></td>
<td>dBc/Hz</td>
</tr>
<tr>
<td>( \Phi_N(\geq10M) )</td>
<td></td>
<td>( \geq10)MHz offset from carrier and noise floor</td>
<td>-160</td>
<td>-153</td>
<td></td>
<td>dBc/Hz</td>
</tr>
<tr>
<td>( \Phi_N(122.88MHz) )</td>
<td></td>
<td>491.52MHz 100Hz–300Hz</td>
<td>-86</td>
<td>-83</td>
<td></td>
<td>dBc</td>
</tr>
<tr>
<td></td>
<td></td>
<td>300Hz–100kHz</td>
<td>-89</td>
<td>-89</td>
<td></td>
<td>dBc</td>
</tr>
<tr>
<td></td>
<td></td>
<td>100kHz–100MHz</td>
<td>-101</td>
<td>-85</td>
<td></td>
<td>dBc</td>
</tr>
<tr>
<td></td>
<td></td>
<td>122.88MHz reference spurious</td>
<td>-80</td>
<td>-70</td>
<td></td>
<td>dBc</td>
</tr>
<tr>
<td></td>
<td></td>
<td>245.76MHz reference spurious</td>
<td>-80</td>
<td>-70</td>
<td></td>
<td>dBc</td>
</tr>
<tr>
<td>( \Phi_N(245.76MHz) )</td>
<td></td>
<td>245.76MHz 100Hz–300Hz</td>
<td>-92</td>
<td>-89</td>
<td></td>
<td>dBc</td>
</tr>
<tr>
<td></td>
<td></td>
<td>300Hz–100kHz</td>
<td>-101</td>
<td>-95</td>
<td></td>
<td>dBc</td>
</tr>
<tr>
<td></td>
<td></td>
<td>100kHz–100MHz</td>
<td>-104</td>
<td>-85</td>
<td></td>
<td>dBc</td>
</tr>
<tr>
<td></td>
<td></td>
<td>122.88MHz reference spurious</td>
<td>-80</td>
<td>-70</td>
<td></td>
<td>dBc</td>
</tr>
</tbody>
</table>

[a] Phase noise and spurious specifications apply for device operation with QREF_r outputs inactive (no SYSREF pulses generated). Phase noise specifications are applicable for all outputs active, Nx not equal.

[b] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[c] Phase noise characteristics at lower frequency offsets (10Hz-1kHz) is primarily a function of the VCXO phase noise: VCXO characteristics: \( f = 122.88\text{MHz} \); phase noise: \(-80\text{dBc/Hz (10Hz)}, -113\text{dBc/Hz (100Hz)}, -141\text{dBc/Hz (1kHz)}, -157\text{dBc/Hz (10kHz)}, -160\text{dBc/Hz (100kHz)}\).
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Φ&lt;sub&gt;N(500)&lt;/sub&gt;</td>
<td>SYSREF Single-side Band Phase Noise</td>
<td>30.72MHz 500Hz offset</td>
<td>-136</td>
<td>-130</td>
<td></td>
<td>dBC/Hz</td>
</tr>
<tr>
<td>Φ&lt;sub&gt;N(10k)&lt;/sub&gt;</td>
<td></td>
<td>10kHz offset from carrier</td>
<td>-152</td>
<td>-130</td>
<td></td>
<td>dBC/Hz</td>
</tr>
<tr>
<td>Φ&lt;sub&gt;N(60k)&lt;/sub&gt;</td>
<td></td>
<td>60kHz offset from carrier</td>
<td>-155</td>
<td>-140</td>
<td></td>
<td>dBC/Hz</td>
</tr>
<tr>
<td>Φ&lt;sub&gt;N(800k)&lt;/sub&gt;</td>
<td></td>
<td>800kHz offset from carrier</td>
<td>-156</td>
<td>-145</td>
<td></td>
<td>dBC/Hz</td>
</tr>
<tr>
<td>Φ&lt;sub&gt;N(≥3M)&lt;/sub&gt;</td>
<td></td>
<td>≥3MHz offset from carrier and noise floor</td>
<td>-157</td>
<td>-145</td>
<td></td>
<td>dBC/Hz</td>
</tr>
<tr>
<td>Φ&lt;sub&gt;N(500)&lt;/sub&gt;</td>
<td>SYSREF Single-side Band Phase Noise</td>
<td>15.36MHz 500Hz offset</td>
<td>-132</td>
<td>-130</td>
<td></td>
<td>dBC/Hz</td>
</tr>
<tr>
<td>Φ&lt;sub&gt;N(10k)&lt;/sub&gt;</td>
<td></td>
<td>10kHz offset from carrier</td>
<td>-148</td>
<td>-130</td>
<td></td>
<td>dBC/Hz</td>
</tr>
<tr>
<td>Φ&lt;sub&gt;N(60k)&lt;/sub&gt;</td>
<td></td>
<td>60kHz offset from carrier</td>
<td>-157</td>
<td>-140</td>
<td></td>
<td>dBC/Hz</td>
</tr>
<tr>
<td>Φ&lt;sub&gt;N(800k)&lt;/sub&gt;</td>
<td></td>
<td>800kHz offset from carrier</td>
<td>-160</td>
<td>-145</td>
<td></td>
<td>dBC/Hz</td>
</tr>
<tr>
<td>Φ&lt;sub&gt;N(≥3M)&lt;/sub&gt;</td>
<td></td>
<td>≥3MHz offset from carrier and noise floor</td>
<td>-160</td>
<td>-145</td>
<td></td>
<td>dBC/Hz</td>
</tr>
<tr>
<td>Φ&lt;sub&gt;N(500)&lt;/sub&gt;</td>
<td>SYSREF Single-side Band Phase Noise</td>
<td>7.68MHz 500Hz offset</td>
<td>-134</td>
<td></td>
<td></td>
<td>dBC/Hz</td>
</tr>
<tr>
<td>Φ&lt;sub&gt;N(10k)&lt;/sub&gt;</td>
<td></td>
<td>10kHz offset from carrier</td>
<td>-146</td>
<td></td>
<td></td>
<td>dBC/Hz</td>
</tr>
<tr>
<td>Φ&lt;sub&gt;N(60k)&lt;/sub&gt;</td>
<td></td>
<td>60kHz offset from carrier</td>
<td>-157</td>
<td></td>
<td></td>
<td>dBC/Hz</td>
</tr>
<tr>
<td>Φ&lt;sub&gt;N(800k)&lt;/sub&gt;</td>
<td></td>
<td>800kHz offset from carrier</td>
<td>-157</td>
<td></td>
<td></td>
<td>dBC/Hz</td>
</tr>
<tr>
<td>Φ&lt;sub&gt;N(≥3M)&lt;/sub&gt;</td>
<td></td>
<td>≥3MHz offset from carrier and noise floor</td>
<td>-157</td>
<td></td>
<td></td>
<td>dBC/Hz</td>
</tr>
<tr>
<td>Φ</td>
<td>Spurious Signals&lt;sup&gt;[c]&lt;/sup&gt;</td>
<td>30.72 MHz &gt;500Hz</td>
<td>-60</td>
<td>-56</td>
<td></td>
<td>dBC</td>
</tr>
<tr>
<td></td>
<td></td>
<td>15.36 MHz &gt;500Hz</td>
<td>-60</td>
<td>-56</td>
<td></td>
<td>dBC</td>
</tr>
<tr>
<td></td>
<td></td>
<td>7.68MHz &gt;500Hz</td>
<td>-60</td>
<td>-56</td>
<td></td>
<td>dBC</td>
</tr>
</tbody>
</table>

<sup>a</sup> Phase noise is measured as additive phase noise contribution by the device on all SYSREF outputs, dividers and channel logic. SYSREF signals measured as continued clock signal. Clock signals (QCLK) are turned on.

<sup>b</sup> Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

<sup>c</sup> Measured as sum of all spurious amplitudes in one side band in the offset frequency range above 500Hz, excluding the harmonics of the fundamental frequency of \( n \times f_{SYSREF} \) (e.g. \( n \times 7.68MHz \)).
**Figure 8. EXT_SYS Input Timing Diagram**

![Timing Diagram](image)

**Table 54. 8V19N490-24 AC Characteristics: Typical QCLK_y Output Amplitude, VDD_V = 3.3V, T_A = 85°C**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Description</th>
<th>Test Conditions</th>
<th>QCLK_y Output Frequency in MHz</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{O(PP)}</td>
<td>LVPECL Output Voltage Swing, Peak-to-peak</td>
<td>250mV amplitude setting</td>
<td>257 281 270 273 278 283</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>500mV amplitude setting</td>
<td>456 520 508 505 540 528</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>750mV amplitude setting</td>
<td>620 772 749 744 776 768</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1000mV amplitude setting</td>
<td>748 1000 968 984 1000 1016</td>
<td>mV</td>
</tr>
<tr>
<td>V_{OD}</td>
<td>LVDS Output Voltage Swing, Peak-to-peak</td>
<td>250mV amplitude setting</td>
<td>145 200 220 220 230 230</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>500mV amplitude setting</td>
<td>310 432 450 450 470 478</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>750mV amplitude setting</td>
<td>455 615 685 680 720 732</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1000mV amplitude setting</td>
<td>580 860 931 910 970 990</td>
<td>mV</td>
</tr>
</tbody>
</table>

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500fpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] LVPECL outputs terminated with 50Ω to V_{DD-V} - 1.5V (250mV amplitude setting), V_{DD-V} - 1.75V (500mV amplitude setting), V_{DD-V} - 2.0V (750mV amplitude setting), V_{DD-V} - 2.25V (1000mV amplitude setting).

[c] LVDS outputs terminated 100Ω across terminals.

**Clock Phase Noise Characteristics**

Measurement conditions for phase noise characteristics:

- VCXO characteristics: f = 122.88MHz; phase noise: -80dBc/Hz(10Hz), -113dBc/Hz(100Hz), -141dBc/Hz(1kHz), -157dBc/Hz(10kHz), -160dBc/Hz(100kHz):
- Input frequency: 245.76MHz
- I_{CPV} VCXO-PLL charge pump current: 0.2mA
- VCXO-PLL bandwidth: 6Hz
- I_{CPF} FemtoClock NG charge pump current: 1.4mA
- FemtoClock NG PLL bandwidth: 111kHz
- V_{DD-V} = 3.3V, T_A = 25°C
Figure 9. 2457.6MHz Output Phase Noise
Figure 10. 491.52MHz Output Phase Noise

Phase Noise 10.00dB/ Ref -10.00dBC/Hz

-10.00
-20.00
-30.00
-40.00
-50.00
-60.00
-70.00
-80.00
-90.00
-100.00
-110.00
-120.00
-130.00
-140.00
-150.00
-160.00
-170.00

1: 10 Hz  -71.0514 dBC/Hz
2: 100 Hz  -102.7205 dBC/Hz
3: 300 Hz  -120.4102 dBC/Hz
4: 1 kHz  -129.9167 dBC/Hz
>5: 10 kHz  -128.5589 dBC/Hz
6: 60 kHz  -133.0446 dBC/Hz
7: 100 kHz  -134.7718 dBC/Hz
8: 200 kHz  -137.8981 dBC/Hz
9: 500 kHz  -148.0063 dBC/Hz
10: 5 MHz  -156.2165 dBC/Hz

x: start 1 kHz
Stop 76.8 MHz
Center 38.4 MHz
Span 76.799 MHz

Analysis Range X: Band Marker
Analysis Range Y: Band Marker

Integ noise: -75.6240 dBC / 76.51 MHz
RMS noise: 234.033 µrad
13.4103 mdeg
RMS jitter: 75.787 fsec
Residual FM: 7.30618 kHz
Figure 11. 245.76MHz Output Phase Noise
Application Information

Power Supply Design and Recommend Application Schematics

Careful power supply and board design is required for best possible AC performance including phase noise and spurious suppression. The analog power supply pins VDD_OSC, VDD_CP, VDD_CPF, VDD_LCF and VDD_LCV require a very clean power supply isolated from the output power supply (VDD_QCLK_y and VDD_QREF_r). Output power supplies should be isolated from each other. The VDD_LCF power supply pin must be supplied by a low-noise LDO with a noise voltage of <6µV or lower. Please refer to the 8V19N490 Hardware Design Guide for information about power supply and isolation, loop filter design for VCXO and VCO, schematics, input and output interfaces/terminations and an example schematics.

Termination for QCLK_y, QREF_r LVDS Outputs (STYLE = 0)

Figure 12 shows an example termination for the QCLK_y, QREF_r LVDS outputs. In this example, the characteristic transmission line impedance is 50Ω. The termination resistor R (100Ω) is matched to the line impedance. The termination resistor must be placed at the end of the transmission line. No external termination resistor is required if R is an internal part of the receiver circuit. The LVDS termination in Figure 12 is applicable for any output amplitude setting specified in Table 15.

Figure 12. LVDS (SYLE = 0) Output Termination

![Termination for QCLK_y, QREF_r LVDS Outputs](image1)

AC Termination for QCLK_y, QREF_r LVDS Outputs (STYLE = 0)

Figure 13 and Figure 14 show AC termination examples for the QCLK_y, QREF_r LVDS outputs. In the examples, the characteristic transmission line impedance is 50Ω. In Figure 13, the termination resistor R (100Ω) is placed at the end of the transmission line. No external termination resistor is required if R is an internal part of the receiver circuit, which is shown in Figure 12. The LVDS terminations in both Figure 13 and Figure 14 are applicable for any output amplitude setting specified in Table 15. The receiver input should be re-biased according to its common mode range specifications.

Figure 13. LVDS (SYLE = 0) AC Output Termination

![AC Termination for QCLK_y, QREF_r LVDS Outputs](image2)
Termination for QCLK_y, QREF_r LVPECL Outputs (STYLE = 1)

Figure 15 shows an example termination for the QCLK_y, QREF_r LVPECL outputs. In this example, the characteristic transmission line impedance is 50Ω. The R1 (50Ω) and R2 (50Ω) resistors are matched load terminations. The output is terminated to the termination voltage \( V_T \). The \( V_T \) must be set according to the output amplitude setting defined in Table 15. The termination resistors must be placed close to the end of the transmission line.

\[
\begin{align*}
V_T &= V_{DD_V} - 1.50V \text{ (250mV Amplitude)} \\
V_T &= V_{DD_V} - 1.75V \text{ (500mV Amplitude)} \\
V_T &= V_{DD_V} - 2.00V \text{ (750mV Amplitude)} \\
V_T &= V_{DD_V} - 2.25V \text{ (1000mV Amplitude)}
\end{align*}
\]
Thermal Characteristics

The device supports applications in a natural convection environment as long as the junction temperature does not exceed the specified junction temperature $T_J$. In applications where the heat dissipates through the PCB, $\Theta_{JB}$ is the correct metric to calculate the junction temperature. $\Psi_{JB}$ is the right metric in all other applications where the majority of the heat dissipates through the board (80%) and a minority (20%) through the top of the device. The following calculation uses the junction-to-board thermal characterization parameter $\Theta_{JB}$ to calculate the junction temperature ($T_J$). Care must be taken to not exceed the maximum allowed junction temperature $T_J$ of 125 °C.

The junction temperature $T_J$ is calculated using the following equation:

$$T_J = T_B + P_{TOT} \times \Psi_{JB}$$

where:
- $T_J$ is the junction temperature at steady state conditions in °C
- $T_B$ is the board temperature at steady state condition in °C, measured on or near the component lead
- $\Psi_{JB}$ is the thermal characterization parameter to report the difference between $T_J$ and $T_B$
- $P_{TOT}$ is the total device power dissipation

The 8V19N490-24 maximum power dissipation scenario: With the maximum allowed junction temperature and the maximum device power consumption and at the max supply voltage of 3.3V + 5%, the maximum supported board temperature can be determined. In the device configuration for the maximum power consumption, $I_{DP, V}$ is 1375mA (see Table 45). In this configuration, all outputs are active and configured to LVDS, the output amplitude is set to 1000mV (QOSC: 750,V amplitude) and outputs use a 100Ω termination:

- Total system power dissipation (incl. termination resistor power): $P_{TOT} = V_{DD,V, MAX} \times I_{DD,V, MAX} = 3.465V \times 1375mA = 4.7643W$
- Total device power dissipation (excluding termination resistor power): $P_{TOT} = 4.7643W$

In this scenario and with the $\Psi_{JB}$ thermal model, the maximum supported board temperature is:

- $T_{B, MAX} = T_{J, MAX} - \Psi_{JB} \times P_{TOT}$
- $T_{B, MAX} = 125°C - 6.43°C/W \times 4.7643W$
- $T_{B, MAX} = 94.4°C$

Table 55. Thermal Characteristics for the 100 CABGA package[a]

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Thermal Parameter</th>
<th>Condition</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\Theta_{JA}$</td>
<td>Junction-to-ambient</td>
<td>0 m/s air flow</td>
<td>24.06</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 m/s air flow</td>
<td>20.89</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>2 m/s air flow</td>
<td>19.07</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3 m/s air flow</td>
<td>18.05</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>4 m/s air flow</td>
<td>17.46</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>5 m/s air flow</td>
<td>17.03</td>
<td></td>
</tr>
<tr>
<td>$\Theta_{JC}$</td>
<td>Junction-to-case</td>
<td></td>
<td>8.54</td>
<td></td>
</tr>
<tr>
<td>$\Theta_{JB}$</td>
<td>Junction-to-board[b]</td>
<td></td>
<td>6.43</td>
<td></td>
</tr>
<tr>
<td>$\Psi_{JB}$</td>
<td>Junction-to-board[c]</td>
<td></td>
<td>4.15</td>
<td></td>
</tr>
</tbody>
</table>

[a] Standard JEDEC 2S2P multilayer PCB.
[b] Thermal model where the heat dissipated in the component is conducted through the board. $T_B$ is measured on or near the component lead.
[c] Thermal model where the majority of the heat dissipates through the board and a minority through the top of the package. $T_B$ is measured on or near the component lead.
Application using the device at the maximum power dissipation must keep the board temperature below 93.9°C.

**Application power dissipation scenarios:** Applications may use device settings that result in a lower power dissipation than the maximum power scenario. The device is a multi-functional, high-speed device that targets a variety of applications. Since this device is highly programmable with a broad range of settings and configurations, the power consumption will vary as settings and configurations are changed. Table 45 shows the typical current consumption and total device power consumption along with the junction temperature for the 6 test cases shown in Table 46. The table also displays the maximum board temperature for the $\Theta_{JB}$ model.

**Table 56. Typical Device Power Dissipation and Junction Temperature**

<table>
<thead>
<tr>
<th>Test Case[a]</th>
<th>Output Configuration</th>
<th>Device</th>
<th>$\Theta_{JB}$ Thermal Model</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>$I_{DD_TOT}$</td>
<td>$P_{TOT}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>mA</td>
<td>W</td>
</tr>
<tr>
<td>1</td>
<td>QCLK: LVPECL, 500mV</td>
<td>950.4</td>
<td>2.72</td>
</tr>
<tr>
<td></td>
<td>QREF: LVDS, 500mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>QCLK: LVPECL, 750mV</td>
<td>999.7</td>
<td>2.06</td>
</tr>
<tr>
<td></td>
<td>QREF: LVDS, 500mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>QCLK: LVPECL, 1000mV</td>
<td>768.1</td>
<td>2.03</td>
</tr>
<tr>
<td></td>
<td>QREF: LVDS (off)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>QCLK: LVPECL, 250mV</td>
<td>844.2</td>
<td>2.42</td>
</tr>
<tr>
<td></td>
<td>QREF: LVDS, 250mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>QCLK: LVDS, 500mV</td>
<td>596.9</td>
<td>1.97</td>
</tr>
<tr>
<td></td>
<td>QREF: LVDS (off)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>QCLK: LVDS, 750mV</td>
<td>665.7</td>
<td>2.2</td>
</tr>
<tr>
<td></td>
<td>QREF: LVDS (off)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

[a] For device settings (see Table 46).
[b] Junction temperature at board temperature $T_B = 85°C$.
[c] Maximum board temperature for junction temperature <125°C.
Recommended Land Pattern

Figure 17. Recommended Land Pattern

NOTE:
1) All dimensions are in mm. Angles are in degrees.
2) Top down view, as view on PCB.
3) NSMD land pattern assumed.
4) Land Pattern Recommendation as per IPC-7351B.

generic requirement for surface mount design and land pattern.

RECOMMENDED LAND PATTERN

9.00

1.00

9.00

1.00

+0.35
Marking Diagram

Figure 18. Marking Diagram

1. Line 1 indicates the part number.
2. Line 2 indicates the part number suffix
3. Line 3:
   - “YYWW” is the last digit of the year and week that the part was assembled.
   - #: denotes sequential lot number.
   - $: denotes mark code.

Ordering Information

<table>
<thead>
<tr>
<th>Part/Order Number</th>
<th>Marking</th>
<th>Package</th>
<th>Shipping Packaging</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>8V19N490-24BDGI</td>
<td>IDT8V19N490-24BDGI</td>
<td>11 × 11 × 1.2 mm 100-CABGA</td>
<td>Tray</td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>8V19N490-24BDGI8</td>
<td>IDT8V19N490-24BDGI</td>
<td></td>
<td>Tape &amp; Reel</td>
<td></td>
</tr>
</tbody>
</table>

Revision History

<table>
<thead>
<tr>
<th>Revision Date</th>
<th>Description of Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>July 27, 2017</td>
<td>• Changed the definition of nBIAS_r in Table 18</td>
</tr>
<tr>
<td></td>
<td>• Updated the definition of 0x76 in Table 29</td>
</tr>
<tr>
<td></td>
<td>• Updated VDIFF_IN in Table 51</td>
</tr>
<tr>
<td></td>
<td>• Completed several minor improvements throughout the document</td>
</tr>
<tr>
<td>June 6, 2017</td>
<td>Updated the description of 0x1D–0x1F in Table 26.</td>
</tr>
<tr>
<td>April 24, 2017</td>
<td>Table 52, swapped $j_{th}(0)$ typical specs.</td>
</tr>
<tr>
<td>April 3, 2017</td>
<td>Initial release.</td>
</tr>
</tbody>
</table>
## Glossary

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Index $n$</td>
<td>Denominates a clock input CLK$_n$. Range: 0 to 3.</td>
</tr>
<tr>
<td>Index $x$</td>
<td>Denominates a channel, channel frequency divider and the associated configuration bits. Range: A, B, C, D, E.</td>
</tr>
<tr>
<td>Index $y$</td>
<td>Denominates a QCLK output and associated configuration bits. Range: A0, A1, A2, B0, B1, C0, C1, D, E0, E1.</td>
</tr>
<tr>
<td>Index $r$</td>
<td>Denominates a QREF output and associated configuration bits. Range: A0, A1, A2, B0, B1, C0, C1, D.</td>
</tr>
<tr>
<td>$V_{DD,V}$</td>
<td>Denominates voltage supply pins. Range: VDD_QCLKA, VDD_QREFA, VDD_QCLKB, VDD_QREFB, VDD_QCLKC, VDD_QREFC, VDD_QCLKD, VDD_QREFD, VDD_QCLKE, VDD_SPI, VDD_INP, VDD_LCV, VDD_LCF, VDD_CP, VDD_SYNC, VDD_CPF, VDD_OSC.</td>
</tr>
<tr>
<td>status_condition</td>
<td>Status conditions are: LOLV (Loss of VCXO-PLL lock), LOLF (Loss of FemtoClock NG-PLL lock) and LOS (Loss of input signal).</td>
</tr>
<tr>
<td>[...]</td>
<td>Index brackets describe a group associated with a logical function or a bank of outputs.</td>
</tr>
<tr>
<td>{...}</td>
<td>List of discrete values.</td>
</tr>
<tr>
<td>Suffix V</td>
<td>Denominates a function associated with the VCXO-PLL.</td>
</tr>
<tr>
<td>Suffix F</td>
<td>Denominates a function associated with the 2nd stage PLL (FemtoClock NG).</td>
</tr>
</tbody>
</table>
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Corporate Headquarters
TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information
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