FemtoClock® NG Crystal-to-HCSL Clock Generator

General Description

The IDT8V41N004I is a clock generator designed for Gigabit Ethernet, 10 Gigabit Ethernet, SGMII and PCI Express™ applications. The device generates a selectable 100MHz, 125MHz, 156.25MHz or 312.5MHz clock signal from 25MHz input. The IDT8V41N004I uses IDT’s fourth generation FemtoClock® NG technology to provide low phase noise performance, combined with excellent power supply noise rejection for optimal performance in the targeted applications. The device supports a 3.3V supply voltage and is packaged in a compact, lead-free (RoHS 6) 32-lead VFQFN package. The industrial temperature range supports high end computing, telecommunication and networking end equipment requirements.

Features

- Fourth generation FemtoClock® NG technology
- Four 100MHz, 125MHz, 156.25MHz and 312.5MHz clocks for Gigabit Ethernet, 10 Gigabit Ethernet, SGMII and PCI Express applications, HCSL interface levels
- Selectable external crystal or differential input source
- Crystal oscillator interface designed for 25MHz parallel resonant crystal
- Differential CLK, nCLK input pair accepts LVPECL, LVDS, LVHSTL, HCSL input levels
- Internal resistor bias on nCLK pin allows the user to drive CLK input with external single-ended (LVCMOS/ LVTTL) input levels
- PCI Express Gen1, Gen2, and Gen 3 compliant
- RMS phase jitter 156.25MHz (12kHz - 20MHz): 0.217ps
- Full 3.3V supply voltage
- -40°C to 85°C ambient operating temperature

Pin Assignment

32 Lead VFQFN
5mm x 5mm x 0.925mm Package Body
3.15mm x 3.15mm EPad Size
NL Package
Top View
Block Diagram

- OE_REF
- CLK_SEL
- XTAL_IN
- XTAL_OUT
- CLK
- nCLK
- IREF
- FSEL1
- FSEL0
- PLL_BYPASS
- OE0
- OE1
- OE2
- OE3
- Pulldown
- Oscillator (OSC)
- PLL
- FSEL[1:0]:
  - 00 ÷ 16
  - 01 ÷ 25
  - 10 ÷ 20
  - 11 ÷ 8
- x2
- REF_OUT
- nREF_OUT
- Q0
- nQ0
- Q1
- nQ1
- Q2
- nQ2
- Q3
- nQ3
- IREF x2
### Pin Description and Pin Characteristic Tables

**Table 1. Pin Descriptions**

<table>
<thead>
<tr>
<th>Number</th>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PLL_BYPASS</td>
<td>Input</td>
<td>Pulldown Active HIGH PLL bypass. LVCMOS/LVTTL interface levels. PLL_BYPASS = 0: PLL mode (default) PLL_BYPASS = 1: Bypass mode</td>
</tr>
<tr>
<td>2</td>
<td>OE_REF</td>
<td>Input</td>
<td>Pulldown Active HIGH output enable for REF_OUT, nREF_OUT differential output. LVCMOS/LVTTL interface levels. OE_REF = 0: Output REF_OUT disabled/high impedance (default) OE_REF = 1: Output REF_OUT enabled</td>
</tr>
<tr>
<td>3</td>
<td>OE1</td>
<td>Input</td>
<td>Pulldown Active HIGH output enable for Q1, nQ1 differential output. LVCMOS/LVTTL interface levels. OE1 = 0: Output Q1 disabled/high impedance (default) OE1 = 1: Output Q1 enabled</td>
</tr>
<tr>
<td>4</td>
<td>OE0</td>
<td>Input</td>
<td>Pulldown Active HIGH output enable for Q0, nQ0 differential output. LVCMOS/LVTTL interface levels. OE0 = 0: Output Q0 disabled/high impedance (default) OE0 = 1: Output Q0 enabled</td>
</tr>
<tr>
<td>5</td>
<td>IREF</td>
<td>Input</td>
<td>Pullup/Pulldown External fixed precision resistor (475Ω) from this pin to ground provides a reference current used for HCSL outputs.</td>
</tr>
<tr>
<td>6, 14, 22, 28, 31</td>
<td>V_DD</td>
<td>Power</td>
<td>Supply voltage pins.</td>
</tr>
<tr>
<td>7</td>
<td>CLK</td>
<td>Input</td>
<td>Pulldown Non voltage differential clock input.</td>
</tr>
<tr>
<td>8</td>
<td>nCLK</td>
<td>Input</td>
<td>Pulldown Inverting differential clock input. V_DD/2 default when left floating.</td>
</tr>
<tr>
<td>9, 10</td>
<td>REF_OUT, nREF_OUT</td>
<td>Output</td>
<td>Differential reference clock output pair. HCSL interface levels.</td>
</tr>
<tr>
<td>11</td>
<td>CLK_SEL</td>
<td>Input</td>
<td>Pulldown Active HIGH clock select input. Selects PLL input source. LVCMOS/LVTTL interface levels. CLK_SEL = 0: XTAL_IN, XTAL_OUT (default) CLK_SEL = 1: CLK, nCLK</td>
</tr>
<tr>
<td>12, 13</td>
<td>XTAL_IN, XTAL_OUT</td>
<td>Input</td>
<td>Crystal oscillator interface. XTAL_IN is the input., XTAL_OUT is the output.</td>
</tr>
<tr>
<td>15, 16</td>
<td>FSEL0, FSEL1</td>
<td>Input</td>
<td>Pulldown Output frequency select pins. LVCMOS/LVTTL interface levels. FSEL[1:0] = 00: F_OUT = 156.25MHz (default) FSEL[1:0] = 01: F_OUT = 100MHz FSEL[1:0] = 10: F_OUT = 125MHz FSEL[1:0] = 11: F_OUT = 312.5MHz</td>
</tr>
<tr>
<td>17, 18</td>
<td>nQ3, Q3</td>
<td>Output</td>
<td>Differential output pair. HCSL interface levels.</td>
</tr>
<tr>
<td>19, 25</td>
<td>GND</td>
<td>Power</td>
<td>Power supply ground.</td>
</tr>
<tr>
<td>20, 21</td>
<td>nQ2, Q2</td>
<td>Output</td>
<td>Differential output pair. HCSL interface levels.</td>
</tr>
<tr>
<td>23, 24</td>
<td>nQ1, Q1</td>
<td>Output</td>
<td>Differential output pair. HCSL interface levels.</td>
</tr>
<tr>
<td>26, 27</td>
<td>nQ0, Q0</td>
<td>Output</td>
<td>Differential output pair. HCSL interface levels.</td>
</tr>
<tr>
<td>29</td>
<td>OE3</td>
<td>Input</td>
<td>Pulldown Active HIGH output enable for Q3, nQ3 differential output. LVCMOS/LVTTL interface levels. OE3 = 0: Output Q3 disabled/high impedance (default) OE3 = 1: Output Q3 enabled</td>
</tr>
<tr>
<td>30</td>
<td>OE2</td>
<td>Input</td>
<td>Pulldown Active HIGH output enable for Q2, nQ2 differential output. LVCMOS/LVTTL interface levels. OE2 = 0: Output Q2 disabled/high impedance (default) OE2 = 1: Output Q2 enabled</td>
</tr>
<tr>
<td>32</td>
<td>V_DDA</td>
<td>Power</td>
<td>Analog supply voltage.</td>
</tr>
</tbody>
</table>

**NOTE:** Pullup and Pulldown refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.
### Table 2. Pin Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_IN</td>
<td>Input Capacitance</td>
<td></td>
<td></td>
<td>3.5</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>R_PULLUP</td>
<td>Input Pullup Resistor</td>
<td></td>
<td></td>
<td>51</td>
<td></td>
<td>KΩ</td>
</tr>
<tr>
<td>R_PULLDOWN</td>
<td>Input Pulldown Resistor</td>
<td></td>
<td></td>
<td>51</td>
<td></td>
<td>KΩ</td>
</tr>
</tbody>
</table>

### Absolute Maximum Ratings

**NOTE:** Stresses beyond those listed under **Absolute Maximum Ratings** may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the **DC Characteristics or AC Characteristics** is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

<table>
<thead>
<tr>
<th>Item</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage, $V_{DD}$</td>
<td>3.6V</td>
</tr>
<tr>
<td>Inputs, $V_I$</td>
<td></td>
</tr>
<tr>
<td>XTAL_IN</td>
<td>0V to 2V</td>
</tr>
<tr>
<td>Other Inputs</td>
<td>-0.5V to $V_{DD} + 0.5V$</td>
</tr>
<tr>
<td>Outputs, $V_O$</td>
<td>-0.5V to $V_{DD} + 0.5V$</td>
</tr>
<tr>
<td>Package Thermal Impedance, $\theta_{JA}$</td>
<td>33.1°C/W (0 mps)</td>
</tr>
<tr>
<td>Storage Temperature, $T_{STG}$</td>
<td>-65°C to 150°C</td>
</tr>
</tbody>
</table>

### DC Electrical Characteristics

**Table 3A. Power Supply DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40°C$ to 85°C**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$</td>
<td>Core Supply Voltage</td>
<td></td>
<td>3.135</td>
<td>3.3</td>
<td>3.465</td>
<td>V</td>
</tr>
<tr>
<td>$V_{DDA}$</td>
<td>Analog Supply Voltage</td>
<td></td>
<td>$V_{DD} - 0.155$</td>
<td>3.3</td>
<td>$V_{DD}$</td>
<td>V</td>
</tr>
<tr>
<td>$I_{DD}$</td>
<td>Power Supply Current</td>
<td>Outputs Disabled</td>
<td></td>
<td>121</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{DDA}$</td>
<td>Analog Supply Current</td>
<td></td>
<td></td>
<td>31</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

**NOTE 1:** This device requires that $V_{DD}$ and $V_{DDA}$ are powered simultaneously. See **Power Supply Sequence Requirement** application note.
### Table 3B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>Input High Voltage</td>
<td>$V_{DD} = V_{IN} = 3.465V$</td>
<td>$150\mu A$</td>
<td>$150\mu A$</td>
<td>$150\mu A$</td>
<td>$150\mu A$</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input Low Voltage</td>
<td>$V_{DD} = V_{IN} = 3.465V$</td>
<td>$0.8V$</td>
<td>$0.8V$</td>
<td>$0.8V$</td>
<td>$0.8V$</td>
</tr>
</tbody>
</table>

### Table 3C. Differential DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{IH}$</td>
<td>Input High Current</td>
<td>$V_{DD} = V_{IN} = 3.465V$</td>
<td>$150\mu A$</td>
<td>$150\mu A$</td>
<td>$150\mu A$</td>
<td>$150\mu A$</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Input Low Current</td>
<td>$V_{DD} = V_{IN} = 3.465V$</td>
<td>$-5\mu A$</td>
<td>$-5\mu A$</td>
<td>$-5\mu A$</td>
<td>$-5\mu A$</td>
</tr>
<tr>
<td>$V_{PP}$</td>
<td>Peak-to-Peak Input Voltage</td>
<td>$V_{DD} = V_{IN} = 3.465V$</td>
<td>$1.3V$</td>
<td>$1.3V$</td>
<td>$1.3V$</td>
<td>$1.3V$</td>
</tr>
<tr>
<td>$V_{CMR}$</td>
<td>Common Mode Input Voltage; NOTE 1</td>
<td>$V_{DD} = V_{IN} = 3.465V$</td>
<td>$V_{DD} - 0.85V$</td>
<td>$V_{DD} - 0.85V$</td>
<td>$V_{DD} - 0.85V$</td>
<td>$V_{DD} - 0.85V$</td>
</tr>
</tbody>
</table>

NOTE 1: Common mode voltage is defined as the crosspoint.

### Table 4. Crystal Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mode of Oscillation</td>
<td>Fundamental</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Frequency</td>
<td>$25MHz$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Load Capacitance ($C_L$)</td>
<td>$12pF$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Equivalent Series Resistance (ESR)</td>
<td>$50\Omega$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Shunt Capacitance</td>
<td>$7pF$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTE: Characterized using a 12pF parallel resonant crystal.

### Table 5. Input Frequency Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{IN}$</td>
<td>Input Frequency</td>
<td>XTAL_IN, XTAL_OUT</td>
<td>$25MHz$</td>
<td>$25MHz$</td>
<td>$25MHz$</td>
<td>$25MHz$</td>
</tr>
<tr>
<td>$f_{IN,DC}$</td>
<td>Input Duty Cycle</td>
<td>CLK, nCLK</td>
<td>$45%$</td>
<td>$55%$</td>
<td>$55%$</td>
<td>$55%$</td>
</tr>
</tbody>
</table>
### AC Electrical Characteristics

**Table 6A. PCI Express Jitter Specifications, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>PCIe Industry Specification</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_j</td>
<td>Phase Jitter Peak-to-Peak; NOTE 1, 4</td>
<td>$f = 100MHz$, 25MHz Crystal Input Evaluation Band: 0Hz - Nyquist (clock frequency/2)</td>
<td>11</td>
<td>18</td>
<td>86</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>$t_{REFCLK_{HF,RMS}}$ (PCIe Gen 2)</td>
<td>Phase Jitter RMS; NOTE 2, 4</td>
<td>$f = 100MHz$, 25MHz Crystal Input High Band: 1.5MHz - Nyquist (clock frequency/2)</td>
<td>1.0</td>
<td>1.6</td>
<td>3.10</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>$t_{REFCLK_{LF,RMS}}$ (PCIe Gen 2)</td>
<td>Phase Jitter RMS; NOTE 2, 4</td>
<td>$f = 100MHz$, 25MHz Crystal Input Low Band: 10kHz - 1.5MHz</td>
<td>0.24</td>
<td>1.1</td>
<td>3.0</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>$t_{REFCLK_{RMS}}$ (PCIe Gen 3)</td>
<td>Phase Jitter RMS; NOTE 3, 4</td>
<td>$f = 100MHz$, 25MHz Crystal Input Evaluation Band: 0Hz - Nyquist (clock frequency/2)</td>
<td>0.24</td>
<td>0.41</td>
<td>0.8</td>
<td></td>
<td>ps</td>
</tr>
</tbody>
</table>

**NOTE:** Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions. For additional information, refer to the *PCI Express Application Note section* in the datasheet.

**NOTE 1:** Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1 is 86ps peak-to-peak for a sample size of $10^5$ clock periods.

**NOTE 2:** RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps RMS for $t_{REFCLK_{HF,RMS}}$ (High Band) and 3.0ps RMS for $t_{REFCLK_{LF,RMS}}$ (Low Band).

**NOTE 3:** RMS jitter after applying system transfer function for the common clock architecture. This specification is based on the *PCI Express Base Specification Revision 0.7, October 2009* and is subject to change pending the final release version of the specification.

**NOTE 4:** This parameter is guaranteed by characterization. Not tested in production.
Table 6B. AC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40°C$ to 85°C

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{OUT}$ Output Frequency</td>
<td>Q[0:3], nQ[0:3] FSEL[1:0] = 00</td>
<td>156.25 MHz</td>
<td>156.25</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Q[0:3], nQ[0:3] FSEL[1:0] = 01</td>
<td>100 MHz</td>
<td>100</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Q[0:3], nQ[0:3] FSEL[1:0] = 10</td>
<td>125 MHz</td>
<td>125</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Q[0:3], nQ[0:3] FSEL[1:0] = 11</td>
<td>312.5 MHz</td>
<td>312.5</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>REF_OUT XTAL, CLK, nCLK = 25MHz</td>
<td>25 MHz</td>
<td>25</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\Phi_N(100)$ Single-Side Band Noise Power, 100Hz from Carrier</td>
<td>25MHz Crystal Input, $f_{OUT} = 156.25MHz$</td>
<td>-85 dBc/Hz</td>
<td>-85 dBc/Hz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\Phi_N(1k)$ Single-Side Band Noise Power, 1kHz from Carrier</td>
<td>25MHz Crystal Input, $f_{OUT} = 156.25MHz$</td>
<td>-118 dBc/Hz</td>
<td>-118 dBc/Hz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\Phi_N(10k)$ Single-Side Band Noise Power, 10kHz from Carrier</td>
<td>25MHz Crystal Input, $f_{OUT} = 156.25MHz$</td>
<td>-133 dBc/Hz</td>
<td>-133 dBc/Hz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\Phi_N(100k)$ Single-Side Band Noise Power, 100kHz from Carrier</td>
<td>25MHz Crystal Input, $f_{OUT} = 156.25MHz$</td>
<td>-138 dBc/Hz</td>
<td>-138 dBc/Hz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\Phi_N(1M)$ Single-Side Band Noise Power, 1MHz from Carrier</td>
<td>25MHz Crystal Input, $f_{OUT} = 156.25MHz$</td>
<td>-143 dBc/Hz</td>
<td>-143 dBc/Hz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\Phi_N(10M)$ Single-Side Band Noise Power, 10MHz from Carrier</td>
<td>25MHz Crystal Input, $f_{OUT} = 156.25MHz$</td>
<td>-156 dBc/Hz</td>
<td>-156 dBc/Hz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{jit(\Omega)}$ RMS Phase Jitter (Random); NOTE 1, 2</td>
<td>100MHz, Integration Range (12kHz to 20MHz)</td>
<td>0.219 ps</td>
<td></td>
<td>ps</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>125MHz, Integration Range: 12kHz – 20MHz</td>
<td>0.205 ps</td>
<td></td>
<td>ps</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>156.25MHz, Integration Range: 12kHz – 20MHz</td>
<td>0.217 ps</td>
<td></td>
<td>ps</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>312.5MHz, Integration Range: 12kHz – 20MHz</td>
<td>0.215 ps</td>
<td></td>
<td>ps</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{REF_OUT,RMS}$ Phase Jitter RMS; NOTE 1</td>
<td>25MHz crystal input Integration Range: 12kHz - 5MHz</td>
<td>0.268 ps</td>
<td></td>
<td>ps</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{sk(o)}$ Output Skew; NOTE 3, 4</td>
<td>Q[0:3], nQ[0:3]</td>
<td>100 ps</td>
<td></td>
<td>ps</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\delta_{jit(cc)}$ Cycle-to-Cycle Jitter; NOTE 3</td>
<td>PLL Mode</td>
<td>12 ps</td>
<td></td>
<td>ps</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\delta_{jit(per)}$ Period Jitter, RMS; NOTE 3</td>
<td>PLL Mode</td>
<td>3.8 ps</td>
<td></td>
<td>ps</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_L$ PLL Lock Time</td>
<td></td>
<td>30 ms</td>
<td></td>
<td>ms</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{MAX}$ Absolute Max. Output Voltage; NOTE 5, 6</td>
<td></td>
<td>1150 mV</td>
<td></td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{MIN}$ Absolute Min. Output Voltage; NOTE 5, 7</td>
<td></td>
<td>-300 mV</td>
<td></td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{RB}$ Ringback Voltage; NOTE 8, 9</td>
<td></td>
<td>-100 mV</td>
<td></td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{STABLE}$ Time before $V_{RB}$ is Allowed; NOTE 8, 9</td>
<td></td>
<td>500 ps</td>
<td></td>
<td>ps</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Refer to Phase Noise Plot section.
NOTE 2: REF_OUT, nREF_OUT is disabled.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 5: Measurement taken from a single ended waveform.
NOTE 6: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.
NOTE 7: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.
NOTE 8: Measurement taken from a differential waveform.
NOTE 9: TSTABLE is the time the differential clock must maintain a minimum ±150mV differential voltage after rising/falling edges before it is allowed to drop back into the VRB ±100 mV differential range.
NOTE 10: Measured at crossing point where the instantaneous voltage value of the rising edge of Qx+ equals the falling edge of Qx-.
NOTE 11: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
NOTE 12: Defined as the total variation of all crossing voltages of rising Qx+ and falling Qx-. This is the maximum allowed variance in Vcross for any particular system. See Parameter Measurement Information Section.
NOTE 13: Measured from -150mV to +150mV on the differential waveform (derived from Q minus nQ). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.
Typical Phase Noise at 156.25MHz

Phase Noise 10.00dB/Ref -20.00dBc/Hz [Smo]

-20.00 dBm

Offset Frequency (Hz)

Noise Power (dBc/Hz)

10 kHz 100 kHz 1 MHz 10 MHz

-180.0

-160.0

-140.0

-120.0

-100.0

-90.0

-80.0

-70.0

-60.0

-50.0

-40.0

-30.0

-20.0

-10.0

0.0

10.0

Noise Power (dBc/Hz)

Offset Frequency (Hz)

Typical Phase Noise at 156.25MHz

Center 156,249589 MHz

Noise X: Start 12 kHz

Stop 20 MHz

Center 10.006 MHz

Span 19.983 MHz

Value

RMS Noise: 213.156 μrad

RMS Jitter: 217.119 fsec

Residual FM: 1.13009 kHz

Analysis Range X: Band Marker

Analysis Range Y: Band Marker

Intg Noise: -76.4364 dBc / 19.69 MHz
Typical Phase Noise at 25MHz (REF_OUT, nREF_OUT)

Carrier 25.0000006 MHz, -0.3817 dBc

-20.00 dBc/Hz
-30.00 dBc/Hz
-40.00 dBc/Hz
-50.00 dBc/Hz
-60.00 dBc/Hz
-70.00 dBc/Hz
-80.00 dBc/Hz
-90.00 dBc/Hz
-100.00 dBc/Hz
-110.00 dBc/Hz
-120.00 dBc/Hz
-130.00 dBc/Hz
-140.00 dBc/Hz
-150.00 dBc/Hz
-160.00 dBc/Hz
-170.00 dBc/Hz

Offset Frequency (HZ)

10 100 1k 10k 100k 1M

Noise Power (dBc/Hz)

-20.00 dBc/Hz
-30.00 dBc/Hz
-40.00 dBc/Hz
-50.00 dBc/Hz
-60.00 dBc/Hz
-70.00 dBc/Hz
-80.00 dBc/Hz
-90.00 dBc/Hz
-100.00 dBc/Hz
-110.00 dBc/Hz
-120.00 dBc/Hz
-130.00 dBc/Hz
-140.00 dBc/Hz
-150.00 dBc/Hz
-160.00 dBc/Hz
-170.00 dBc/Hz

Typical Phase Noise at 25MHz (REF_OUT, nREF_OUT)
Parameter Measurement Information

3.3V HCSL Output Load Test Circuit 1

This load condition is used for $V_{MAX}$, $V_{MIN}$, $V_{RB}$, $t_{STABLE}$, $V_{CROSS}$, $\Delta V_{CROSS}$, and $t_{SLEW_a}$ measurements.

3.3V HCSL Output Load Test Circuit 2

This load condition is used for tjit(cc), tjit(per), tjit(Ø), tREF_OUT_RMS, $\phi_N$, tsk(o), and odc measurements.

Differential Input Level

Cycle-to-Cycle Jitter

Period Jitter

Output Skew
Parameter Measurement Information, continued

RMS Phase Jitter

\[
\text{RMS Phase Jitter} = \frac{1}{\sqrt{2\pi f}} \sqrt{\text{Area Under Curve Defined by the Offset Frequency Markers}}
\]

PLL Lock Time

Differential Measurement Points for Duty Cycle/Period

Single-ended Measurement Points for Absolute Cross Point and Swing

Differential Measurement Points for Rise/Fall Edge Rate
Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Inputs
For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

Crystal Inputs
For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

LVCMOS Control Pins
All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

Differential Outputs
All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Wiring the Differential Input to Accept Single-Ended Levels

*Figure 1* shows how a differential input can be wired to accept single ended levels. The reference voltage \( V_1 = V_{DD}/2 \) is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the \( V_1 \) in the center of the input voltage swing. For example, if the input clock swing is 2.5V and \( V_{DD} = 3.3V \), R1 and R2 value should be adjusted to set \( V_1 \) at 1.25V. The values below are for when both the single ended swing and \( V_{DD} \) are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however \( V_{IL} \) cannot be less than -0.3V and \( V_{IH} \) cannot be more than \( V_{DD} + 0.3V \). Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

![Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels](image)
Differential Clock Input Interface

The CLK / nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both signals must meet the $V_{PP}$ and $V_{CMR}$ input requirements. Figures 2A to 2E show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

**Figure 2A.** CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

**Figure 2B.** CLK/nCLK Input Driven by a 3.3V LVPECL Driver

**Figure 2C.** CLK/nCLK Input Driven by a 3.3V LVPECL Driver

**Figure 2D.** CLK/nCLK Input Driven by a 3.3V LVDS Driver

**Figure 2E.** CLK/nCLK Input Driven by a 3.3V HCSL Driver
Power Supply Sequence Requirement

The IDT8V41N004I has a power supply sequence requirement. This device requires that \( V_{DD} \) and \( V_{DDA} \) are powered simultaneously. This device has been characterized using the recommended power supply filtering techniques in Figure 4.

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. Figure 3A shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (\( R_o \)) and the series resistance (\( R_s \)) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, \( R_1 \) and \( R_2 \) in parallel should equal the transmission line impedance. For most 50\( \Omega \) applications, \( R_1 \) and \( R_2 \) can be 100\( \Omega \). This can also be accomplished by removing \( R_1 \) and changing \( R_2 \) to 50\( \Omega \). The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. Figure 3B shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

![Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface](image)

![Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface](image)
Schematic Example

*Figure 4 (next page)* shows an example of an IDT8V41N004I application schematic. The schematic example focuses on functional connections and is intended as an example only. It may not represent the exact user configuration. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set. For example, OE[3:0] and FSEL[1:0] can be configured from an FPGA instead of set with pull up and pull down resistors as shown.

For this device, the crystal load capacitors are required for proper operation. A 12pF parallel resonant 25MHz crystal is used. The load capacitance C1 = C2 = 1pF is recommended for frequency accuracy. Depending on the parasitic of the printed circuit board layout, these values might require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used, but this will require adjusting C1 and C2.

The schematic example shows two different HCSL output terminations; the standard termination when the HCSL receiver is on the same PCB as the IDT8V41N004I as well as the termination for a PCIe add-in card.

As with any high speed analog circuitry, the power supply pins are vulnerable to noise. To achieve optimum jitter performance, power supply isolation is required. The IDT8V41N004I provides separate power supply pins to isolate noise from coupling into the internal PLL. In order to achieve the best possible filtering, it is highly recommended that the 0.1uF capacitors at the output of the LC filter be placed on the IDT8V41N004I side of the PCB as close to the corresponding power pin as possible. This is represented by the placement of these capacitors in the schematic.

Do not share ground vias; use at least one ground via per 0.1uF cap or crystal load cap. If space is limited, the ferrite beads, 10uf capacitors and the 0.1uF capacitors connected directly to 3.3V can be placed on the opposite side of the PCB. If space permits, place all filter components on the device side of the board.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.
Place each 0.1uF bypass cap directly adjacent to its corresponding VDD or VDDA pin.

Note:
PLL_BYPASS, OE_REF, OE[3:0] and FSEL[1:0] are internally pulled down so no external components are required to select the defaults.
If external pull-up/down needed, see "Logic Control Input Examples" shown at left.

Figure 4. IDT8V41N004I Schematic Layout
PCI Express Application Note

PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used Common Clock Architecture in which a copy of the reference clock is provided to both ends of the PCI Express Link.

In the jitter analysis, the transmit (Tx) and receive (Rx) serdes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

\[ H_t(s) = H_3(s) \times [H_1(s) - H_2(s)] \]

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

\[ Y(s) = X(s) \times H_3(s) \times [H_1(s) - H_2(s)] \]

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on \(X(s) H_3(s) \times [H_1(s) - H_2(s)]\).

PCI Express Common Clock Architecture

For PCI Express Gen 1, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g. for a 100MHz reference clock: 0Hz – 50MHz) and the jitter result is reported in peak-peak.

For PCI Express Gen 2, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in rms. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the individual transfer functions as well as the overall transfer function \(H_t\).

For PCI Express Gen 3, one transfer function is defined and the evaluation is performed over the entire spectrum. The transfer function parameters are different from Gen 1 and the jitter result is reported in RMS.

For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note PCI Express Reference Clock Requirements.
VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in Figure 5. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

Figure 5. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)
Recommended Termination

*Figure 6A* is the recommended source termination for applications where the driver and receiver will be on separate PCBs. This termination is the standard for PCI Express™ and HCSL output types. All traces should be 50Ω impedance single-ended or 100Ω differential.

![Figure 6A. Recommended Source Termination (where the driver and receiver will be on separate PCBs)](image)

*Figure 6B* is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will be minimized. In addition, a series resistor (Rs) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single-ended or 100Ω differential.

![Figure 6B. Recommended Termination (where a point-to-point connection can be used)](image)
Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8V41N004I. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT8V41N004I is the sum of the core power plus analog power plus the power dissipation at the outputs. The following is the power dissipation for $V_{DD} = 3.3V + 5\% = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipation at the outputs.

- Power (core)$_{\text{MAX}} = V_{DD_{\text{MAX}}} \times (I_{\text{D_MAX}} + I_{\text{DDA_{MAX}}}) = 3.465V \times (121mA + 31mA) = 526.7mW$

- Power (outputs)$_{\text{MAX}} = 44.5mW/\text{Loaded Output pair}$

If all outputs are loaded, the total power is $5 \times 44.5mW = 222.5mW$

Total Power$_{\text{MAX}} = (3.465V, \text{if all outputs are loaded}) = 526.7mW + 222.5mW = 749.2mW$

2. Junction Temperature.

Junction temperature, $T_j$, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, $T_j$, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for $T_j$ is as follows: $T_j = \theta_{JA} \times P_d_{\text{total}} + T_A$

$\theta_{JA} = \text{Junction-to-Ambient Thermal Resistance}$

$P_d_{\text{total}} = \text{Total Device Power Dissipation}$ (example calculation is in section 1 above)$

$T_A = \text{Ambient Temperature}$

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming no air flow and a multi-layer board, the appropriate value is 33.1°C/W per Table 7 below.

Therefore, $T_j$ for an ambient temperature of 85°C with all outputs switching is:

$85°C + 0.749W \times 33.1°C/W = 109.8°C$. This is below the limit of 125°C.

This calculation is only an example. $T_j$ will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance $\theta_{JA}$ for 32 Lead VFQFN, Forced Convection

<table>
<thead>
<tr>
<th>Meters per Second</th>
<th>0</th>
<th>1</th>
<th>3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multi-Layer PCB, JEDEC Standard Test Boards</td>
<td>33.1°C/W</td>
<td>28.1°C/W</td>
<td>25.4°C/W</td>
</tr>
</tbody>
</table>
3. Calculations and Equations.

The purpose of this section is to calculate power dissipation on the IC per HCSL output pairs.

HCSL output driver circuit and termination are shown in Figure 7.

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs at \( V_{DD_{MAX}} \).

\[
\text{Power} = (V_{DD_{MAX}} - V_{OUT}) \times I_{OUT}
\]

since \( V_{OUT} = I_{OUT} \times R_L \)

\[
\text{Power} = (V_{DD_{MAX}} - I_{OUT} \times R_L) \times I_{OUT}
\]

\[
= (3.465V - 17mA \times 50\Omega) \times 17mA
\]

Total Power Dissipation per output pair = 44.5mW
Reliability Information

Table 7. $\theta_{JA}$ vs. Air Flow Table for a 32 Lead VFQFN

<table>
<thead>
<tr>
<th>Meters per Second</th>
<th>0</th>
<th>1</th>
<th>3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multi-Layer PCB, JEDEC Standard Test Boards</td>
<td>33.1°C/W</td>
<td>28.1°C/W</td>
<td>25.4°C/W</td>
</tr>
</tbody>
</table>

Transistor Count

The transistor count for IDT8V41N004I is: 24,809
32 Lead VFQFN Package Outline and Package Dimensions
## Ordering Information

**Table 8. Ordering Information**

<table>
<thead>
<tr>
<th>Part/Order Number</th>
<th>Marking</th>
<th>Package</th>
<th>Shipping Packaging</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>8V41N004NLGI</td>
<td>IDT8V41N004NLGI</td>
<td>“Lead-Free” 32 Lead VFQFN</td>
<td>Tray</td>
<td>-40°C to 85°C</td>
</tr>
<tr>
<td>8V41N004NLGI8</td>
<td>IDT8V41N004NLGI</td>
<td>“Lead-Free” 32 Lead VFQFN</td>
<td>Tape &amp; Reel</td>
<td>-40°C to 85°C</td>
</tr>
</tbody>
</table>
Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.

2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.

3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.

4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.

5. Renesas Electronics products are classified according to the following two quality grades. "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.

   *Standard*: Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

   *High Quality*: Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implants; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.

6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.

7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.

8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.

9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.

10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.

11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.

12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:

www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.