General Description

The IDT8V44N003I is a programmable LVDS synthesizer designed for applications requiring frequency conversion from a differential or single-end reference source. The device is designed to provide optimum performance of low phase noise and high power supply noise rejection over a wide range of output frequencies. Oscillator level phase noise performance is achieved through the use of IDT's Fourth Generation FemtoClock®NG PLL technology. Default output frequency settings are factory programmable via a one time programmable ROM while the I²C interface can be used to program the output frequency after power up. A buffered copy of the input reference clock is provided at both LVDS output levels for applications requiring efficient board space utilization.

Features

- Fourth generation FemtoClock® (NG) technology
- Reference clock input accepts differential HCSL, LVDS, LVPECL or single-ended sine wave or LVCMOS input levels
- Input frequency range of 20MHz to 500MHz
- Output frequency range of 50MHz to 1.2GHz
- Buffered copy of input reference clock at LVDS output levels
- PLL lock indicator
- Full 3.3V output supply mode
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Pin Assignment

- VDDA
- nc
- VDD
- nc
- SDATA
- GND
- nc
- SCLK
- nc
- Reserved
- VPP
- nc
- nVDD
- nc
- nGND
- nc
- nc
- nc
- nc
- Lock
- REF_CLKIN
- nREF_CLKIN
- REF_CLKOUT
- nREF_CLKOUT
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Table 1. Pin Descriptions

<table>
<thead>
<tr>
<th>Number</th>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1, 4, 5, 7, 9, 11, 17, 19, 22, 24, 26, 28, 31</td>
<td>nc</td>
<td>Unused</td>
<td>These pins are to be left unconnected.</td>
</tr>
<tr>
<td>2</td>
<td>Reserved</td>
<td>Reserve</td>
<td>Reserved pin. This pin is left unconnected.</td>
</tr>
<tr>
<td>3</td>
<td>VPP</td>
<td>Input</td>
<td>Pullup</td>
</tr>
<tr>
<td>6, 8, 10, 18, 30</td>
<td>GND</td>
<td>Power</td>
<td>Power supply ground.</td>
</tr>
<tr>
<td>12</td>
<td>nREF_CLKIN</td>
<td>Input</td>
<td>Pulldown/Pullup</td>
</tr>
<tr>
<td>13</td>
<td>REF_CLKIN</td>
<td>Input</td>
<td>Pulldown</td>
</tr>
<tr>
<td>14</td>
<td>LOCK</td>
<td>Output</td>
<td>PLL lock indicator. LVCMOS/LVTTL interface levels.</td>
</tr>
<tr>
<td>15, 16</td>
<td>nREF_CLKOUT, REF_CLKOUT</td>
<td>Output</td>
<td>Differential output pair. Buffered copy of REF_CLKIN. LVDS interface levels.</td>
</tr>
<tr>
<td>20, 21</td>
<td>nQ, Q</td>
<td>Output</td>
<td>Differential output pair. LVDS interface levels.</td>
</tr>
<tr>
<td>23, 27</td>
<td>VDD</td>
<td>Power</td>
<td>Power supply pins.</td>
</tr>
<tr>
<td>25</td>
<td>VDDA</td>
<td>Power</td>
<td>Analog power supply pin.</td>
</tr>
<tr>
<td>32</td>
<td>SCLK</td>
<td>Input</td>
<td>Pullup</td>
</tr>
</tbody>
</table>

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_IN</td>
<td>Input Capacitance</td>
<td></td>
<td>3.5</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>R_PULLUP</td>
<td>Input Pullup Resistor</td>
<td></td>
<td>51</td>
<td></td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td>R_PULLDOWN</td>
<td>Input Pulldown Resistor</td>
<td></td>
<td>51</td>
<td></td>
<td></td>
<td>kΩ</td>
</tr>
</tbody>
</table>
Block Diagram with Programming Registers

- **REF_CLKIN** Pulldown
- **nREF_CLKIN** PU/PD
- **±P**
- **PFD & LPF**
- **PFD & LPF**
- **FemtoClock™ NG VCO 1980-2550MHz**
- **Feedback Divider M (25 Bits)**
  - MINT (7 bits)
  - MFRAC (18 bits)
- **MINT**
- **MFRAC**
- **Feedback Divider M (25 Bits)**
  - P0 MINT0 MFRAC0 N0
  - P1 MINT1 MFRAC1 N1
  - P2 MINT2 MFRAC2 N2
  - P3 MINT3 MFRAC3 N3
- **I2C Control**
- **±N**
- **LOCK**
- **REF_CLKOUT**
- **nREF_CLKOUT**
- **Q**
- **nQ**
- **SCLK** Pullup
- **SDATA** Pullup
- **VPP**

**I2C:**
- 3 bits
- 7 bits
- 18 bits
- 7 bits

**Def:**
- 3 bits
- 7 bits
- 18 bits
- 7 bits
## Register Settings

### Table 3A. I²C Register Map

<table>
<thead>
<tr>
<th>Register</th>
<th>Binary Register Address</th>
<th>Register Bit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>D7 D6 D5 D4 D3 D2 D1 D0</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>10000</td>
<td>reserved reserved reserved reserved reserved reserved reserved reserved</td>
</tr>
<tr>
<td>17</td>
<td>10001</td>
<td>reserved reserved reserved reserved reserved reserved reserved reserved</td>
</tr>
<tr>
<td>18</td>
<td>10010</td>
<td>reserved reserved nPLL_BYPASS FSEL[1] reserved FSEL[0] reserved reserved reserved reserved</td>
</tr>
<tr>
<td>19</td>
<td>10011</td>
<td>reserved reserved reserved reserved reserved reserved reserved reserved reserved</td>
</tr>
</tbody>
</table>
### Table 3B. I2C Register Function Descriptions

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>MINTn[6:0]</td>
<td>Integer Feedback Divider Register n (n = 0...3)</td>
<td>Sets the integer portion of the feedback divider value. Can be set to a value of 4 to 127. For binary values &lt; 4, the value is x+4. So programming 0000000 would yield a feedback divider of ÷4, 0000001 = ÷5, etc. It should also be noted that with a reference of 100MHz and P=1, the minimum value loaded into this register should be 20 to remain above the minimum VCO frequency of 1980MHz.</td>
</tr>
<tr>
<td>MFRACn[17:0]</td>
<td>Fractional Feedback Divider Register n (n = 0...3)</td>
<td>Sets the fractional value of the feedback divider resulting in a fraction of MFRAC0[17:0]÷2^18. From a 100MHz reference, this means the frequency is incrimented by about 381Hz÷5 for each LSB increment.</td>
</tr>
<tr>
<td>Nn[6:0]</td>
<td>Output Divider Register n (n = 0...3)</td>
<td>Sets the output divider. The output divider value can range from 2, 3, 4, 5, 6 and 8, 10, 12 to 126 (step: 2). See Table 3D for the output divider coding.</td>
</tr>
<tr>
<td>Pn[2:0]</td>
<td>Input Divider Register n (n = 0...4)</td>
<td>Sets the input divider. The divider value has the range of 1, 2, 4, 8 and 0.5. See Table 3C for the divider coding.</td>
</tr>
<tr>
<td>FSEL[1:0]</td>
<td>Frequency Select Frequency Select Control used to select 1 of 4 frequency settings. See Table 3H default frequency setting.</td>
<td></td>
</tr>
<tr>
<td>Q_ENABLE</td>
<td>Q Output Enable</td>
<td>Q, nQ output enable. 1 = Output disabled (Q = low, nQ = high) 0 = Output enabled</td>
</tr>
<tr>
<td>LVDS_SWING</td>
<td>LVDS Swing</td>
<td>Normal LVDS output swing when LOW. Swing &gt;400mV when HIGH. Recommended setting = 1</td>
</tr>
<tr>
<td>DG0</td>
<td>Dither Gain</td>
<td>Recommended setting = 1</td>
</tr>
<tr>
<td>DG1</td>
<td>Dither Gain</td>
<td>Recommended setting = 1</td>
</tr>
<tr>
<td>DG2</td>
<td>Dither Gain</td>
<td>Recommended setting = 1</td>
</tr>
<tr>
<td>DG3</td>
<td>Dither Gain</td>
<td>Recommended setting = 1</td>
</tr>
<tr>
<td>DSM_ENAn</td>
<td>DSM Enable (n = 0...3)</td>
<td>Delta Sigma Modulator Enable. 0 = DSM not enabled 1 = DSM Enabled (default)</td>
</tr>
<tr>
<td>LFn</td>
<td>Loop Filter Value (n = 0...3)</td>
<td>Together with CPn[1:0] sets the PLL loop parameters. A higher value results in lower bandwidth. Contact IDT for a recommendation for changing LFn.</td>
</tr>
<tr>
<td>CPn[1:0]</td>
<td>Charge Pump Current</td>
<td>Together with LFn sets the loop parameters. A higher value results in higher loop bandwidth (opposite of LFn). Contact IDT for a recommendation for changing LFn.</td>
</tr>
<tr>
<td>OE_REF</td>
<td>REF_CLKOUT Output Enable</td>
<td>REF_CLKOUT, nREF_CLKOUT 1 = Output disabled 0 = Output enabled</td>
</tr>
<tr>
<td>nPLL_BYPASS</td>
<td>PLL Bypass</td>
<td>PLL Bypass. The output frequency = reference clock divided by N. 0 = PLL Bypass 1 = PLL Enable (default)</td>
</tr>
</tbody>
</table>
### Table 3C. Input Divider P Coding

<table>
<thead>
<tr>
<th>Register Bit</th>
<th>Input Divider P</th>
</tr>
</thead>
<tbody>
<tr>
<td>P&lt;sub&gt;n2&lt;/sub&gt; P&lt;sub&gt;n1&lt;/sub&gt; P&lt;sub&gt;n0&lt;/sub&gt;</td>
<td></td>
</tr>
<tr>
<td>0 0 0</td>
<td>1</td>
</tr>
<tr>
<td>0 0 1</td>
<td>2</td>
</tr>
<tr>
<td>0 1 0</td>
<td>4</td>
</tr>
<tr>
<td>0 1 1</td>
<td>8</td>
</tr>
<tr>
<td>1 X X</td>
<td>0.5</td>
</tr>
</tbody>
</table>

### Table 3D. PLL Post Divider N Coding

<table>
<thead>
<tr>
<th>Register Bit</th>
<th>Frequency Divider N</th>
<th>Output Frequency Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>N&lt;sub&gt;n&lt;/sub&gt;[6:0]</td>
<td></td>
<td>f&lt;sub&gt;OUT,MIN&lt;/sub&gt; (MHz)</td>
</tr>
<tr>
<td>000000X</td>
<td>2</td>
<td>990</td>
</tr>
<tr>
<td>0000010</td>
<td>2</td>
<td>990</td>
</tr>
<tr>
<td>0000011</td>
<td>3</td>
<td>660</td>
</tr>
<tr>
<td>0000100</td>
<td>4</td>
<td>495</td>
</tr>
<tr>
<td>0000101</td>
<td>5</td>
<td>396</td>
</tr>
<tr>
<td>000011X</td>
<td>6</td>
<td>330</td>
</tr>
<tr>
<td>000100X</td>
<td>8</td>
<td>247.5</td>
</tr>
<tr>
<td>000101X</td>
<td>10</td>
<td>198</td>
</tr>
<tr>
<td>000110X</td>
<td>12</td>
<td>165</td>
</tr>
<tr>
<td>000111X</td>
<td>14</td>
<td>141.4286</td>
</tr>
<tr>
<td>001000X</td>
<td>16</td>
<td>123.75</td>
</tr>
<tr>
<td>...</td>
<td>N (even integer)</td>
<td>(1980 ÷ N)</td>
</tr>
<tr>
<td>111101X</td>
<td>124</td>
<td>15.96774</td>
</tr>
<tr>
<td>111111X</td>
<td>126</td>
<td>15.71429</td>
</tr>
</tbody>
</table>

NOTE: “X” can be either 0 or 1 (don’t care).
Serial Interface Configuration Description

The IDT8V44003I has an I²C-compatible configuration interface to access any of the internal registers (Table 3A) for frequency and PLL parameter programming. The IDT8V44003I acts as a slave device on the I²C bus and has the address 0b1101110. The interface accepts byte-oriented block write and block read operations. An address byte (P) specifies the register address (Table 3A) as the byte position of the first register to write or read. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first, see Tables 3F, 3G). Read and write block transfers can be stopped after any complete byte transfer. It is recommended to terminate the I²C read or write transfer after accessing byte #23 by sending a stop command.

For full electrical I²C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-up resistors have a size of 51kΩ typical.

Table 3E. I²C Device Slave Address

<table>
<thead>
<tr>
<th>Address</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>1110110</td>
<td></td>
</tr>
</tbody>
</table>

Table 3F. Block Write Operation

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Length (bits)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>START</td>
<td>17</td>
</tr>
<tr>
<td>2:8</td>
<td>Slave Address W(0)</td>
<td>1</td>
</tr>
<tr>
<td>9</td>
<td>Ack</td>
<td>1</td>
</tr>
<tr>
<td>10</td>
<td>Ack</td>
<td>1</td>
</tr>
<tr>
<td>11:18</td>
<td>Data Byte P</td>
<td>8</td>
</tr>
<tr>
<td>19</td>
<td>Ack</td>
<td>1</td>
</tr>
<tr>
<td>20:27</td>
<td>Data Byte (P)</td>
<td>8</td>
</tr>
<tr>
<td>28</td>
<td>Ack</td>
<td>1</td>
</tr>
<tr>
<td>29-36</td>
<td>Data Byte (P+1)</td>
<td>8</td>
</tr>
<tr>
<td>37</td>
<td>Ack</td>
<td>1</td>
</tr>
<tr>
<td>...</td>
<td>Data Byte ...</td>
<td>1</td>
</tr>
<tr>
<td>...</td>
<td>ACK</td>
<td></td>
</tr>
<tr>
<td>STOP</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 3G. Block Read Operation

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Length (bits)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>START</td>
<td>17</td>
</tr>
<tr>
<td>2:8</td>
<td>Slave Address W(0)</td>
<td>1</td>
</tr>
<tr>
<td>9</td>
<td>Ack</td>
<td>1</td>
</tr>
<tr>
<td>10</td>
<td>Ack</td>
<td>1</td>
</tr>
<tr>
<td>11:18</td>
<td>Data Byte P</td>
<td>8</td>
</tr>
<tr>
<td>19</td>
<td>Ack</td>
<td>1</td>
</tr>
<tr>
<td>20</td>
<td>Ack</td>
<td>1</td>
</tr>
<tr>
<td>21:27</td>
<td>Slave Address R(1)</td>
<td>8</td>
</tr>
<tr>
<td>28</td>
<td>Ack</td>
<td>1</td>
</tr>
<tr>
<td>29</td>
<td>Ack</td>
<td>1</td>
</tr>
<tr>
<td>30:37</td>
<td>Data Byte (P)</td>
<td>8</td>
</tr>
<tr>
<td>38</td>
<td>Ack</td>
<td>1</td>
</tr>
<tr>
<td>39-46</td>
<td>Data Byte (P+1)</td>
<td>8</td>
</tr>
<tr>
<td>47</td>
<td>Ack</td>
<td>1</td>
</tr>
<tr>
<td>...</td>
<td>Data Byte ...</td>
<td>1</td>
</tr>
<tr>
<td>...</td>
<td>Ack</td>
<td></td>
</tr>
<tr>
<td>STOP</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 3H. Default Frequency Settings

<table>
<thead>
<tr>
<th>Register Bit</th>
<th>Output Frequency, ( f_{\text{out}} ) (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>FSEL[1:0]</td>
<td></td>
</tr>
<tr>
<td>00 (default)</td>
<td>480</td>
</tr>
<tr>
<td>01</td>
<td>480</td>
</tr>
<tr>
<td>10</td>
<td>240</td>
</tr>
<tr>
<td>11</td>
<td>240</td>
</tr>
</tbody>
</table>

NOTE: Output frequency based on REF_CLKIN = 80MHz
Absolute Maximum Ratings

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the DC Characteristics or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

<table>
<thead>
<tr>
<th>Item</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage, ( V_{DD} )</td>
<td>3.63V</td>
</tr>
<tr>
<td>Inputs, ( V_I ) (LVCMOS)</td>
<td>-0.5V to ( V_{DD} + 0.5V )</td>
</tr>
<tr>
<td>Outputs, ( V_O ) (LVCMOS)</td>
<td>-0.5V to ( V_{DD} + 0.5V )</td>
</tr>
<tr>
<td>Outputs, ( I_O ) (LVDS)</td>
<td>10mA</td>
</tr>
<tr>
<td>Continuous Current</td>
<td>15mA</td>
</tr>
<tr>
<td>Surge Current</td>
<td></td>
</tr>
<tr>
<td>Package Thermal Impedance, ( \theta_{JA} )</td>
<td>43.7°C/W (0 mps)</td>
</tr>
<tr>
<td>Storage Temperature, ( T_{STG} )</td>
<td>-65°C to 150°C</td>
</tr>
<tr>
<td>HBM – ESD Protection (Human Body Model); NOTE 1</td>
<td>2.500kV</td>
</tr>
<tr>
<td>CDM – ESD Protection (Charged Device Model); NOTE 1</td>
<td>1500V</td>
</tr>
</tbody>
</table>

NOTE 1: According to JEDEC/JESD 22-A114/22-C101.

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, \( V_{DD} = 3.3V \pm 5\% \), \( T_A = -40°C \) to \( 85°C \)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{DD} )</td>
<td>Core Supply Voltage</td>
<td>( V_{DD} ) - 0.17</td>
<td>3.135</td>
<td>3.3</td>
<td>3.465</td>
<td>V</td>
</tr>
<tr>
<td>( V_{DDA} )</td>
<td>Analog Supply Voltage</td>
<td>( V_{DD} )</td>
<td>3.3</td>
<td>( V_{DD} )</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( I_{DD} )</td>
<td>Core Supply Current</td>
<td>( V_{DD} )</td>
<td>136</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{DDA} )</td>
<td>Analog Supply Current</td>
<td>( V_{DD} )</td>
<td>17</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 4B. LVCMOS/LVTTL DC Characteristics, \( V_{DD} = 3.3V \pm 5\% \), \( T_A = -40°C \) to \( 85°C \)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IH} )</td>
<td>Input High Voltage</td>
<td>( V_{DD} = 3.3V )</td>
<td>2</td>
<td>( V_{DD} + 0.3 )</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{IL} )</td>
<td>Input Low Voltage</td>
<td>( V_{DD} = 3.3V )</td>
<td>0.8</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{IH} )</td>
<td>Input High Current</td>
<td>SCLK, SDATA</td>
<td>( V_{DD} = V_{IN} = 3.465V )</td>
<td>5</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>( I_{IL} )</td>
<td>Input Low Current</td>
<td>SCLK, SDATA</td>
<td>( V_{DD} = 3.465V, V_{IN} = 0V )</td>
<td>-150</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>( V_{OH} )</td>
<td>Output High Voltage</td>
<td>LOCK</td>
<td>( I_{OH} = -8mA )</td>
<td>2.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{OL} )</td>
<td>Output Low Voltage</td>
<td>LOCK</td>
<td>( I_{OL} = 8mA )</td>
<td>0.5</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>
### Table 4C. Differential DC Characteristics, $V_{DD} = 3.3V \pm 5\%, T_A = -40^\circ C$ to $85^\circ C$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{IH}$</td>
<td>Input High Current</td>
<td>REF_CLKIN, nREF_CLKIN</td>
<td>$V_{DD} = V_{IN} = 3.465V$</td>
<td>150</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Input Low Current</td>
<td>REF_CLKOUT</td>
<td>$V_{DD} = 3.465V, V_{IN} = 0V$</td>
<td>-5</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>nREF_CLKOUT</td>
<td>$V_{DD} = 3.465V, V_{IN} = 0V$</td>
<td>-150</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>$V_{PP}$</td>
<td>Peak-to-Peak Input Voltage</td>
<td></td>
<td></td>
<td>0.15</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{CMR}$</td>
<td>Common Mode Input Voltage; NOTE 1</td>
<td></td>
<td></td>
<td>1.1</td>
<td>$V_{DD}$</td>
<td></td>
</tr>
</tbody>
</table>

**NOTE 1.** Common mode voltage is defined as the crosspoint.

### Table 4D. LVDS DC Characteristics, $V_{DD} = 3.3V \pm 5\%, T_A = -40^\circ C$ to $85^\circ C$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OD}$</td>
<td>Differential Output Voltage</td>
<td></td>
<td>270</td>
<td>530</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>$\Delta V_{OD}$</td>
<td>$V_{OD}$ Magnitude Change</td>
<td></td>
<td>50</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OS}$</td>
<td>Offset Voltage</td>
<td></td>
<td>1.06</td>
<td>1.38</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$\Delta V_{OS}$</td>
<td>$V_{OS}$ Magnitude Change</td>
<td></td>
<td>50</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### AC Electrical Characteristics

**Table 5. AC Characteristics, \( V_{DD} = 3.3V \pm 5\%, T_A = -40^\circ C \) to 85°C**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_{IN} )</td>
<td>Input Frequency</td>
<td>REF_CLKIN, nREF_CLKIN</td>
<td>20</td>
<td>80</td>
<td>500</td>
<td>MHz</td>
</tr>
<tr>
<td>( f_{OUT} )</td>
<td>Output Frequency</td>
<td>Q, nQ</td>
<td>50</td>
<td>480</td>
<td>1200</td>
<td>MHz</td>
</tr>
<tr>
<td>( \Phi_{IN} (100) )</td>
<td>Single-Side Band Noise Power, 100Hz from Carrier</td>
<td>( f_{OUT} (Q) = 480MHz )</td>
<td>-96.64</td>
<td>dBC/Hz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \Phi_{IN} (1k) )</td>
<td>Single-Side Band Noise Power, 1kHz from Carrier</td>
<td>( f_{OUT} (Q) = 480MHz )</td>
<td>-104.57</td>
<td>dBC/Hz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \Phi_{IN} (10k) )</td>
<td>Single-Side Band Noise Power, 10kHz from Carrier</td>
<td>( f_{OUT} (Q) = 480MHz )</td>
<td>-113.20</td>
<td>dBC/Hz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \Phi_{IN} (100k) )</td>
<td>Single-Side Band Noise Power, 100kHz from Carrier</td>
<td>( f_{OUT} (Q) = 480MHz )</td>
<td>-122.79</td>
<td>dBC/Hz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \Phi_{IN} (1M) )</td>
<td>Single-Side Band Noise Power, 1MHz from Carrier</td>
<td>( f_{OUT} (Q) = 480MHz )</td>
<td>-128.71</td>
<td>dBC/Hz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \Phi_{IN} (10M) )</td>
<td>Single-Side Band Noise Power, 10MHz from Carrier</td>
<td>( f_{OUT} (Q) = 480MHz )</td>
<td>-145.79</td>
<td>dBC/Hz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \Phi_{N2} (100) )</td>
<td>Single-Side Band Noise Power, 100Hz from Carrier</td>
<td>( \Phi_{IN} (100) = -100dBC/Hz, ) REF_CLKOUT = 80MHz</td>
<td>-120.73</td>
<td>dBC/Hz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \Phi_{N2} (1k) )</td>
<td>Single-Side Band Noise Power, 1kHz from Carrier</td>
<td>( \Phi_{IN} (1k) = -130dBC/Hz, ) REF_CLKOUT = 80MHz</td>
<td>-133.593</td>
<td>dBC/Hz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \Phi_{N2} (10k) )</td>
<td>Single-Side Band Noise Power, 10kHz from Carrier</td>
<td>( \Phi_{IN} (10k) = -148dBC/Hz, ) REF_CLKOUT = 80MHz</td>
<td>-145.273</td>
<td>dBC/Hz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \Phi_{N2} (100k) )</td>
<td>Single-Side Band Noise Power, 100kHz from Carrier</td>
<td>( \Phi_{IN} (100k) = -150dBC/Hz, ) REF_CLKOUT = 80MHz</td>
<td>-146.428</td>
<td>dBC/Hz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \Phi_{N2} (1M) )</td>
<td>Single-Side Band Noise Power, 1MHz from Carrier</td>
<td>( \Phi_{IN} (1M) = -150dBC/Hz, ) REF_CLKOUT = 80MHz</td>
<td>-147.038</td>
<td>dBC/Hz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \Phi_{N2} (10M) )</td>
<td>Single-Side Band Noise Power, 10MHz from Carrier</td>
<td>( \Phi_{IN} (10M) = -150dBC/Hz, ) REF_CLKOUT = 80MHz</td>
<td>-147.16</td>
<td>dBC/Hz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \Phi_{SPUR} )</td>
<td>Single-Side Band Spur Power</td>
<td></td>
<td>-63</td>
<td>-50</td>
<td>dBC</td>
<td></td>
</tr>
<tr>
<td>Output ISOLATION</td>
<td>Output Isolation: NOTE 2</td>
<td>( f_{OUT} (Q) (480MHz) to ) ( \pm ) REF_CLKOUT, nREF_CLKOUT</td>
<td>-55.1</td>
<td>-49</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td> </td>
<td> </td>
<td>( f_{OUT} (Q) ) to REF_CLKOUT (High Impedance)</td>
<td>-57</td>
<td>-50</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>( t_R / t_F )</td>
<td>Output Rise/Fall Time</td>
<td>Q, nQ</td>
<td>175</td>
<td>590</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td> </td>
<td> </td>
<td>( f_{OUT} \leq 500MHz, 20% ) to 80%</td>
<td>175</td>
<td>590</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td> </td>
<td> </td>
<td>( 500MHz \leq f_{OUT} &lt; 1GHz, 20% ) to 80%</td>
<td>110</td>
<td>420</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td> </td>
<td> </td>
<td>( f_{OUT} \geq 1GHz, 20% ) to 80%</td>
<td>75</td>
<td>245</td>
<td>ps</td>
<td></td>
</tr>
</tbody>
</table>

Continued on next page.
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>odc</td>
<td>Output Duty Cycle</td>
<td>Q, nQ</td>
<td>f&lt;sub&gt;OUT&lt;/sub&gt; &lt; 1GHz</td>
<td>46</td>
<td>54</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>f&lt;sub&gt;OUT&lt;/sub&gt; ≥ 1GHz</td>
<td>43</td>
<td>57</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td>REF_CLKOUT, nREF_CLKOUT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>LOCK</td>
<td></td>
<td></td>
<td>44</td>
<td>56</td>
</tr>
<tr>
<td>t&lt;sub&gt;LOCK&lt;/sub&gt;</td>
<td>PLL Lock Time</td>
<td>LOCK</td>
<td></td>
<td></td>
<td>20</td>
<td>ms</td>
</tr>
</tbody>
</table>

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.


NOTE 3. Measured using a Rohde & Schwarz SMA100 signal generator, 9kHz to 6GHz as the input source with ±500mV sinewave single-ended input to REF_CLKIN.
Single Side Band Noise Power (80MHz)

Offset from Carrier Frequency (Hz)

SSB Phase Noise  dBC/Hz

Carrier 79.999999 MHz  -6.5977 dBm

Frequency Details:
1: 100 Hz  -119.7463 dBC/Hz
2: 1 kHz  -132.9222 dBC/Hz
3: 10 kHz  -142.8476 dBC/Hz
4: 100 kHz  -146.0758 dBC/Hz
5: 1 MHz  -147.1330 dBC/Hz
6: 10 MHz  -147.1668 dBC/Hz
7: >10 MHz  -147.1668 dBC/Hz

X: Start 100 Hz
Step 10 MHz
Center 80.0000 MHz
Span 4,000 MHz

Analysis Range X: Band Marker
Analysis Range Y: Band Marker

Integ Noise: -77.0820 dBc/√Hz
RMS Noise: 107.0312 nrad
11.3406 mdeg
RMS Jitter: 303.771 Fsec
Residual FM: 1.13482 kHz
RMS Phase Jitter (480MHz)

Offset from Carrier Frequency (Hz)

SSB Phase Noise dBc/Hz

-140 -120 -100 -80 -60 -40 dBc/Hz

10 Hz 100 Hz 1 kHz 10 kHz 100 kHz 1 MHz 10 MHz 300 MHz

Top -40 dBc/Hz -95.45 dBc/Hz 8.61 dB -105.81 dBc/Hz -113.2 dBc/Hz -122.95 dBc/Hz

EL1

EL2
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise**. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

Measured using a Rohde & Schwarz SMA100 as the input source.
Parameter Measurement Information

3.3V LVDS Output Load AC Test Circuit

Differential Input Level

Propagation Delay

RMS Phase Jitter

Output isolation (Q, nQ (480MHz) to ±REF_CLKOUT, nREF_CLKOUT)

Output isolation

Output select five
input clock signal

Output select active
input clock signal

Output select static
input

Output isolation

Spectrum of Output Signal Q

Output ISOL = A₀ – A₁

(fundamental)

Frequency

Amplitude (dB)

A₀

A₁

Offset Frequency

RMS Jitter = \( \sqrt{\text{Area Under Curve Defined by the Offset Frequency Markers}} \)

Phase Noise Plot

Noise Power
Parameter Measurement Information, continued

LVDS Output Duty Cycle/Pulse Width/Period

LVDS Output Rise/Fall Time

Differential Output Voltage Setup

Offset Voltage Setup

PLL Lock Time
Applications Information

Recommendations for Unused Input and Output Pins

Inputs:
LVCMOS Control Pins
All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:
LVDS Outputs
All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage \( V_1 = V_{DD}/2 \) is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the \( V_1 \) in the center of the input voltage swing. For example, if the input clock swing is 2.5V and \( V_{DD} = 3.3V \), R1 and R2 value should be adjusted to set \( V_1 \) at 1.25V. The values below are for when both the single ended swing and \( V_{DD} \) are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance.

For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however \( V_{IL} \) cannot be less than -0.3V and \( V_{IH} \) cannot be more than \( V_{DD} + 0.3V \). Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels
3.3V LVPECL Clock Input Interface

The REF_CLK/nREF_CLK accepts LVPECL, LVDS, HCSL and other differential signals. Both differential signals must meet the V_{pp} and V_{CMR} input requirements. Figures 2A to 2D show interface examples for the REF_CLK/nREF_CLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

Figure 2A. REF_CLK/nREF_CLK Input Driven by a 3.3V LVPECL Driver

Figure 2B. REF_CLK/nREF_CLK Input Driven by a 3.3V LVPECL Driver with AC Couple

Figure 2C. REF_CLK/nREF_CLK Input Driven by a 3.3V LVDS Driver

Figure 2D. REF_CLK/nREF_CLK Input Driven by a 3.3V HCSL Driver
LVDS Driver Termination

A general LVDS interface is shown in Figure 3A. Standard termination for LVDS type output structure requires both a 100Ω parallel resistor at the receiver and a 100Ω differential transmission line environment. In order to avoid any transmission line reflection issues, the 100Ω resistor must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in Figure 3A can be used with either type of output structure. If using a non-standard termination, it is recommended to contact IDT and confirm if the output is a current source or a voltage source type structure. In addition, since these outputs are LVDS compatible, the amplitude and common mode input range of the input receivers should be verified for compatibility with the output.

![Diagram](image)

**Figure 3A. Standard Termination**

**Figure 3B. Optional Termination**

LVDS Driver Termination
VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in Figure 4. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)
Schematic Example

Figure 5 shows an example of IDT8V44N003I application schematic. Input and output terminations shown are intended as examples only and may not represent the exact user configuration.

As with any high speed analog circuitry, the power supply pins are vulnerable to noise. To achieve optimum jitter performance, power supply isolation is required. The IDT8V44N003I provides separate power VDD and VDDA power supplies to isolate from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uF capacitor in each power pin filter should be placed on the device side of the PCB and the other components can be placed on the opposite side.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supply frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitances in the local area of all devices.

Figure 5. IDT8V44N003I Application Schematic
Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8V44N003I. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT8V44N003I is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for $V_{DD} = 3.3V + 5\% = 3.465V$, which gives worst case results.

   - Power (core)$_{MAX} = V_{DD\_MAX} \times (I_{DD\_MAX} + I_{DDA\_MAX}) = 3.465V \times (136mA + 17mA) = 530.145mW$

2. Junction Temperature.

Junction temperature, $T_j$, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, $T_j$, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

   - The equation for $T_j$ is as follows: $T_j = \theta_{JA} \times Pd\_total + T_A$
   - $T_j = $ Junction Temperature
   - $\theta_{JA} = $ Junction-to-Ambient Thermal Resistance
   - $Pd\_total = $ Total Device Power Dissipation (example calculation is in section 1 above)
   - $T_A = $ Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming no air flow and a multi-layer board, the appropriate value is 43.7°C/W per Table 6 below.

Therefore, $T_j$ for an ambient temperature of 85°C with all outputs switching is:

   - 85°C + 0.530W $\times$ 43.7°C/W = 108.2°C. This is below the limit of 125°C.

This calculation is only an example. $T_j$ will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance $\theta_{JA}$ for 32 Lead VFQFN, Forced Convection

<table>
<thead>
<tr>
<th>$\theta_{JA}$ by Velocity</th>
<th>0</th>
<th>1</th>
<th>2.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Meters per Second</td>
<td>43.7°C/W</td>
<td>38.2°C/W</td>
<td>34.2°C/W</td>
</tr>
<tr>
<td>Multi-Layer PCB, JEDEC Standard Test Boards</td>
<td>43.7°C/W</td>
<td>38.2°C/W</td>
<td>34.2°C/W</td>
</tr>
</tbody>
</table>
Reliability Information

Table 7. $\theta_{JA}$ vs. Air Flow Table for a 32 Lead VFQFN

<table>
<thead>
<tr>
<th></th>
<th>$\theta_{JA}$ vs. Air Flow</th>
</tr>
</thead>
<tbody>
<tr>
<td>Meter per Second</td>
<td>0</td>
</tr>
<tr>
<td>Multi-Layer PCB, JEDEC Standard Test Boards</td>
<td>43.7°C/W</td>
</tr>
</tbody>
</table>

Transistor Count

The transistor count for IDT8V44N003I is: 47,632
Package Outline and Package Dimensions
### Ordering Information

**Table 8. Ordering Information**

<table>
<thead>
<tr>
<th>Part/Order Number</th>
<th>Marking</th>
<th>Package</th>
<th>Shipping Packaging</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>8V44N003NLGI</td>
<td>IDT8V44N003NLGI</td>
<td>“Lead-Free” 32 Lead VFQFN</td>
<td>Tray</td>
<td>-40°C to 85°C</td>
</tr>
<tr>
<td>8V44N003NLGI8</td>
<td>IDT8V44N003NLGI</td>
<td>“Lead-Free” 32 Lead VFQFN</td>
<td>2500 Tape &amp; Reel</td>
<td>-40°C to 85°C</td>
</tr>
</tbody>
</table>

**NOTE:** Parts that are ordered with an "G" suffix to the part number are the Pb-Free configuration and are RoHS compliant.
## Revision History Sheet

<table>
<thead>
<tr>
<th>Rev</th>
<th>Table</th>
<th>Page</th>
<th>Description of Change</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td></td>
<td>2</td>
<td>Corrected block diagram, missing line from PFD to VCO to mux.</td>
<td>4/24/12</td>
</tr>
</tbody>
</table>
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