Programmable Timing Control Hub™ for Next Gen P4™ processor

Recommended Application:

Chipset for P4 type processor with PCI-Express

Output Features:

- 2 - 0.7V current-mode differential CPU pairs
- 1 - 0.7V current-mode differential CPU/PCI-Express selectable pair
- 6 - PCI, 33MHz
- 2 - REF, 14.318MHz
- 3 - 3V66, 66.66MHz
- 1 - 48MHz
- 1 - 24/48MHz
- 5 - PCI-Express 0.7V current mode differential pairs

Key Specifications:

- CPU outputs cycle-cycle jitter < 85ps
- 3V66 outputs cycle-cycle jitter < 250ps
- PCI outputs cycle-cycle jitter < 500ps

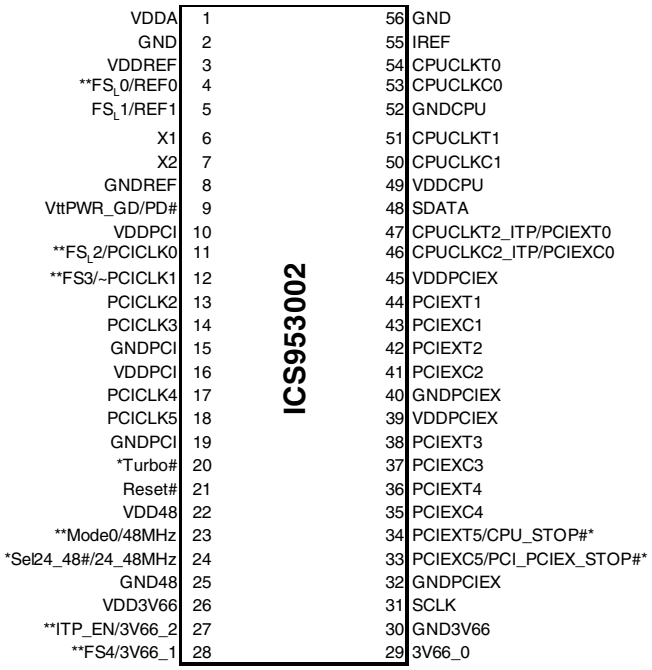
Features/Benefits:

- Programmable output frequency.
- Programmable asynchronous 3V66&PCI frequency.
- Programmable asynchronous PCI-Express frequency.
- Programmable output divider ratios.
- Programmable output skew.
- Programmable spread percentage for EMI control.
- Watchdog timer technology to reset system if system malfunctions.
- Programmable watch dog safe frequency.
- Support I2C Index read/write and block read/write operations.
- Uses external 14.318MHz reference input, external crystal load caps are required for frequency tuning.

Functionality

B0b4	B0b3	B0b2	B0b1	B0b0	PCI-EX	AGP	PCI	CPU
FS4	FS3	FSL2	FSL1	FSL0	MHz	MHz	MHz	MHz
0	0	0	0	0	100.00	66.66	33.33	266.66
0	0	0	0	1	100.00	66.66	33.33	133.33
0	0	0	1	0	100.00	66.66	33.33	200.00
0	0	0	1	1	100.00	66.66	33.33	166.66
0	0	1	0	0	N/A	N/A	N/A	N/A
0	0	1	0	1	100.00	66.66	33.33	100.00
0	0	1	1	0	100.00	66.66	33.33	400.00
0	0	1	1	1	100.00	66.66	33.33	200.00
0	1	0	0	0	100.00	66.66	33.33	100.00
0	1	0	0	1	100.00	66.66	33.33	133.33
0	1	0	1	0	100.00	66.66	33.33	200.00
0	1	0	1	1	100.00	66.66	33.33	166.66
0	1	1	0	0	100.00	66.66	33.33	100.00
0	1	1	0	1	100.00	66.66	33.33	133.33
0	1	1	1	0	100.00	66.66	33.33	200.00
0	1	1	1	1	100.00	66.66	33.33	166.66
1	0	0	0	0	100.00	66.66	33.33	266.66
1	0	0	0	1	100.00	66.66	33.33	133.33
1	0	0	1	0	100.00	66.66	33.33	200.00
1	0	0	1	1	100.00	66.66	33.33	166.66
1	0	1	0	0	N/A	N/A	N/A	N/A
1	0	1	0	1	100.00	66.66	33.33	100.00
1	0	1	1	0	100.00	66.66	33.33	400.00
1	0	1	1	1	100.00	66.66	33.33	200.00
1	1	0	0	0	100.00	66.66	33.33	266.66
1	1	0	0	1	100.00	66.66	33.33	133.33
1	1	0	1	0	100.00	66.66	33.33	200.00
1	1	0	1	1	100.00	66.66	33.33	166.66
1	1	1	0	0	N/A	N/A	N/A	N/A
1	1	1	0	1	100.00	66.66	33.33	100.00
1	1	1	1	0	100.00	66.66	33.33	400.00
1	1	1	1	1	100.00	66.66	33.33	200.00

Pin Configuration



56-Pin SSOP

*These inputs have 120K internal pull-up resistors to VDD.

**These inputs have 120K internal pull-down resistors to GND.

~This output is default 2X drive strength.

Pin Description

PIN #	PIN NAME	TYPE	DESCRIPTION
1	VDDA	PWR	3.3V power for the PLL core.
2	GND	PWR	Ground pin.
3	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
4	**FSL0/REF0	I/O	3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. / 14.318 MHz reference
5	FSL1/REF1	I/O	3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. / 14.318 MHz reference
6	X1	IN	Crystal input, Nominally 14.318MHz.
7	X2	OUT	Crystal output, Nominally 14.318MHz
8	GNDREF	PWR	Ground pin for the REF outputs.
9	VttPWR_GD/PD#	IN	This 3.3V LVTTL input is a level sensitive strobe used to determine when latch inputs are valid and are ready to be sampled. This is an active high input. / Asynchronous active low input pin used to power down the device into a low power state.
10	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
11	**FSL2/PCICLK0	I/O	3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. / 3.3V PCI clock output.
12	**FS3/~PCICLK1	I/O	Frequency select latch input pin / 3.3V PCI clock output.
13	PCICLK2	OUT	PCI clock output.
14	PCICLK3	OUT	PCI clock output.
15	GNDPCI	PWR	Ground pin for the PCI outputs
16	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
17	PCICLK4	OUT	PCI clock output.
18	PCICLK5	OUT	PCI clock output.
19	GNDPCI	PWR	Ground pin for the PCI outputs
20	*Turbo#	IN	Real time input pin to change frequency to a pre-programmed under or over clock entries located in the Rom table.
21	Reset#	OUT	Real time system reset signal for frequency gear ratio change or watchdog timer timeout. This signal is active low.
22	VDD48	PWR	Power pin for the 48MHz output.3.3V
23	**Mode0/48MHz	I/O	Function select pin, 1=Mobile Mode, 0=Desktop Mode / 48MHz clock output. 3.3V.
24	*Sel24_48#/24_48MHz	I/O	Latched select input for 24/48MHz output / 24/48MHz clock output. 1=24MHz, 0 = 48MHz.
25	GND48	PWR	Ground pin for the 48MHz outputs
26	VDD3V66	PWR	Power pin for the 3.3V 66MHz clocks.
27	**ITP_EN/3V66_2	I/O	3.3V 66.66MHz clock output./ ITP_EN: latched input to select pin functionality 1 = CPU_2_ITP pair 0 = PCI-EX0 pair
28	**FS4/3V66_1	I/O	Frequency select latch input pin / 66.66MHz clock output. 3.3V

Pin Description (Continued)

PIN #	PIN NAME	TYPE	DESCRIPTION
29	3V66_0	OUT	3.3V 66.66MHz clock output
30	GND3V66	PWR	Ground pin for the 3.3V 66MHz clocks
31	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
32	GNDPCIEX	PWR	Ground pin for the PCI-EX outputs
33	PCIEXC5/PCI_PCIEX_STOP#*	OUT	Complement clock of differential PCI_Express pair. / Active low signal that stops all PCI and PCIEX clocks besides the free running clocks
34	PCIEXT5/CPU_STOP#*	OUT	True clock of differential PCI_Express pair./Stops all CPUCLK besides the free running clocks
35	PCIEXC4	OUT	Complement clock of differential PCI_Express pair.
36	PCIEXT4	OUT	True clock of differential PCI_Express pair.
37	PCIEXC3	OUT	Complement clock of differential PCI_Express pair.
38	PCIEXT3	OUT	True clock of differential PCI_Express pair.
39	VDDPCIEX	PWR	Power supply for PCI Express clocks, nominal 3.3V
40	GNDPCIEX	PWR	Ground pin for the PCI-EX outputs
41	PCIEXC2	OUT	Complement clock of differential PCI_Express pair.
42	PCIEXT2	OUT	True clock of differential PCI_Express pair.
43	PCIEXC1	OUT	Complement clock of differential PCI_Express pair.
44	PCIEXT1	OUT	True clock of differential PCI_Express pair.
45	VDDPCIEX	PWR	Power supply for PCI Express clocks, nominal 3.3V
46	CPUCLKC2_ITP/PCIEXC0	OUT	Complementary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias./ Complement clock of differential PCIEX pair
47	CPUCLKT2_ITP/PCIEXT0	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias. / True clock of differential PCIEX pair
48	SDATA	I/O	Data pin for SMBus circuitry, 5V tolerant.
49	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
50	CPUCLKC1	OUT	Complementary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
51	CPUCLKT1	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
52	GNDCPU	PWR	Ground pin for the CPU outputs
53	CPUCLKC0	OUT	Complementary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
54	CPUCLKT0	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
55	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
56	GND	PWR	Ground pin.

General Description

ICS953002 is a 56-pin clock chip for P4 type processors with PCI-Express.

The **ICS953002** is part of a whole new line of ICS clock generators and buffers called TCH™ (Timing Control Hub). This part incorporates ICS's newest clock technology which offers more robust features and functionality. Employing the use of a serially programmable I^2C interface, this device can adjust the output clocks by configuring the frequency setting, the output divider ratios, selecting the ideal spread percentage, the output skew, the output strength, and enabling/disabling each individual output clock. M/N control can configure output frequency with resolution up to 0.1MHz increment.

Block Diagram

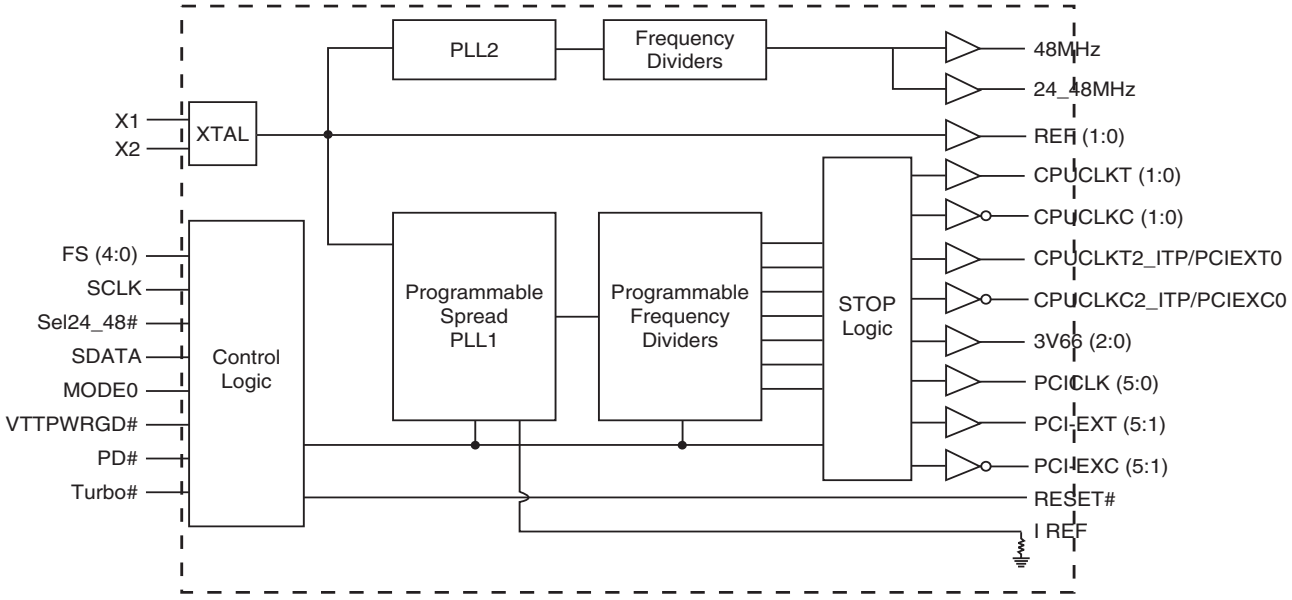


Table 1a. CPU PLL1 Turbo Rom

FS4	FS3	FSL2	FSL1	FSL0	CPUFS4	CPUFS3	CPUFS2	CPUFS1	CPUFS0	CPU	PCI-EX	AGP	PCI	Spreading
B0b4	B0b3	B0b2	B0b1	B0b0	B1bit4	B1bit3	B1bit2	B1bit1	B1bit0	Mhz	(default)	(default)	(default)	%
0	0	0	0	0	0	0	0	0	0	N/A	N/A	N/A	N/A	Down Sp 0-0.5 %
0	0	0	0	0	0	0	0	0	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	0	0	0	0	0	0	1	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	0	0	0	0	0	0	1	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	0	0	0	0	0	1	0	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	0	0	0	0	0	1	0	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	0	0	0	0	0	1	1	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	0	0	0	0	0	1	1	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	0	0	0	0	1	0	0	0	266.67	100.00	66.67	33.33	Down Sp 0-0.5 %
0	0	0	0	0	0	1	0	0	1	269.33	101.00	67.33	33.67	Center +/- 0.25
0	0	0	0	0	0	1	0	1	0	274.67	103.00	68.67	34.33	Center +/- 0.25
0	0	0	0	0	0	1	0	1	1	280.00	105.00	70.00	35.00	Center +/- 0.25
0	0	0	0	0	0	1	1	0	0	285.33	107.00	71.33	35.67	Center +/- 0.25
0	0	0	0	0	0	1	1	0	1	290.67	109.00	72.67	36.33	Center +/- 0.25
0	0	0	0	0	0	1	1	1	0	293.33	110.00	73.33	36.67	Center +/- 0.25
0	0	0	0	0	0	1	1	1	1	296.00	111.00	74.00	37.00	Center +/- 0.25
0	0	0	0	0	1	0	0	0	0	222.22	111.11	66.67	33.33	Down Sp 0-0.5 %
0	0	0	0	0	1	0	0	0	1	224.44	112.22	67.33	33.67	Center +/- 0.25
0	0	0	0	0	1	0	0	1	0	228.89	114.44	68.67	34.33	Center +/- 0.25
0	0	0	0	0	1	0	0	1	1	233.33	116.67	70.00	35.00	Center +/- 0.25
0	0	0	0	0	1	0	1	0	0	237.78	118.89	71.33	35.67	Center +/- 0.25
0	0	0	0	0	1	0	1	0	1	242.22	121.11	72.67	36.33	Center +/- 0.25
0	0	0	0	0	1	0	1	1	0	244.44	122.22	73.33	36.67	Center +/- 0.25
0	0	0	0	0	1	0	1	1	1	246.66	123.33	74.00	37.00	Center +/- 0.25
0	0	0	0	0	1	1	0	0	0	266.67	100.00	66.67	33.33	Down Sp 0-0.5 %
0	0	0	0	0	1	1	0	0	1	269.33	101.00	67.33	33.67	Center +/- 0.25
0	0	0	0	0	1	1	0	1	0	274.67	103.00	68.67	34.33	Center +/- 0.25
0	0	0	0	0	1	1	0	1	1	280.00	105.00	70.00	35.00	Center +/- 0.25
0	0	0	0	0	1	1	1	0	0	285.33	107.00	71.33	35.67	Center +/- 0.25
0	0	0	0	0	1	1	1	0	1	290.67	109.00	72.67	36.33	Center +/- 0.25
0	0	0	0	0	1	1	1	1	0	293.33	110.00	73.33	36.67	Center +/- 0.25
0	0	0	0	0	1	1	1	1	1	296.00	111.00	74.00	37.00	Center +/- 0.25

Table 1a. CPU PLL1 Turbo Rom (continued)

FS4	FS3	FSL2	FSL1	FSL0	CPUFS4	CPUFS3	CPUFS2	CPUFS1	CPUFS0	CPU	PCI-EX	AGP	PCI	Spreading
B0b4	B0b3	B0b2	B0b1	B0b0	B1bit4	B1bit3	B1bit2	B1bit1	B1bit0	Mhz	(default)	(default)	(default)	%
0	0	0	0	1	0	0	0	0	0	N/A	N/A	N/A	N/A	Down Sp 0-0.5 %
0	0	0	0	1	0	0	0	0	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	0	0	1	0	0	0	1	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	0	0	1	0	0	0	1	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	0	0	1	0	0	1	0	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	0	0	1	0	0	1	0	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	0	0	1	0	0	1	1	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	0	0	1	0	0	1	1	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	0	0	1	0	1	0	0	0	133.33	100.00	66.67	33.33	Down Sp 0-0.5 %
0	0	0	0	1	0	1	0	0	1	134.67	101.00	67.33	33.67	Center +/- 0.25
0	0	0	0	1	0	1	0	1	0	137.33	103.00	68.67	34.33	Center +/- 0.25
0	0	0	0	1	0	1	0	1	1	140.00	105.00	70.00	35.00	Center +/- 0.25
0	0	0	0	1	0	1	1	0	0	142.67	107.00	71.33	35.67	Center +/- 0.25
0	0	0	0	1	0	1	1	0	1	145.33	109.00	72.67	36.33	Center +/- 0.25
0	0	0	0	1	0	1	1	1	0	146.67	110.00	73.33	36.67	Center +/- 0.25
0	0	0	0	1	0	1	1	1	1	148.00	111.00	74.00	37.00	Center +/- 0.25
0	0	0	0	1	1	0	0	0	0	111.11	111.11	66.67	33.33	Down Sp 0-0.5 %
0	0	0	0	1	1	0	0	0	1	112.22	112.22	67.33	33.67	Center +/- 0.25
0	0	0	0	1	1	0	0	1	0	114.44	114.44	68.67	34.33	Center +/- 0.25
0	0	0	0	1	1	0	0	1	1	116.67	116.67	70.00	35.00	Center +/- 0.25
0	0	0	0	1	1	0	1	0	0	118.89	118.89	71.33	35.67	Center +/- 0.25
0	0	0	0	1	1	0	1	0	1	121.11	121.11	72.67	36.33	Center +/- 0.25
0	0	0	0	1	1	0	1	1	0	122.22	122.22	73.33	36.67	Center +/- 0.25
0	0	0	0	1	1	0	1	1	1	123.33	123.33	74.00	37.00	Center +/- 0.25
0	0	0	0	1	1	1	0	0	0	133.33	100.00	66.67	33.33	Down Sp 0-0.5 %
0	0	0	0	1	1	1	0	0	1	134.67	101.00	67.33	33.67	Center +/- 0.25
0	0	0	0	1	1	1	0	1	0	137.33	103.00	68.67	34.33	Center +/- 0.25
0	0	0	0	1	1	1	0	1	1	140.00	105.00	70.00	35.00	Center +/- 0.25
0	0	0	0	1	1	1	1	0	0	142.67	107.00	71.33	35.67	Center +/- 0.25
0	0	0	0	1	1	1	1	0	1	145.33	109.00	72.67	36.33	Center +/- 0.25
0	0	0	0	1	1	1	1	1	0	146.67	110.00	73.33	36.67	Center +/- 0.25
0	0	0	0	1	1	1	1	1	1	148.00	111.00	74.00	37.00	Center +/- 0.25

Table 1a. CPU PLL1 Turbo Rom (continued)

FS4	FS3	FSL2	FSL1	FSL0	CPUFS4	CPUFS3	CPUFS2	CPUFS1	CPUFS0	CPU	PCI-EX	AGP	PCI	Spreading
B0b4	B0b3	B0b2	B0b1	B0b0	B1bit4	B1bit3	B1bit2	B1bit1	B1bit0	Mhz	(default)	(default)	(default)	%
0	0	0	1	0	0	0	0	0	0	N/A	N/A	N/A	N/A	Down Sp 0-0.5 %
0	0	0	1	0	0	0	0	0	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	0	1	0	0	0	0	1	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	0	1	0	0	0	0	1	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	0	1	0	0	0	1	0	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	0	1	0	0	0	1	0	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	0	1	0	0	0	1	1	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	0	1	0	0	0	1	1	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	0	1	0	0	1	0	0	0	200.00	100.00	66.67	33.33	Down Sp 0-0.5 %
0	0	0	1	0	0	1	0	0	1	202.00	101.00	67.33	33.67	Center +/- 0.25
0	0	0	1	0	0	1	0	1	0	206.00	103.00	68.67	34.33	Center +/- 0.25
0	0	0	1	0	0	1	0	1	1	210.00	105.00	70.00	35.00	Center +/- 0.25
0	0	0	1	0	0	1	1	0	0	214.00	107.00	71.33	35.67	Center +/- 0.25
0	0	0	1	0	0	1	1	0	1	218.00	109.00	72.67	36.33	Center +/- 0.25
0	0	0	1	0	0	1	1	1	0	220.00	110.00	73.33	36.67	Center +/- 0.25
0	0	0	1	0	0	1	1	1	1	222.00	111.00	74.00	37.00	Center +/- 0.25
0	0	0	1	0	1	0	0	0	0	166.67	111.11	66.67	33.33	Down Sp 0-0.5 %
0	0	0	1	0	1	0	0	0	1	168.33	112.22	67.33	33.67	Center +/- 0.25
0	0	0	1	0	1	0	0	1	0	171.66	114.44	68.67	34.33	Center +/- 0.25
0	0	0	1	0	1	0	0	1	1	175.00	116.67	70.00	35.00	Center +/- 0.25
0	0	0	1	0	1	0	1	0	0	178.33	118.89	71.33	35.67	Center +/- 0.25
0	0	0	1	0	1	0	1	0	1	181.66	121.11	72.67	36.33	Center +/- 0.25
0	0	0	1	0	1	0	1	1	0	183.33	122.22	73.33	36.67	Center +/- 0.25
0	0	0	1	0	1	0	1	1	1	185.00	123.33	74.00	37.00	Center +/- 0.25
0	0	0	1	0	1	1	0	0	0	200.00	100.00	66.67	33.33	Down Sp 0-0.5 %
0	0	0	1	0	1	1	0	0	1	202.00	101.00	67.33	33.67	Center +/- 0.25
0	0	0	1	0	1	1	0	1	0	206.00	103.00	68.67	34.33	Center +/- 0.25
0	0	0	1	0	1	1	0	1	1	210.00	105.00	70.00	35.00	Center +/- 0.25
0	0	0	1	0	1	1	1	0	0	214.00	107.00	71.33	35.67	Center +/- 0.25
0	0	0	1	0	1	1	1	0	1	218.00	109.00	72.67	36.33	Center +/- 0.25
0	0	0	1	0	1	1	1	1	0	220.00	110.00	73.33	36.67	Center +/- 0.25
0	0	0	1	0	1	1	1	1	1	222.00	111.00	74.00	37.00	Center +/- 0.25

Table 1a. CPU PLL1 Turbo Rom (continued)

FS4	FS3	FSL2	FSL1	FSL0	CPUFS4	CPUFS3	CPUFS2	CPUFS1	CPUFS0	CPU	PCI-EX	AGP	PCI	Spreading
B0b4	B0b3	B0b2	B0b1	B0b0	B1bit4	B1bit3	B1bit2	B1bit1	B1bit0	Mhz	(default)	(default)	(default)	%
0	0	0	1	1	0	0	0	0	0	N/A	N/A	N/A	N/A	Down Sp 0-0.5 %
0	0	0	1	1	0	0	0	0	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	0	1	1	0	0	0	1	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	0	1	1	0	0	0	1	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	0	1	1	0	0	1	0	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	0	1	1	0	0	1	0	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	0	1	1	0	0	1	1	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	0	1	1	0	0	1	1	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	0	1	1	0	1	0	0	0	200.00	100.00	66.67	33.33	Down Sp 0-0.5 %
0	0	0	1	1	0	1	0	0	1	202.00	101.00	67.33	33.67	Center +/- 0.25
0	0	0	1	1	0	1	0	1	0	206.00	103.00	68.67	34.33	Center +/- 0.25
0	0	0	1	1	0	1	0	1	1	210.00	105.00	70.00	35.00	Center +/- 0.25
0	0	0	1	1	0	1	1	0	0	214.00	107.00	71.33	35.67	Center +/- 0.25
0	0	0	1	1	0	1	1	0	1	218.00	109.00	72.67	36.33	Center +/- 0.25
0	0	0	1	1	0	1	1	1	0	220.00	110.00	73.33	36.67	Center +/- 0.25
0	0	0	1	1	0	1	1	1	1	222.00	111.00	74.00	37.00	Center +/- 0.25
0	0	0	1	1	1	0	0	0	0	166.67	111.11	66.67	33.33	Down Sp 0-0.5 %
0	0	0	1	1	1	0	0	0	1	168.33	112.22	67.33	33.67	Center +/- 0.25
0	0	0	1	1	1	0	0	1	0	171.66	114.44	68.67	34.33	Center +/- 0.25
0	0	0	1	1	1	0	0	1	1	175.00	116.67	70.00	35.00	Center +/- 0.25
0	0	0	1	1	1	0	1	0	0	178.33	118.89	71.33	35.67	Center +/- 0.25
0	0	0	1	1	1	0	1	0	1	181.66	121.11	72.67	36.33	Center +/- 0.25
0	0	0	1	1	1	0	1	1	0	183.33	122.22	73.33	36.67	Center +/- 0.25
0	0	0	1	1	1	0	1	1	1	185.00	123.33	74.00	37.00	Center +/- 0.25
0	0	0	1	1	1	1	0	0	0	200.00	100.00	66.67	33.33	Down Sp 0-0.5 %
0	0	0	1	1	1	1	0	0	1	202.00	101.00	67.33	33.67	Center +/- 0.25
0	0	0	1	1	1	1	0	1	0	206.00	103.00	68.67	34.33	Center +/- 0.25
0	0	0	1	1	1	1	0	1	1	210.00	105.00	70.00	35.00	Center +/- 0.25
0	0	0	1	1	1	1	1	0	0	214.00	107.00	71.33	35.67	Center +/- 0.25
0	0	0	1	1	1	1	1	0	1	218.00	109.00	72.67	36.33	Center +/- 0.25
0	0	0	1	1	1	1	1	1	0	220.00	110.00	73.33	36.67	Center +/- 0.25
0	0	0	1	1	1	1	1	1	1	222.00	111.00	74.00	37.00	Center +/- 0.25

Table 1a. CPU PLL1 Turbo Rom (continued)

FS4	FS3	FSL2	FSL1	FSL0	CPUFS4	CPUFS3	CPUFS2	CPUFS1	CPUFS0	CPU	PCI-EX	AGP	PCI	Spreading
B0b4	B0b3	B0b2	B0b1	B0b0	B1bit4	B1bit3	B1bit2	B1bit1	B1bit0	Mhz	(default)	(default)	(default)	%
0	0	1	0	0	0	0	0	0	0	N/A	N/A	N/A	N/A	Down Sp 0-0.5 %
0	0	1	0	0	0	0	0	0	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	1	0	0	0	0	0	1	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	1	0	0	0	0	0	1	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	1	0	0	0	0	1	0	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	1	0	0	0	0	1	0	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	1	0	0	0	0	1	1	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	1	0	0	0	0	1	1	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	1	0	0	0	1	0	0	0	266.67	100.00	66.67	33.33	Down Sp 0-0.5 %
0	0	1	0	0	0	1	0	0	1	269.33	101.00	67.33	33.67	Center +/- 0.25
0	0	1	0	0	0	1	0	1	0	274.67	103.00	68.67	34.33	Center +/- 0.25
0	0	1	0	0	0	1	0	1	1	280.00	105.00	70.00	35.00	Center +/- 0.25
0	0	1	0	0	0	1	1	0	0	285.33	107.00	71.33	35.67	Center +/- 0.25
0	0	1	0	0	0	1	1	0	1	290.67	109.00	72.67	36.33	Center +/- 0.25
0	0	1	0	0	0	1	1	1	0	293.33	110.00	73.33	36.67	Center +/- 0.25
0	0	1	0	0	0	1	1	1	1	296.00	111.00	74.00	37.00	Center +/- 0.25
0	0	1	0	0	1	0	0	0	0	222.22	111.11	66.67	33.33	Down Sp 0-0.5 %
0	0	1	0	0	1	0	0	0	1	224.44	112.22	67.33	33.67	Center +/- 0.25
0	0	1	0	0	1	0	0	1	0	228.89	114.44	68.67	34.33	Center +/- 0.25
0	0	1	0	0	1	0	0	1	1	233.33	116.67	70.00	35.00	Center +/- 0.25
0	0	1	0	0	1	0	1	0	0	237.78	118.89	71.33	35.67	Center +/- 0.25
0	0	1	0	0	1	0	1	0	1	242.22	121.11	72.67	36.33	Center +/- 0.25
0	0	1	0	0	1	0	1	1	0	244.44	122.22	73.33	36.67	Center +/- 0.25
0	0	1	0	0	1	0	1	1	1	246.66	123.33	74.00	37.00	Center +/- 0.25
0	0	1	0	0	1	1	0	0	0	266.67	100.00	66.67	33.33	Down Sp 0-0.5 %
0	0	1	0	0	1	1	0	0	1	269.33	101.00	67.33	33.67	Center +/- 0.25
0	0	1	0	0	1	1	0	1	0	274.67	103.00	68.67	34.33	Center +/- 0.25
0	0	1	0	0	1	1	0	1	1	280.00	105.00	70.00	35.00	Center +/- 0.25
0	0	1	0	0	1	1	1	0	0	285.33	107.00	71.33	35.67	Center +/- 0.25
0	0	1	0	0	1	1	1	0	1	290.67	109.00	72.67	36.33	Center +/- 0.25
0	0	1	0	0	1	1	1	1	0	293.33	110.00	73.33	36.67	Center +/- 0.25
0	0	1	0	0	1	1	1	1	1	296.00	111.00	74.00	37.00	Center +/- 0.25

Table 1a. CPU PLL1 Turbo Rom (continued)

FS4	FS3	FSL2	FSL1	FSL0	CPUFS4	CPUFS3	CPUFS2	CPUFS1	CPUFS0	CPU	PCI-EX	AGP	PCI	Spreading
B0b4	B0b3	B0b2	B0b1	B0b0	B1bit4	B1bit3	B1bit2	B1bit1	B1bit0	Mhz	(default)	(default)	(default)	%
0	0	1	0	1	0	0	0	0	0	N/A	N/A	N/A	N/A	Down Sp 0-0.5 %
0	0	1	0	1	0	0	0	0	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	1	0	1	0	0	0	1	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	1	0	1	0	0	0	1	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	1	0	1	0	0	1	0	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	1	0	1	0	0	1	0	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	1	0	1	0	0	1	1	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	1	0	1	0	0	1	1	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	1	0	1	0	1	0	0	0	100.00	100.00	66.67	33.33	Down Sp 0-0.5 %
0	0	1	0	1	0	1	0	0	1	101.00	101.00	67.33	33.67	Center +/- 0.25
0	0	1	0	1	0	1	0	1	0	103.00	103.00	68.67	34.33	Center +/- 0.25
0	0	1	0	1	0	1	0	1	1	105.00	105.00	70.00	35.00	Center +/- 0.25
0	0	1	0	1	0	1	1	0	0	107.00	107.00	71.33	35.67	Center +/- 0.25
0	0	1	0	1	0	1	1	0	1	109.00	109.00	72.67	36.33	Center +/- 0.25
0	0	1	0	1	0	1	1	1	0	110.00	110.00	73.33	36.67	Center +/- 0.25
0	0	1	0	1	0	1	1	1	1	111.00	111.00	74.00	37.00	Center +/- 0.25
0	0	1	0	1	1	0	0	0	0	83.33	111.11	66.67	33.33	Down Sp 0-0.5 %
0	0	1	0	1	1	0	0	0	1	84.17	112.22	67.33	33.67	Center +/- 0.25
0	0	1	0	1	1	0	0	1	0	85.83	114.44	68.67	34.33	Center +/- 0.25
0	0	1	0	1	1	0	0	1	1	87.50	116.67	70.00	35.00	Center +/- 0.25
0	0	1	0	1	1	0	1	0	0	89.17	118.89	71.33	35.67	Center +/- 0.25
0	0	1	0	1	1	0	1	0	1	90.83	121.11	72.67	36.33	Center +/- 0.25
0	0	1	0	1	1	0	1	1	0	91.67	122.22	73.33	36.67	Center +/- 0.25
0	0	1	0	1	1	0	1	1	1	92.50	123.33	74.00	37.00	Center +/- 0.25
0	0	1	0	1	1	1	0	0	0	100.00	100.00	66.67	33.33	Down Sp 0-0.5 %
0	0	1	0	1	1	1	0	0	1	101.00	101.00	67.33	33.67	Center +/- 0.25
0	0	1	0	1	1	1	0	1	0	103.00	103.00	68.67	34.33	Center +/- 0.25
0	0	1	0	1	1	1	0	1	1	105.00	105.00	70.00	35.00	Center +/- 0.25
0	0	1	0	1	1	1	1	0	0	107.00	107.00	71.33	35.67	Center +/- 0.25
0	0	1	0	1	1	1	1	0	1	109.00	109.00	72.67	36.33	Center +/- 0.25
0	0	1	0	1	1	1	1	1	0	110.00	110.00	73.33	36.67	Center +/- 0.25
0	0	1	0	1	1	1	1	1	1	111.00	111.00	74.00	37.00	Center +/- 0.25

Table 1a. CPU PLL1 Turbo Rom (continued)

FS4	FS3	FSL2	FSL1	FSL0	CPUFS4	CPUFS3	CPUFS2	CPUFS1	CPUFS0	CPU	PCI-EX	AGP	PCI	Spreading
B0b4	B0b3	B0b2	B0b1	B0b0	B1bit4	B1bit3	B1bit2	B1bit1	B1bit0	Mhz	(default)	(default)	(default)	%
0	0	1	1	0	0	0	0	0	0	N/A	N/A	N/A	N/A	Down Sp 0-0.5 %
0	0	1	1	0	0	0	0	0	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	1	1	0	0	0	0	1	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	1	1	0	0	0	0	1	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	1	1	0	0	0	1	0	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	1	1	0	0	0	1	0	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	1	1	0	0	0	1	1	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	1	1	0	0	0	1	1	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	1	1	0	0	1	0	0	0	400.00	100.00	66.67	33.33	Down Sp 0-0.5 %
0	0	1	1	0	0	1	0	0	1	404.00	101.00	67.33	33.67	Center +/- 0.25
0	0	1	1	0	0	1	0	1	0	412.00	103.00	68.67	34.33	Center +/- 0.25
0	0	1	1	0	0	1	0	1	1	420.00	105.00	70.00	35.00	Center +/- 0.25
0	0	1	1	0	0	1	1	0	0	428.00	107.00	71.33	35.67	Center +/- 0.25
0	0	1	1	0	0	1	1	0	1	436.00	109.00	72.67	36.33	Center +/- 0.25
0	0	1	1	0	0	1	1	1	0	440.00	110.00	73.33	36.67	Center +/- 0.25
0	0	1	1	0	0	1	1	1	1	444.00	111.00	74.00	37.00	Center +/- 0.25
0	0	1	1	0	1	0	0	0	0	333.33	111.11	66.67	33.33	Down Sp 0-0.5 %
0	0	1	1	0	1	0	0	0	1	336.66	112.22	67.33	33.67	Center +/- 0.25
0	0	1	1	0	1	0	0	1	0	343.33	114.44	68.67	34.33	Center +/- 0.25
0	0	1	1	0	1	0	0	1	1	350.00	116.67	70.00	35.00	Center +/- 0.25
0	0	1	1	0	1	0	1	0	0	356.66	118.89	71.33	35.67	Center +/- 0.25
0	0	1	1	0	1	0	1	0	1	363.33	121.11	72.67	36.33	Center +/- 0.25
0	0	1	1	0	1	0	1	1	0	366.66	122.22	73.33	36.67	Center +/- 0.25
0	0	1	1	0	1	0	1	1	1	370.00	123.33	74.00	37.00	Center +/- 0.25
0	0	1	1	0	1	1	0	0	0	400.00	100.00	66.67	33.33	Down Sp 0-0.5 %
0	0	1	1	0	1	1	0	0	1	404.00	101.00	67.33	33.67	Center +/- 0.25
0	0	1	1	0	1	1	0	1	0	412.00	103.00	68.67	34.33	Center +/- 0.25
0	0	1	1	0	1	1	0	1	1	420.00	105.00	70.00	35.00	Center +/- 0.25
0	0	1	1	0	1	1	1	0	0	428.00	107.00	71.33	35.67	Center +/- 0.25
0	0	1	1	0	1	1	1	0	1	436.00	109.00	72.67	36.33	Center +/- 0.25
0	0	1	1	0	1	1	1	1	0	440.00	110.00	73.33	36.67	Center +/- 0.25
0	0	1	1	0	1	1	1	1	1	444.00	111.00	74.00	37.00	Center +/- 0.25

Table 1a. CPU PLL1 Turbo Rom (continued)

FS4	FS3	FSL2	FSL1	FSL0	CPUFS4	CPUFS3	CPUFS2	CPUFS1	CPUFS0	CPU	PCI-EX	AGP	PCI	Spreading
B0b4	B0b3	B0b2	B0b1	B0b0	B1bit4	B1bit3	B1bit2	B1bit1	B1bit0	Mhz	(default)	(default)	(default)	%
0	0	1	1	1	0	0	0	0	0	N/A	N/A	N/A	N/A	Down Sp 0-0.5 %
0	0	1	1	1	0	0	0	0	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	1	1	1	0	0	0	1	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	1	1	1	0	0	0	1	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	1	1	1	0	0	1	0	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	1	1	1	0	0	1	0	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	1	1	1	0	0	1	1	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	1	1	1	0	0	1	1	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	0	1	1	1	0	1	0	0	0	200.00	100.00	66.67	33.33	Down Sp 0-0.5 %
0	0	1	1	1	0	1	0	0	1	202.00	101.00	67.33	33.67	Center +/- 0.25
0	0	1	1	1	0	1	0	1	0	206.00	103.00	68.67	34.33	Center +/- 0.25
0	0	1	1	1	0	1	0	1	1	210.00	105.00	70.00	35.00	Center +/- 0.25
0	0	1	1	1	0	1	1	0	0	214.00	107.00	71.33	35.67	Center +/- 0.25
0	0	1	1	1	0	1	1	0	1	218.00	109.00	72.67	36.33	Center +/- 0.25
0	0	1	1	1	0	1	1	1	0	220.00	110.00	73.33	36.67	Center +/- 0.25
0	0	1	1	1	0	1	1	1	1	222.00	111.00	74.00	37.00	Center +/- 0.25
0	0	1	1	1	1	0	0	0	0	166.67	111.11	66.67	33.33	Down Sp 0-0.5 %
0	0	1	1	1	1	0	0	0	1	168.33	112.22	67.33	33.67	Center +/- 0.25
0	0	1	1	1	1	0	0	1	0	171.66	114.44	68.67	34.33	Center +/- 0.25
0	0	1	1	1	1	0	0	1	1	175.00	116.67	70.00	35.00	Center +/- 0.25
0	0	1	1	1	1	0	1	0	0	178.33	118.89	71.33	35.67	Center +/- 0.25
0	0	1	1	1	1	0	1	0	1	181.66	121.11	72.67	36.33	Center +/- 0.25
0	0	1	1	1	1	0	1	1	0	183.33	122.22	73.33	36.67	Center +/- 0.25
0	0	1	1	1	1	0	1	1	1	185.00	123.33	74.00	37.00	Center +/- 0.25
0	0	1	1	1	1	1	0	0	0	200.00	100.00	66.67	33.33	Down Sp 0-0.5 %
0	0	1	1	1	1	1	0	0	1	202.00	101.00	67.33	33.67	Center +/- 0.25
0	0	1	1	1	1	1	0	1	0	206.00	103.00	68.67	34.33	Center +/- 0.25
0	0	1	1	1	1	1	0	1	1	210.00	105.00	70.00	35.00	Center +/- 0.25
0	0	1	1	1	1	1	1	0	0	214.00	107.00	71.33	35.67	Center +/- 0.25
0	0	1	1	1	1	1	1	0	1	218.00	109.00	72.67	36.33	Center +/- 0.25
0	0	1	1	1	1	1	1	1	0	220.00	110.00	73.33	36.67	Center +/- 0.25
0	0	1	1	1	1	1	1	1	1	222.00	111.00	74.00	37.00	Center +/- 0.25

Table 1a. CPU PLL1 Turbo Rom (continued)

FS4	FS3	FSL2	FSL1	FSL0	CPUFS4	CPUFS3	CPUFS2	CPUFS1	CPUFS0	CPU	PCI-EX	AGP	PCI	Spreading
B0b4	B0b3	B0b2	B0b1	B0b0	B1bit4	B1bit3	B1bit2	B1bit1	B1bit0	Mhz	(default)	(default)	(default)	%
0	1	0	0	0	0	0	0	0	0	N/A	N/A	N/A	N/A	Down Sp 0-0.5 %
0	1	0	0	0	0	0	0	0	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	0	0	0	0	0	0	1	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	0	0	0	0	0	0	1	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	0	0	0	0	0	1	0	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	0	0	0	0	0	1	0	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	0	0	0	0	0	1	1	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	0	0	0	0	0	1	1	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	0	0	0	0	1	0	0	0	100.00	100.00	66.67	33.33	Down Sp 0-0.5 %
0	1	0	0	0	0	1	0	0	1	101.00	101.00	67.33	33.67	Center +/- 0.25
0	1	0	0	0	0	1	0	1	0	103.00	103.00	68.67	34.33	Center +/- 0.25
0	1	0	0	0	0	1	0	1	1	105.00	105.00	70.00	35.00	Center +/- 0.25
0	1	0	0	0	0	1	1	0	0	107.00	107.00	71.33	35.67	Center +/- 0.25
0	1	0	0	0	0	1	1	0	1	109.00	109.00	72.67	36.33	Center +/- 0.25
0	1	0	0	0	0	1	1	1	0	110.00	110.00	73.33	36.67	Center +/- 0.25
0	1	0	0	0	0	1	1	1	1	111.00	111.00	74.00	37.00	Center +/- 0.25
0	1	0	0	0	1	0	0	0	0	83.33	111.11	66.67	33.33	Down Sp 0-0.5 %
0	1	0	0	0	1	0	0	0	1	84.17	112.22	67.33	33.67	Center +/- 0.25
0	1	0	0	0	1	0	0	1	0	85.83	114.44	68.67	34.33	Center +/- 0.25
0	1	0	0	0	1	0	0	1	1	87.50	116.67	70.00	35.00	Center +/- 0.25
0	1	0	0	0	1	0	1	0	0	89.17	118.89	71.33	35.67	Center +/- 0.25
0	1	0	0	0	1	0	1	0	1	90.83	121.11	72.67	36.33	Center +/- 0.25
0	1	0	0	0	1	0	1	1	0	91.67	122.22	73.33	36.67	Center +/- 0.25
0	1	0	0	0	1	0	1	1	1	92.50	123.33	74.00	37.00	Center +/- 0.25
0	1	0	0	0	1	1	0	0	0	100.00	100.00	66.67	33.33	Down Sp 0-0.5 %
0	1	0	0	0	1	1	0	0	1	101.00	101.00	67.33	33.67	Center +/- 0.25
0	1	0	0	0	1	1	0	1	0	103.00	103.00	68.67	34.33	Center +/- 0.25
0	1	0	0	0	1	1	0	1	1	105.00	105.00	70.00	35.00	Center +/- 0.25
0	1	0	0	0	1	1	1	0	0	107.00	107.00	71.33	35.67	Center +/- 0.25
0	1	0	0	0	1	1	1	0	1	109.00	109.00	72.67	36.33	Center +/- 0.25
0	1	0	0	0	1	1	1	1	0	110.00	110.00	73.33	36.67	Center +/- 0.25
0	1	0	0	0	1	1	1	1	1	111.00	111.00	74.00	37.00	Center +/- 0.25

Table 1a. CPU PLL1 Turbo Rom (continued)

FS4	FS3	FSL2	FSL1	FSL0	CPUFS4	CPUFS3	CPUFS2	CPUFS1	CPUFS0	CPU	PCI-EX	AGP	PCI	Spreading
B0b4	B0b3	B0b2	B0b1	B0b0	B1bit4	B1bit3	B1bit2	B1bit1	B1bit0	Mhz	(default)	(default)	(default)	%
0	1	0	0	1	0	0	0	0	0	N/A	N/A	N/A	N/A	Down Sp 0-0.5 %
0	1	0	0	1	0	0	0	0	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	0	0	1	0	0	0	1	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	0	0	1	0	0	0	1	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	0	0	1	0	0	1	0	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	0	0	1	0	0	1	0	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	0	0	1	0	0	1	1	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	0	0	1	0	0	1	1	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	0	0	1	0	1	0	0	0	133.33	100.00	66.67	33.33	Down Sp 0-0.5 %
0	1	0	0	1	0	1	0	0	1	134.67	101.00	67.33	33.67	Center +/- 0.25
0	1	0	0	1	0	1	0	1	0	137.33	103.00	68.67	34.33	Center +/- 0.25
0	1	0	0	1	0	1	0	1	1	140.00	105.00	70.00	35.00	Center +/- 0.25
0	1	0	0	1	0	1	1	0	0	142.67	107.00	71.33	35.67	Center +/- 0.25
0	1	0	0	1	0	1	1	0	1	145.33	109.00	72.67	36.33	Center +/- 0.25
0	1	0	0	1	0	1	1	1	0	146.67	110.00	73.33	36.67	Center +/- 0.25
0	1	0	0	1	0	1	1	1	1	148.00	111.00	74.00	37.00	Center +/- 0.25
0	1	0	0	1	1	0	0	0	0	111.11	111.11	66.67	33.33	Down Sp 0-0.5 %
0	1	0	0	1	1	0	0	0	1	112.22	112.22	67.33	33.67	Center +/- 0.25
0	1	0	0	1	1	0	0	1	0	114.44	114.44	68.67	34.33	Center +/- 0.25
0	1	0	0	1	1	0	0	1	1	116.67	116.67	70.00	35.00	Center +/- 0.25
0	1	0	0	1	1	0	1	0	0	118.89	118.89	71.33	35.67	Center +/- 0.25
0	1	0	0	1	1	0	1	0	1	121.11	121.11	72.67	36.33	Center +/- 0.25
0	1	0	0	1	1	0	1	1	0	122.22	122.22	73.33	36.67	Center +/- 0.25
0	1	0	0	1	1	0	1	1	1	123.33	123.33	74.00	37.00	Center +/- 0.25
0	1	0	0	1	1	1	0	0	0	133.33	100.00	66.67	33.33	Down Sp 0-0.5 %
0	1	0	0	1	1	1	0	0	1	134.67	101.00	67.33	33.67	Center +/- 0.25
0	1	0	0	1	1	1	0	1	0	137.33	103.00	68.67	34.33	Center +/- 0.25
0	1	0	0	1	1	1	0	1	1	140.00	105.00	70.00	35.00	Center +/- 0.25
0	1	0	0	1	1	1	1	0	0	142.67	107.00	71.33	35.67	Center +/- 0.25
0	1	0	0	1	1	1	1	0	1	145.33	109.00	72.67	36.33	Center +/- 0.25
0	1	0	0	1	1	1	1	1	0	146.67	110.00	73.33	36.67	Center +/- 0.25
0	1	0	0	1	1	1	1	1	1	148.00	111.00	74.00	37.00	Center +/- 0.25

Table 1a. CPU PLL1 Turbo Rom (continued)

FS4	FS3	FSL2	FSL1	FSL0	CPUFS4	CPUFS3	CPUFS2	CPUFS1	CPUFS0	CPU	PCI-EX	AGP	PCI	Spreading
B0b4	B0b3	B0b2	B0b1	B0b0	B1bit4	B1bit3	B1bit2	B1bit1	B1bit0	Mhz	(default)	(default)	(default)	%
0	1	0	1	0	0	0	0	0	0	N/A	N/A	N/A	N/A	Down Sp 0-0.5 %
0	1	0	1	0	0	0	0	0	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	0	1	0	0	0	0	1	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	0	1	0	0	0	0	1	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	0	1	0	0	0	1	0	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	0	1	0	0	0	1	0	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	0	1	0	0	0	1	1	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	0	1	0	0	0	1	1	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	0	1	0	0	1	0	0	0	200.00	100.00	66.67	33.33	Down Sp 0-0.5 %
0	1	0	1	0	0	1	0	0	1	202.00	101.00	67.33	33.67	Center +/- 0.25
0	1	0	1	0	0	1	0	1	0	206.00	103.00	68.67	34.33	Center +/- 0.25
0	1	0	1	0	0	1	0	1	1	210.00	105.00	70.00	35.00	Center +/- 0.25
0	1	0	1	0	0	1	1	0	0	214.00	107.00	71.33	35.67	Center +/- 0.25
0	1	0	1	0	0	1	1	0	1	218.00	109.00	72.67	36.33	Center +/- 0.25
0	1	0	1	0	0	1	1	1	0	220.00	110.00	73.33	36.67	Center +/- 0.25
0	1	0	1	0	0	1	1	1	1	222.00	111.00	74.00	37.00	Center +/- 0.25
0	1	0	1	0	1	0	0	0	0	166.67	111.11	66.67	33.33	Down Sp 0-0.5 %
0	1	0	1	0	1	0	0	0	1	168.33	112.22	67.33	33.67	Center +/- 0.25
0	1	0	1	0	1	0	0	1	0	171.66	114.44	68.67	34.33	Center +/- 0.25
0	1	0	1	0	1	0	0	1	1	175.00	116.67	70.00	35.00	Center +/- 0.25
0	1	0	1	0	1	0	1	0	0	178.33	118.89	71.33	35.67	Center +/- 0.25
0	1	0	1	0	1	0	1	0	1	181.66	121.11	72.67	36.33	Center +/- 0.25
0	1	0	1	0	1	0	1	1	0	183.33	122.22	73.33	36.67	Center +/- 0.25
0	1	0	1	0	1	0	1	1	1	185.00	123.33	74.00	37.00	Center +/- 0.25
0	1	0	1	0	1	1	0	0	0	200.00	100.00	66.67	33.33	Down Sp 0-0.5 %
0	1	0	1	0	1	1	0	0	1	202.00	101.00	67.33	33.67	Center +/- 0.25
0	1	0	1	0	1	1	0	1	0	206.00	103.00	68.67	34.33	Center +/- 0.25
0	1	0	1	0	1	1	0	1	1	210.00	105.00	70.00	35.00	Center +/- 0.25
0	1	0	1	0	1	1	1	0	0	214.00	107.00	71.33	35.67	Center +/- 0.25
0	1	0	1	0	1	1	1	0	1	218.00	109.00	72.67	36.33	Center +/- 0.25
0	1	0	1	0	1	1	1	1	0	220.00	110.00	73.33	36.67	Center +/- 0.25
0	1	0	1	0	1	1	1	1	1	222.00	111.00	74.00	37.00	Center +/- 0.25

Table 1a. CPU PLL1 Turbo Rom (continued)

FS4	FS3	FSL2	FSL1	FSL0	CPUFS4	CPUFS3	CPUFS2	CPUFS1	CPUFS0	CPU	PCI-EX	AGP	PCI	Spreading
B0b4	B0b3	B0b2	B0b1	B0b0	B1bit4	B1bit3	B1bit2	B1bit1	B1bit0	Mhz	(default)	(default)	(default)	%
0	1	0	1	1	0	0	0	0	0	N/A	N/A	N/A	N/A	Down Sp 0-0.5 %
0	1	0	1	1	0	0	0	0	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	0	1	1	0	0	0	1	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	0	1	1	0	0	0	1	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	0	1	1	0	0	1	0	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	0	1	1	0	0	1	0	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	0	1	1	0	0	1	1	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	0	1	1	0	0	1	1	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	0	1	1	0	1	0	0	0	200.00	100.00	66.67	33.33	Down Sp 0-0.5 %
0	1	0	1	1	0	1	0	0	1	202.00	101.00	67.33	33.67	Center +/- 0.25
0	1	0	1	1	0	1	0	1	0	206.00	103.00	68.67	34.33	Center +/- 0.25
0	1	0	1	1	0	1	0	1	1	210.00	105.00	70.00	35.00	Center +/- 0.25
0	1	0	1	1	0	1	1	0	0	214.00	107.00	71.33	35.67	Center +/- 0.25
0	1	0	1	1	0	1	1	0	1	218.00	109.00	72.67	36.33	Center +/- 0.25
0	1	0	1	1	0	1	1	1	0	220.00	110.00	73.33	36.67	Center +/- 0.25
0	1	0	1	1	0	1	1	1	1	222.00	111.00	74.00	37.00	Center +/- 0.25
0	1	0	1	1	1	0	0	0	0	166.67	111.11	66.67	33.33	Down Sp 0-0.5 %
0	1	0	1	1	1	0	0	0	1	168.33	112.22	67.33	33.67	Center +/- 0.25
0	1	0	1	1	1	0	0	1	0	171.66	114.44	68.67	34.33	Center +/- 0.25
0	1	0	1	1	1	0	0	1	1	175.00	116.67	70.00	35.00	Center +/- 0.25
0	1	0	1	1	1	0	1	0	0	178.33	118.89	71.33	35.67	Center +/- 0.25
0	1	0	1	1	1	0	1	0	1	181.66	121.11	72.67	36.33	Center +/- 0.25
0	1	0	1	1	1	0	1	1	0	183.33	122.22	73.33	36.67	Center +/- 0.25
0	1	0	1	1	1	0	1	1	1	185.00	123.33	74.00	37.00	Center +/- 0.25
0	1	0	1	1	1	1	0	0	0	200.00	100.00	66.67	33.33	Down Sp 0-0.5 %
0	1	0	1	1	1	1	0	0	1	202.00	101.00	67.33	33.67	Center +/- 0.25
0	1	0	1	1	1	1	0	1	0	206.00	103.00	68.67	34.33	Center +/- 0.25
0	1	0	1	1	1	1	0	1	1	210.00	105.00	70.00	35.00	Center +/- 0.25
0	1	0	1	1	1	1	1	0	0	214.00	107.00	71.33	35.67	Center +/- 0.25
0	1	0	1	1	1	1	1	0	1	218.00	109.00	72.67	36.33	Center +/- 0.25
0	1	0	1	1	1	1	1	1	0	220.00	110.00	73.33	36.67	Center +/- 0.25
0	1	0	1	1	1	1	1	1	1	222.00	111.00	74.00	37.00	Center +/- 0.25

Table 1a. CPU PLL1 Turbo Rom (continued)

FS4	FS3	FSL2	FSL1	FSL0	CPUFS4	CPUFS3	CPUFS2	CPUFS1	CPUFS0	CPU	PCI-EX	AGP	PCI	Spreading
B0b4	B0b3	B0b2	B0b1	B0b0	B1bit4	B1bit3	B1bit2	B1bit1	B1bit0	Mhz	(default)	(default)	(default)	%
0	1	1	0	0	0	0	0	0	0	N/A	N/A	N/A	N/A	Down Sp 0-0.5 %
0	1	1	0	0	0	0	0	0	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	1	0	0	0	0	0	1	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	1	0	0	0	0	0	1	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	1	0	0	0	0	1	0	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	1	0	0	0	0	1	0	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	1	0	0	0	0	1	1	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	1	0	0	0	0	1	1	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	1	0	0	0	1	0	0	0	100.00	100.00	66.67	33.33	Down Sp 0-0.5 %
0	1	1	0	0	0	1	0	0	1	101.00	101.00	67.33	33.67	Center +/- 0.25
0	1	1	0	0	0	1	0	1	0	103.00	103.00	68.67	34.33	Center +/- 0.25
0	1	1	0	0	0	1	0	1	1	105.00	105.00	70.00	35.00	Center +/- 0.25
0	1	1	0	0	0	1	1	0	0	107.00	107.00	71.33	35.67	Center +/- 0.25
0	1	1	0	0	0	1	1	0	1	109.00	109.00	72.67	36.33	Center +/- 0.25
0	1	1	0	0	0	1	1	1	0	110.00	110.00	73.33	36.67	Center +/- 0.25
0	1	1	0	0	0	1	1	1	1	111.00	111.00	74.00	37.00	Center +/- 0.25
0	1	1	0	0	1	0	0	0	0	83.33	111.11	66.67	33.33	Down Sp 0-0.5 %
0	1	1	0	0	1	0	0	0	1	84.17	112.22	67.33	33.67	Center +/- 0.25
0	1	1	0	0	1	0	0	1	0	85.83	114.44	68.67	34.33	Center +/- 0.25
0	1	1	0	0	1	0	0	1	1	87.50	116.67	70.00	35.00	Center +/- 0.25
0	1	1	0	0	1	0	1	0	0	89.17	118.89	71.33	35.67	Center +/- 0.25
0	1	1	0	0	1	0	1	0	1	90.83	121.11	72.67	36.33	Center +/- 0.25
0	1	1	0	0	1	0	1	1	0	91.67	122.22	73.33	36.67	Center +/- 0.25
0	1	1	0	0	1	0	1	1	1	92.50	123.33	74.00	37.00	Center +/- 0.25
0	1	1	0	0	1	1	0	0	0	100.00	100.00	66.67	33.33	Down Sp 0-0.5 %
0	1	1	0	0	1	1	0	0	1	101.00	101.00	67.33	33.67	Center +/- 0.25
0	1	1	0	0	1	1	0	1	0	103.00	103.00	68.67	34.33	Center +/- 0.25
0	1	1	0	0	1	1	0	1	1	105.00	105.00	70.00	35.00	Center +/- 0.25
0	1	1	0	0	1	1	1	0	0	107.00	107.00	71.33	35.67	Center +/- 0.25
0	1	1	0	0	1	1	1	0	1	109.00	109.00	72.67	36.33	Center +/- 0.25
0	1	1	0	0	1	1	1	1	0	110.00	110.00	73.33	36.67	Center +/- 0.25
0	1	1	0	0	1	1	1	1	1	111.00	111.00	74.00	37.00	Center +/- 0.25

Table 1a. CPU PLL1 Turbo Rom (continued)

FS4	FS3	FSL2	FSL1	FSL0	CPUFS4	CPUFS3	CPUFS2	CPUFS1	CPUFS0	CPU	PCI-EX	AGP	PCI	Spreading
B0b4	B0b3	B0b2	B0b1	B0b0	B1bit4	B1bit3	B1bit2	B1bit1	B1bit0	Mhz	(default)	(default)	(default)	%
0	1	1	0	1	0	0	0	0	0	N/A	N/A	N/A	N/A	Down Sp 0-0.5 %
0	1	1	0	1	0	0	0	0	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	1	0	1	0	0	0	1	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	1	0	1	0	0	0	1	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	1	0	1	0	0	1	0	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	1	0	1	0	0	1	0	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	1	0	1	0	0	1	1	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	1	0	1	0	0	1	1	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	1	0	1	0	1	0	0	0	133.33	100.00	66.67	33.33	Down Sp 0-0.5 %
0	1	1	0	1	0	1	0	0	1	134.67	101.00	67.33	33.67	Center +/- 0.25
0	1	1	0	1	0	1	0	1	0	137.33	103.00	68.67	34.33	Center +/- 0.25
0	1	1	0	1	0	1	0	1	1	140.00	105.00	70.00	35.00	Center +/- 0.25
0	1	1	0	1	0	1	1	0	0	142.67	107.00	71.33	35.67	Center +/- 0.25
0	1	1	0	1	0	1	1	0	1	145.33	109.00	72.67	36.33	Center +/- 0.25
0	1	1	0	1	0	1	1	1	0	146.67	110.00	73.33	36.67	Center +/- 0.25
0	1	1	0	1	0	1	1	1	1	148.00	111.00	74.00	37.00	Center +/- 0.25
0	1	1	0	1	1	0	0	0	0	111.11	111.11	66.67	33.33	Down Sp 0-0.5 %
0	1	1	0	1	1	0	0	0	1	112.22	112.22	67.33	33.67	Center +/- 0.25
0	1	1	0	1	1	0	0	1	0	114.44	114.44	68.67	34.33	Center +/- 0.25
0	1	1	0	1	1	0	0	1	1	116.67	116.67	70.00	35.00	Center +/- 0.25
0	1	1	0	1	1	0	1	0	0	118.89	118.89	71.33	35.67	Center +/- 0.25
0	1	1	0	1	1	0	1	0	1	121.11	121.11	72.67	36.33	Center +/- 0.25
0	1	1	0	1	1	0	1	1	0	122.22	122.22	73.33	36.67	Center +/- 0.25
0	1	1	0	1	1	0	1	1	1	123.33	123.33	74.00	37.00	Center +/- 0.25
0	1	1	0	1	1	1	0	0	0	133.33	100.00	66.67	33.33	Down Sp 0-0.5 %
0	1	1	0	1	1	1	0	0	1	134.67	101.00	67.33	33.67	Center +/- 0.25
0	1	1	0	1	1	1	0	1	0	137.33	103.00	68.67	34.33	Center +/- 0.25
0	1	1	0	1	1	1	0	1	1	140.00	105.00	70.00	35.00	Center +/- 0.25
0	1	1	0	1	1	1	1	0	0	142.67	107.00	71.33	35.67	Center +/- 0.25
0	1	1	0	1	1	1	1	0	1	145.33	109.00	72.67	36.33	Center +/- 0.25
0	1	1	0	1	1	1	1	1	0	146.67	110.00	73.33	36.67	Center +/- 0.25
0	1	1	0	1	1	1	1	1	1	148.00	111.00	74.00	37.00	Center +/- 0.25

Table 1a. CPU PLL1 Turbo Rom (continued)

FS4	FS3	FSL2	FSL1	FSL0	CPUFS4	CPUFS3	CPUFS2	CPUFS1	CPUFS0	CPU	PCI-EX	AGP	PCI	Spreading
B0b4	B0b3	B0b2	B0b1	B0b0	B1bit4	B1bit3	B1bit2	B1bit1	B1bit0	Mhz	(default)	(default)	(default)	%
0	1	1	1	0	0	0	0	0	0	N/A	N/A	N/A	N/A	Down Sp 0-0.5 %
0	1	1	1	0	0	0	0	0	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	1	1	0	0	0	0	1	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	1	1	0	0	0	0	1	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	1	1	0	0	0	1	0	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	1	1	0	0	0	1	0	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	1	1	0	0	0	1	1	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	1	1	0	0	0	1	1	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	1	1	0	0	1	0	0	0	200.00	100.00	66.67	33.33	Down Sp 0-0.5 %
0	1	1	1	0	0	1	0	0	1	202.00	101.00	67.33	33.67	Center +/- 0.25
0	1	1	1	0	0	1	0	1	0	206.00	103.00	68.67	34.33	Center +/- 0.25
0	1	1	1	0	0	1	0	1	1	210.00	105.00	70.00	35.00	Center +/- 0.25
0	1	1	1	0	0	1	1	0	0	214.00	107.00	71.33	35.67	Center +/- 0.25
0	1	1	1	0	0	1	1	0	1	218.00	109.00	72.67	36.33	Center +/- 0.25
0	1	1	1	0	0	1	1	1	0	220.00	110.00	73.33	36.67	Center +/- 0.25
0	1	1	1	0	0	1	1	1	1	222.00	111.00	74.00	37.00	Center +/- 0.25
0	1	1	1	0	1	0	0	0	0	166.67	111.11	66.67	33.33	Down Sp 0-0.5 %
0	1	1	1	0	1	0	0	0	1	168.33	112.22	67.33	33.67	Center +/- 0.25
0	1	1	1	0	1	0	0	1	0	171.66	114.44	68.67	34.33	Center +/- 0.25
0	1	1	1	0	1	0	0	1	1	175.00	116.67	70.00	35.00	Center +/- 0.25
0	1	1	1	0	1	0	1	0	0	178.33	118.89	71.33	35.67	Center +/- 0.25
0	1	1	1	0	1	0	1	0	1	181.66	121.11	72.67	36.33	Center +/- 0.25
0	1	1	1	0	1	0	1	1	0	183.33	122.22	73.33	36.67	Center +/- 0.25
0	1	1	1	0	1	0	1	1	1	185.00	123.33	74.00	37.00	Center +/- 0.25
0	1	1	1	0	1	1	0	0	0	200.00	100.00	66.67	33.33	Down Sp 0-0.5 %
0	1	1	1	0	1	1	0	0	1	202.00	101.00	67.33	33.67	Center +/- 0.25
0	1	1	1	0	1	1	0	1	0	206.00	103.00	68.67	34.33	Center +/- 0.25
0	1	1	1	0	1	1	0	1	1	210.00	105.00	70.00	35.00	Center +/- 0.25
0	1	1	1	0	1	1	1	0	0	214.00	107.00	71.33	35.67	Center +/- 0.25
0	1	1	1	0	1	1	1	0	1	218.00	109.00	72.67	36.33	Center +/- 0.25
0	1	1	1	0	1	1	1	1	0	220.00	110.00	73.33	36.67	Center +/- 0.25
0	1	1	1	0	1	1	1	1	1	222.00	111.00	74.00	37.00	Center +/- 0.25

Table 1a. CPU PLL1 Turbo Rom (continued)

FS4	FS3	FSL2	FSL1	FSL0	CPUFS4	CPUFS3	CPUFS2	CPUFS1	CPUFS0	CPU	PCI-EX	AGP	PCI	Spreading
B0b4	B0b3	B0b2	B0b1	B0b0	B1bit4	B1bit3	B1bit2	B1bit1	B1bit0	Mhz	(default)	(default)	(default)	%
0	1	1	1	1	0	0	0	0	0	N/A	N/A	N/A	N/A	Down Sp 0-0.5 %
0	1	1	1	1	0	0	0	0	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	1	1	1	0	0	0	1	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	1	1	1	0	0	0	1	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	1	1	1	0	0	1	0	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	1	1	1	0	0	1	0	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	1	1	1	0	0	1	1	0	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	1	1	1	0	0	1	1	1	N/A	N/A	N/A	N/A	Center +/- 0.25
0	1	1	1	1	0	1	0	0	0	200.00	100.00	66.67	33.33	Down Sp 0-0.5 %
0	1	1	1	1	0	1	0	0	1	202.00	101.00	67.33	33.67	Center +/- 0.25
0	1	1	1	1	0	1	0	1	0	206.00	103.00	68.67	34.33	Center +/- 0.25
0	1	1	1	1	0	1	0	1	1	210.00	105.00	70.00	35.00	Center +/- 0.25
0	1	1	1	1	0	1	1	0	0	214.00	107.00	71.33	35.67	Center +/- 0.25
0	1	1	1	1	0	1	1	0	1	218.00	109.00	72.67	36.33	Center +/- 0.25
0	1	1	1	1	0	1	1	1	0	220.00	110.00	73.33	36.67	Center +/- 0.25
0	1	1	1	1	0	1	1	1	1	222.00	111.00	74.00	37.00	Center +/- 0.25
0	1	1	1	1	1	0	0	0	0	166.67	111.11	66.67	33.33	Down Sp 0-0.5 %
0	1	1	1	1	1	0	0	0	1	168.33	112.22	67.33	33.67	Center +/- 0.25
0	1	1	1	1	1	0	0	1	0	171.66	114.44	68.67	34.33	Center +/- 0.25
0	1	1	1	1	1	0	0	1	1	175.00	116.67	70.00	35.00	Center +/- 0.25
0	1	1	1	1	1	0	1	0	0	178.33	118.89	71.33	35.67	Center +/- 0.25
0	1	1	1	1	1	0	1	0	1	181.66	121.11	72.67	36.33	Center +/- 0.25
0	1	1	1	1	1	0	1	1	0	183.33	122.22	73.33	36.67	Center +/- 0.25
0	1	1	1	1	1	0	1	1	1	185.00	123.33	74.00	37.00	Center +/- 0.25
0	1	1	1	1	1	1	0	0	0	200.00	100.00	66.67	33.33	Down Sp 0-0.5 %
0	1	1	1	1	1	1	0	0	1	202.00	101.00	67.33	33.67	Center +/- 0.25
0	1	1	1	1	1	1	0	1	0	206.00	103.00	68.67	34.33	Center +/- 0.25
0	1	1	1	1	1	1	0	1	1	210.00	105.00	70.00	35.00	Center +/- 0.25
0	1	1	1	1	1	1	1	0	0	214.00	107.00	71.33	35.67	Center +/- 0.25
0	1	1	1	1	1	1	1	0	1	218.00	109.00	72.67	36.33	Center +/- 0.25
0	1	1	1	1	1	1	1	1	0	220.00	110.00	73.33	36.67	Center +/- 0.25
0	1	1	1	1	1	1	1	1	1	222.00	111.00	74.00	37.00	Center +/- 0.25

Table 1b. PLL2 AGP/PCI/SRC/PCI-EX Select

B0b4	B0b3	B0b2	PCI-EX	AGP	PCI	Spread
FS4	FS3	FSL2	B5b6 = 1	B5b7 = 1	B5b7=1	%
0	0	0	100	66.66	33.33	0 to -0.5% Down
0	0	1	100	66.66	33.33	0 to -0.5% Down
0	1	0	100	66.66	33.33	0 to -0.5% Down
0	1	1	102.00	68.00	34.00	Center SP +/- 0.25
1	0	0	102.00	68.00	34.00	Center SP +/- 0.25
1	0	1	102.00	68.00	34.00	Center SP +/- 0.25
1	1	0	100	66.66	33.33	Center SP +/- 0.25
1	1	1	100	66.66	33.33	Center SP +/- 0.25

General I²C serial interface information for the ICS953002

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if X(H) was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address D2(H)			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
	○		
	○		○
	○		○
			○
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)		ICS (Slave/Receiver)	
T	starT bit		
Slave Address D2(H)			
WR	WRite		
		ACK	
Beginning Byte = N			
		ACK	
RT	Repeat starT		
Slave Address D3(H)			
RD	ReaD		
		ACK	
		Data Byte Count = X	
ACK			
		X Byte	Beginning Byte N
ACK			
			○
○			○
○			○
○			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

I²C Table: Device Control Register

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	FS Source	Frequency H/W IIC Select	RW	Latch Inputs	IIC	0
Bit 6	-	Reserved	Reserved	RW	-	-	1
Bit 5	-	ROD	Reset On Demand	RW	Disable	Enable	0
Bit 4	-	FS4	Freq/Div Sel Bit 4	RW	See Table 1b: PLL2 AGP/PCI Frequency Selection Table		latch
Bit 3	-	FS3	Freq/Div Sel Bit 3	RW			latch
Bit 2	-	FSL2	Freq/Div Sel Bit 2	RW			latch
Bit 1	-	FSL1	Freq/Div Sel Bit 1	RW			latch
Bit 0	-	FSL0	Freq/Div Sel Bit 0	RW			latch

I²C Table: Device Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SS_EN1	PLL1 Spread Enable	RW	OFF	ON	1
Bit 6	-	SS_EN2	PLL2 Spread Enable	RW	OFF	ON	1
Bit 5	-	M/N Enable bit	M/N Programming Enable bit	RW	Disable	Enable	0
Bit 4	-	CPUFS4	PLL1 VCO Sel b4	RW	See Table 1a: PLL1 Rom VCO Frequency Selection Table		X
Bit 3	-	CPUFS3	PLL1 VCO Sel b3	RW			X
Bit 2	-	CPUFS2	PLL1 VCO Sel b2	RW			0
Bit 1	-	CPUFS1	PLL1 VCO Sel b1	RW			0
Bit 0	-	CPUFS0	PLL1 VCO Sel b0	RW			0

B1b[4:3] = 00 is invalid

I²C Table: Output Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	REF0	Output Control	RW	Disable	Enable	1
Bit 6	-	REF1	Output Control	RW	Disable	Enable	1
Bit 5	-	PCICLK0	Output Control	RW	Disable	Enable	1
Bit 4	-	PCICLK1	Output Control	RW	Disable	Enable	1
Bit 3	-	PCICLK2	Output Control	RW	Disable	Enable	1
Bit 2	-	PCICLK3	Output Control	RW	Disable	Enable	1
Bit 1	-	PCICLK4	Output Control	RW	Disable	Enable	1
Bit 0	-	PCICLK5	Output Control	RW	Disable	Enable	1

I²C Table: Output Control Register

Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	48MHz	Output Control	RW	Disable	Enable	1
Bit 6	-	24_48MHz	Output Control	RW	Disable	Enable	1
Bit 5	-	3V66_2	Output Control	RW	Disable	Enable	1
Bit 4	-	3V66_1	Output Control	RW	Disable	Enable	1
Bit 3	-	3V66_0	Output Control	RW	Disable	Enable	1
Bit 2	-	SEL24_48MHz	Output Select	RW	48MHz	24MHz	Latch
Bit 1	-	ITP_EN	Output Select	RW	PCIEXCLKT/C0	CPUCLKT/C2	Latch
Bit 0	-	Mode 0	Output Select	RW	PCIEXCLKT/C5	CPU_STOP/PCI_PCIEX_STOP	Latch

I²C Table: Output Control Register

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	PCIEXCLKT/C5	Output Control	RW	Disable	Enable	1
Bit 6	-	PCIEXCLKT/C4	Output Control	RW	Disable	Enable	1
Bit 5	-	PCIEXCLKT/C3	Output Control	RW	Disable	Enable	1
Bit 4	-	PCIEXCLKT/C2	Output Control	RW	Disable	Enable	1
Bit 3	-	PCIEXCLKT/C1	Output Control	RW	Disable	Enable	1
Bit 2	-	CPUCLK2/PCIEX0	Output Control	RW	Disable	Enable	1
Bit 1	-	CPUCLKT/C1	Output Control	RW	Disable	Enable	1
Bit 0	-	CPUCLKT/C0	Output Control	RW	Disable	Enable	1

I²C Table: Device Control Register

Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	AGP/PCI PLL Cntrl	AGP/PCI PLL Source	RW	PLL1	PLL2	0
Bit 6	-	PCIEX PLL Cntrl	PCIEX PLL Source	RW	PLL1	PLL2	0
Bit 5	-	Reserved	Reserved	RW	-	-	1
Bit 4	-	Reserved	Reserved	RW	-	-	1
Bit 3	-	ASYNC1	3V66/PCI Async Freq Prog bits	RW	00 = PLL1/2	10 = 75.4/37.7	0
Bit 2	-	ASYNC0		RW	01 = 66.0/33.0	11 = 88.0/44.0	0
Bit 1	-	Reserved	Reserved	RW	-	-	1
Bit 0	-	Reserved	Reserved	RW	-	-	1

I²C Table: Reserved Register

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	0
Bit 6	-	Reserved	Reserved	RW	-	-	0
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	Reserved	Reserved	RW	-	-	0
Bit 3	-	Reserved	Reserved	RW	-	-	0
Bit 2	-	Reserved	Reserved	RW	-	-	0
Bit 1	-	Reserved	Reserved	RW	-	-	0
Bit 0	-	Reserved	Reserved	RW	-	-	0

I²C Table: Vendor ID Register

Byte 7	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	REVID3	Revision ID	R	-	-	0
Bit 6	-	REVID2	Revision ID	R	-	-	0
Bit 5	-	REVID1	Revision ID	R	-	-	0
Bit 4	-	REVID0	Revision ID	R	-	-	0
Bit 3	-	VID3	Vendor ID	R	-	-	0
Bit 2	-	VID2	Vendor ID	R	-	-	0
Bit 1	-	VID1	Vendor ID	R	-	-	0
Bit 0	-	VID0	Vendor ID	R	0001 = ICS	-	1

I²C Table: Byte Count Register

Byte 8	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	BC7	Byte Count Programming b(7:0)	RW	Writing to this register will configure how many bytes will be read back, default is 0F = 15 bytes.		0
Bit 6	-	BC6		RW			0
Bit 5	-	BC5		RW			0
Bit 4	-	BC4		RW			0
Bit 3	-	BC3		RW			1
Bit 2	-	BC2		RW			1
Bit 1	-	BC1		RW			1
Bit 0	-	BC0		RW			1

I²C Table: WD Time Control Register

Byte 9	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	WDEN	Watchdog Enable	RW	Disable	Enable	0
Bit 6	-	WDSEN	Watchdog Soft Reset Enable	RW	Disable	Enable	0
Bit 5	-	WD Alarm Status	WD Alarm Status	R	Normal	Alarm	x
Bit 4	-	WD Soft Status	WD Soft Reset Status	R	Normal	Alarm	x
Bit 3	-	WDTCtrl	Watch Dog Time base Control	RW	290ms Base	1160ms Base	0
Bit 2	-	WD2	WD Timer Bit 2	RW	These bits represent X*290ms (or 1.16S) the watchdog timer waits before it goes to alarm mode. Default is 7 X 290ms = 2s.		1
Bit 1	-	WD1	WD Timer Bit 1	RW			1
Bit 0	-	WD0	WD Timer Bit 0	RW			1

I²C Table: M/N Programming & WD Safe Frequency Control Register

Byte 10	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	1
Bit 6	-	Reserved	Reserved	RW	-	-	1
Bit 5	-	WD Safe Freq Source	WD Safe Freq Source	RW	B10b(4:0)	Latch Inputs	0
Bit 4	-	WD SF4	Watch Dog Safe Freq Programming bits	RW	Writing to these bit will configure the safe frequency as Byte0 bit (4:0).		0
Bit 3	-	WD SF3		RW			0
Bit 2	-	WD SF2		RW			0
Bit 1	-	WD SF1		RW			0
Bit 0	-	WD SF0		RW			0

I²C Table: PLL1 Frequency Control Register

Byte 11	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div8	N Divider Prog bit 8	RW	The decimal representation of M and N Divier in Byte 11 and 12 will configure the PLL1 VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div9	N Divider Prog bit 9	RW			X
Bit 5	-	M Div5	M Divider Programming bits	RW			X
Bit 4	-	M Div4		RW			X
Bit 3	-	M Div3		RW			X
Bit 2	-	M Div2		RW			X
Bit 1	-	M Div1		RW			X
Bit 0	-	M Div0		RW			X

I²C Table: PLL1 Frequency Control Register

Byte 12	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div7	N Divider Programming b(7:0)	RW	The decimal representation of M and N Divier in Byte 11 and 12 will configure the PLL1 VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div6		RW			X
Bit 5	-	N Div5		RW			X
Bit 4	-	N Div4		RW			X
Bit 3	-	N Div3		RW			X
Bit 2	-	N Div2		RW			X
Bit 1	-	N Div1		RW			X
Bit 0	-	N Div0		RW			X

I²C Table: PLL1 Spread Spectrum Control Register

Byte 13	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SSP7	Spread Spectrum Programming b(7:0)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread pecentage of PLL1		X
Bit 6	-	SSP6		RW			X
Bit 5	-	SSP5		RW			X
Bit 4	-	SSP4		RW			X
Bit 3	-	SSP3		RW			X
Bit 2	-	SSP2		RW			X
Bit 1	-	SSP1		RW			X
Bit 0	-	SSP0		RW			X

I²C Table: PLL1 Spread Spectrum Control Register

Byte 14	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	R	-	-	0
Bit 6	-	SSP14	Spread Spectrum Programming b(14:8)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread pecentage of PLL1		X
Bit 5	-	SSP13		RW			X
Bit 4	-	SSP12		RW			X
Bit 3	-	SSP11		RW			X
Bit 2	-	SSP10		RW			X
Bit 1	-	SSP9		RW			X
Bit 0	-	SSP8		RW			X

I²C Table: Output Divider Control Register

Byte 15	Pin #	Name	Control Function	Type	0		1		PWD
Bit 7	-	CPUDiv3	CPU Divider Ratio Programmaing Bits	RW	0000:/2	0100:/4	1000:/8	1100:/16	X
Bit 6	-	CPUDiv2		RW	0001:/3	0101:/6	1001:/12	1101:/24	X
Bit 5	-	CPUDiv1		RW	0010:/5	0110:/10	1010:/20	1110:/40	X
Bit 4	-	CPUDiv0		RW	0011:/7	0111:/14	1011:/28	1111:/56	X
Bit 3	-	AGP/PCIDiv3	AGP/PCI Divider Ratio Programmaing Bits PLL2	RW	0000:/2	0100:/4	1000:/8	1100:/16	X
Bit 2	-	AGP/PCIDiv2		RW	0001:/3	0101:/6	1001:/12	1101:/24	X
Bit 1	-	AGP/PCIDiv1		RW	0010:/5	0110:/10	1010:/20	1110:/40	X
Bit 0	-	AGP/PCIDiv0		RW	0011:/7	0111:/14	1011:/28	1111:/56	X

I²C Table: Output Divider Control Register

Byte 16	Pin #	Name	Control Function	Type	0		1		PWD
Bit 7	-	Reserved	Reserved	RW	-		-		1
Bit 6	-	Reserved	Reserved	RW	-		-		1
Bit 5	-	Reserved	Reserved	RW	-		-		1
Bit 4	-	Reserved	Reserved	RW	-		-		1
Bit 3	-	AGP/PCIDiv3	AGP/PCI Divider Ratio Programmaing Bits PLL1	RW	0000:/4	0100:/8	1000:/16	1100:/32	X
Bit 2	-	AGP/PCIDiv2		RW	0001:/3	0101:/6	1001:/12	1101:/24	X
Bit 1	-	AGP/PCIDiv1		RW	0010:/5	0110:/10	1010:/20	1110:/40	X
Bit 0	-	AGP/PCIDiv0		RW	0011:/9	0111:/18	1011:/36	1111:/72	X

I²C Table: PLL2 Frequency Control Register

Byte 17	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div8	N Divider Prog bit 8	RW	The decimal representation of M and N Divier in Byte 17 and 18 will configure the PLL2 VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div9	N Divider Prog bit 9	RW			X
Bit 5	-	M Div5	M Divider Programming bits	RW			X
Bit 4	-	M Div4		RW			X
Bit 3	-	M Div3		RW			X
Bit 2	-	M Div2		RW			X
Bit 1	-	M Div1		RW			X
Bit 0	-	M Div0		RW			X

I²C Table: PLL2 Frequency Control Register

Byte 18	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div7	N Divider Programming b(7:0)	RW	The decimal representation of M and N Divier in Byte 17 and 18 will configure the PLL2 VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div6		RW			X
Bit 5	-	N Div5		RW			X
Bit 4	-	N Div4		RW			X
Bit 3	-	N Div3		RW			X
Bit 2	-	N Div2		RW			X
Bit 1	-	N Div1		RW			X
Bit 0	-	N Div0		RW			X

I²C Table: PLL2 Spread Spectrum Control Register

Byte 19	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SSP7	Spread Spectrum Programming b(7:0)	RW	These Spread Spectrum bits in Byte 19 and 20 will program the spread pecentage of PLL2		X
Bit 6	-	SSP6		RW			X
Bit 5	-	SSP5		RW			X
Bit 4	-	SSP4		RW			X
Bit 3	-	SSP3		RW			X
Bit 2	-	SSP2		RW			X
Bit 1	-	SSP1		RW			X
Bit 0	-	SSP0		RW			X

I²C Table: PLL2 Spread Spectrum Control Register

Byte 20	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	R	-	-	0
Bit 6	-	SSP14	Spread Spectrum Programming b(14:8)	RW	These Spread Spectrum bits in Byte 19 and 20 will program the spread pecentage of PLL2		X
Bit 5	-	SSP13		RW			X
Bit 4	-	SSP12		RW			X
Bit 3	-	SSP11		RW			X
Bit 2	-	SSP10		RW			X
Bit 1	-	SSP9		RW			X
Bit 0	-	SSP8		RW			X

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

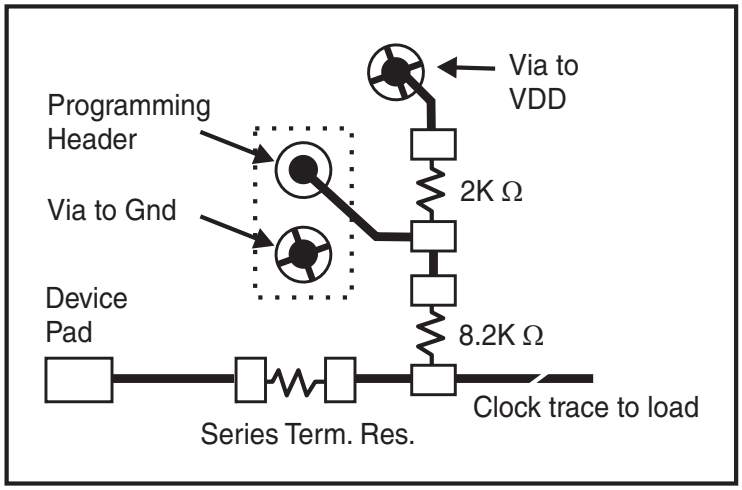


Fig. 1

Absolute Maximum Rating

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
3.3V Core Supply Voltage	VDD_A	-			V_{DD} + 0.5V	V	1
3.3V Logic Input Supply Voltage	VDD_In	-	GND - 0.5		V_{DD} + 0.5V	V	1
Storage Temperature	Ts	-	-65		150	˚C	1
Ambient Operating Temp	Tambient	-	0		70	°C	1
Case Temperature	Tcase	-			115	°C	1
Input ESD protection HBM	ESD prot	-	2000			V	1

[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	Notes
Input High Voltage	V_{IH}	3.3 V +/-5%	2		V_{DD} + 0.3	V	1
Input Low Voltage	V_{IL}	3.3 V +/-5%	V_{SS} - 0.3		0.8	V	1
Input High Current	I_{IH}	$V_{IN} = V_{DD}$	-5		5	uA	1
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			uA	1
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			uA	1
Low Threshold Input-High Voltage	V_{IH_FS}	3.3 V +/-5%	0.7		V_{DD} + 0.3	V	1
Low Threshold Input-Low Voltage	V_{IL_FS}	3.3 V +/-5%	V_{SS} - 0.3		0.35	V	1
Operating Supply Current	$I_{DD3.3OP}$	Full Active, C_L = Full load;			350	mA	1
Operating Current	$I_{DD3.3OP}$	all outputs driven			400	mA	1
Powerdown Current	$I_{DD3.3PD}$	all diff pairs driven			70	mA	1
		all differential pairs tri-stated			12	mA	1
Input Frequency	F_i	V_{DD} = 3.3 V		14.31818		MHz	2
Pin Inductance	L_{pin}				7	nH	1
Input Capacitance	C_{IN}	Logic Inputs			5	pF	1
	C_{OUT}	Output pin capacitance			6	pF	1
	C_{INX}	X1 & X2 pins			5	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} Power-Up or de-assertion of PD# to 1st clock			1.8	ms	1
Modulation Frequency		Triangular Modulation	30		33	kHz	1
Tdrive_PD#		CPU output enable after PD# de-assertion			300	us	1
Tfall_Pd#		PD# fall time of			5	ns	1
Trise_Pd#		PD# rise time of			5	ns	1
SMBus Voltage	V_{DD}		2.7		5.5	V	1
Low-level Output Voltage	V_{OL}	@ I_{PULLUP}			0.4	V	1
Current sinking at V_{OL} = 0.4 V	I_{PULLUP}		4			mA	1
SCLK/SDATA Clock/Data Rise Time	T_{RI2C}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Clock/Data Fall Time	T_{FI2C}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Input frequency should be measured at the REF pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.

Electrical Characteristics - CPUCLKT/C -- 0.7V Current Mode Differential Pair

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Current Source Output Impedance	Zo	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal	660		850	mV	1,3
Voltage Low	VLow		-150		150	mV	1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	Vuds		-300			mV	1
Crossing Voltage (abs)	Vx(abs)		250		550	mV	1
Crossing Voltage (var)	d-Vx	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Average period	Tperiod	400MHz nominal	2.4993		2.5008	ns	2
		400MHz spread	2.4993		2.5133	ns	2
		333.33MHz nominal	2.9991		3.0009	ns	2
		333.33MHz spread	2.9991		3.016	ns	2
		266.66MHz nominal	3.7489		3.7511	ns	2
		266.66MHz spread	3.7489		3.77	ns	2
		200MHz nominal	4.9985		5.0015	ns	2
		200MHz spread	4.9985		5.0266	ns	2
		166.66MHz nominal	5.9982		6.0018	ns	2
		166.66MHz spread	5.9982		6.0320	ns	2
		133.33MHz nominal	7.4978		7.5023	ns	2
		133.33MHz spread	7.4978		7.5400	ns	2
		100.00MHz nominal	9.9970		10.0030	ns	2
		100.00MHz spread	9.9970		10.0533	ns	2
Absolute min period	T_{absmin}	400MHz nominal/spread	2.4143			ns	1,2
		333.33MHz nominal/spread	2.9141			ns	1,2
		266.66MHz nominal/spread	3.6639			ns	1,2
		200MHz nominal/spread	4.8735			ns	1,2
		166.66MHz nominal/spread	5.8732			ns	1,2
		133.33MHz nominal/spread	7.3728			ns	1,2
		100.00MHz nominal/spread	9.8720			ns	1,2
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175		700	ps	1
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175		700	ps	1
Rise Time Variation	d-t_r	V_{OL} = 0.175V, V_{OH} = 0.525V			125	ps	1
Fall Time Variation	d-t_f	V_{OH} = 0.525V V_{OL} = 0.175V			125	ps	1
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45		55	%	1
Skew	t_{sk3}	CPU(1:0), V_T = 50%			100	ps	1
Skew	t_{sk4}	CPU(1:0) to CPU2_ITP, V_T = 50%			150	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	Measurement from differential wavefrom (CPU2_ITP)			125	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	Measurement from differential wavefrom, (CPU(1:0))			85	ps	1

*T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω, I_{REF} = 475Ω

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3]$I_{REF} = V_{DD}/(3xR_R)$. For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

Electrical Characteristics - SRC/SATA/PCIEX 0.7V Current Mode Differential Pair

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	Notes
Current Source Output Impedance	Zo	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal	660		850	mV	1,3
Voltage Low	VLow		-150		150	mV	1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	Vuds		-300			mV	1
Crossing Voltage (abs)	Vx(abs)		250		550	mV	1
Crossing Voltage (var)	d-Vx	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Average period	Tperiod	100.00MHz nominal	9.9970		10.0030	ns	2
		100.00MHz spread	9.9970		10.0533	ns	2
Absolute min period	Tabsmin	100.00MHz nominal/spread	9.8720			ns	1,2
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175		700	ps	1
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175		700	ps	1
Rise Time Variation	d-t_r	V_{OL} = 0.175V, V_{OH} = 0.525V			125	ps	1
Fall Time Variation	d-t_f	V_{OH} = 0.525V V_{OL} = 0.175V			125	ps	1
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45		55	%	1
Skew	t_{sk3}	V_T = 50%			250	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	Measurement from differential wavefrom			125	ps	1

*T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω, I_{REF} = 475Ω

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3]$I_{REF} = V_{DD}/(3xR_R)$. For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

Electrical Characteristics - PCICLK/PCICLK_F

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Output Impedance	R_{DSP}	$V_O = V_{DD}$*(0.5)	12		55	Ω	1
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-33			mA	1
		V_{OH}@MAX = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	30			mA	1
		V_{OL} @ MAX = 0.4 V			38	mA	1
Edge Rate	$t_{slewr/f}$	Rising/Falling edge rate	1		4	V/ns	1
Rise Time	t_r	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns	1
Fall Time	t_f	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Group Skew	t_{skew}	V_T = 1.5 V			500	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V			500	ps	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 20 pF with Rs = 7Ω (unless otherwise specified)

[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - 48MHz/USB48MHz/24_48MHz

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	1
Clock period	T_{period}	48.00MHz output nominal	20.8313		20.8354	ns	
Output Impedance	R_{DSP}	$V_O = V_{DD}*(0.5)$	12		55	Ω	1
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-33			mA	1
		V_{OH}@MAX = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	30			mA	1
		V_{OL} @ MAX = 0.4 V			38	mA	1
Edge Rate	$t_{slewr/f}$	Rising/Falling edge rate	1		4	V/ns	1
Edge Rate	t_{slewr/f_USB}	USB48 Rising/Falling edge rate	1		2	V/ns	1
Rise Time	t_r	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns	1
Fall Time	t_f	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns	1
Rise Time	t_{r_USB}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1		2	ns	1
Fall Time	t_{f_USB}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1		2	ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Group Skew	t_{skew}	V_T = 1.5 V			250	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V			500	ps	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 20 pF with Rs = 7Ω (Rs is used in USB48MHz test only)

[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - AGPCLK/3V66

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Output Impedance	R_{DSP}	$V_O = V_{DD}*(0.5)$	12		55	Ω	1
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-33			mA	1
		V_{OH}@MAX = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	30			mA	1
		V_{OL} @ MAX = 0.4 V			38	mA	1
Rise Time	t_r	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns	1
Fall Time	t_f	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Group Skew	t_{skew}	V_T = 1.5 V			150	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V			250	ps	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 10-30 pF (unless otherwise specified)

[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - REF-14.318MHz

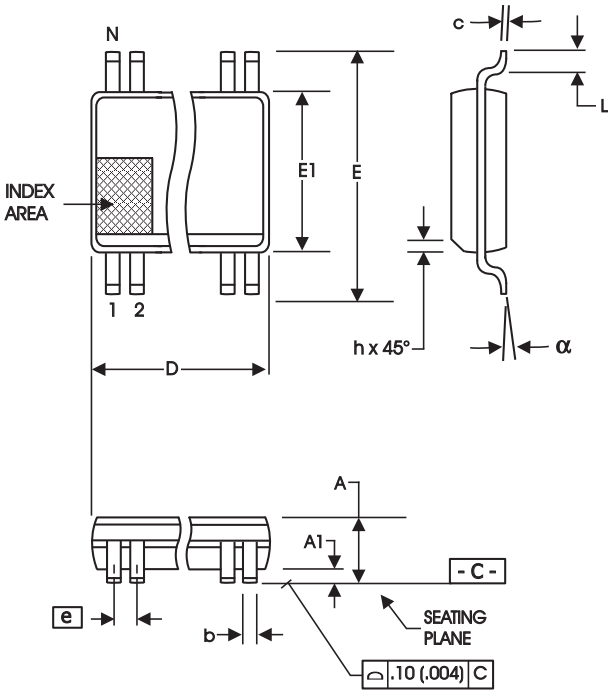
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Clock period	T_{period}	14.318MHz output nominal	69.8270		69.8550	ns	2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V, V_{OH}@MAX = 3.135 V	-29		-23	mA	1
Output Low Current	I_{OL}	V_{OL} @MIN = 1.95 V, V_{OL} @MAX = 0.4 V	29		27	mA	1
Edge Rate	$t_{slewr/f}$	Rising/Falling edge rate	1		4	V/ns	1
Rise Time	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1		2	ns	1
Fall Time	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1		2	ns	1
Skew	t_{sk1}	V_T = 1.5 V		Inverted		ps	3
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Jitter	$t_{jcyc-cyc}$	V_T = 1.5 V			1000	ps	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 20 pF with Rs = 7Ω (Rs is used in USB48MHz test only)

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3] The REF outputs are inverted with respect to each other. The exact skew value is not critical.



56-Lead, 300 mil Body, 25 mil, SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	18.31	18.55	.720	.730

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
953002CFLF	Tubes	56-pin SSOP	0 to +70° C
953002CFLFT	Tape and Reel	56-pin SSOP	0 to +70° C
953002DFLF	Tubes	56-pin SSOP	0 to +70° C
953002DFLFT	Tape and Reel	56-pin SSOP	0 to +70° C

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

0924—11/18/09

Revision History

Rev.	Issue Date	Description	Page #
0.1	6/13/2005	1. Updated frequency table. 2. Updated LF Ordering Information to RoHS Compliant.	1, 5-12, 25
0.2	9/1/2005	Updated frequency table	5-12
0.3	5/29/2008	Added SMBus Read/Write Information.	21
0.4	9/26/2008	Corrected typos on Bytes 15:20	25, 26, 27
A	6/11/2009	Moved to final.	
B	11/18/2009	Removed REF skew spec from DS. This spec is not required and is not critical functionality of the device or system. The REF outputs are inverted (180 degrees out of phase) with each other.	33

Notice

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