

DDR Phase Lock Loop Clock Driver (60MHz - 220MHz)

Recommended Application:

1:2 DDRI Clock Driver

Product Description/Features:

- Low skew, low jitter PLL clock driver
- Feedback pins for input to output synchronization
- Spread Spectrum tolerant inputs
- With bypass mode mux
- Operating frequency 60 to 220 MHz

Switching Characteristics:

- CYCLE - CYCLE jitter: <75ps
- OUTPUT - OUTPUT skew: <60ps
- Period jitter: ±75ps
- Half-Period jitter: ±75ps

Pin Configuration

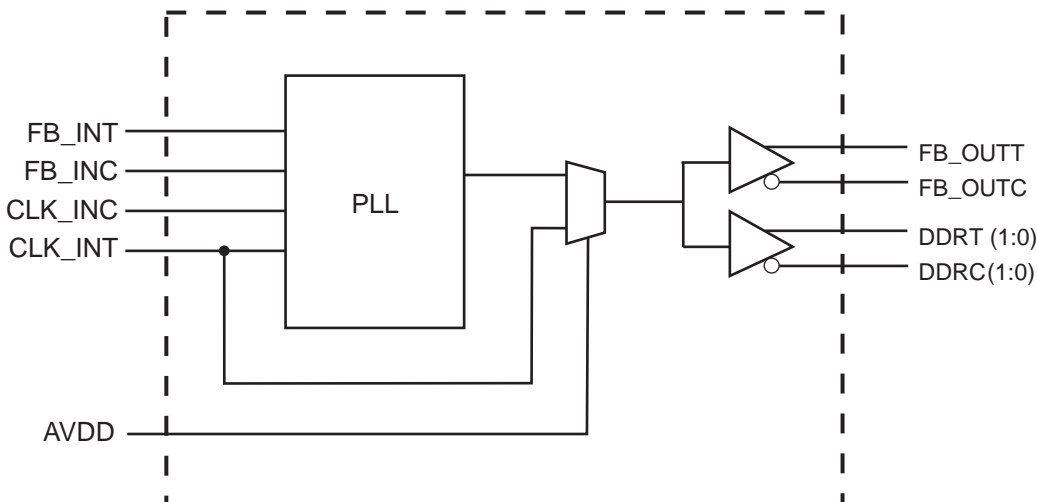
| | | | | |
|---------|---|-----------|----|---------|
| VDD2.5 | 1 | ICS95V842 | 16 | GND |
| DDRT0 | 2 | | 15 | DDRC1 |
| DDRC0 | 3 | | 14 | DDRT1 |
| GND | 4 | | 13 | VDD2.5 |
| CLK_INT | 5 | | 12 | FB_INC |
| CLK_INC | 6 | | 11 | FB_INT |
| AVDD | 7 | | 10 | FB_OUTT |
| AGND | 8 | | 9 | FB_OUTC |

16 pin SSOP

Functionality

| INPUTS | | | OUTPUTS | | | | PLL State |
|------------|---------|---------|---------|------|---------|---------|--------------|
| AVDD | CLK_INT | CLK_INC | CLKT | CLKC | FB_OUTT | FB_OUTC | |
| GND | L | H | L | H | L | H | Bypassed/Off |
| GND | H | L | H | L | H | L | Bypassed/Off |
| 2.5V (nom) | L | H | L | H | L | H | On |
| 2.5V (nom) | H | L | H | L | H | L | On |

Block Diagram



Pin Descriptions

| PIN # | PIN NAME | PIN TYPE | DESCRIPTION |
|-------|----------|----------|--|
| 1 | VDD2.5 | PWR | Power supply, nominal 2.5V |
| 2 | DDRT0 | OUT | "True" Clock of differential pair output. |
| 3 | DDRC0 | OUT | "Complementary" Clock of differential pair output. |
| 4 | GND | PWR | Ground pin. |
| 5 | CLK_INT | IN | "True" reference clock input. |
| 6 | CLK_INC | IN | "Complementary" reference clock input. |
| 7 | AVDD | PWR | 3.3V Analog Power pin for Core PLL |
| 8 | AGND | PWR | Analog Ground pin for Core PLL |
| 9 | FB_OUTC | OUT | Complement single-ended feedback output, dedicated external feedback. It switches at the same frequency as other DDR outputs, This output must be connect to FB_INC. |
| 10 | FB_OUTT | OUT | True single-ended feedback output, dedicated external feedback. It switches at the same frequency as other DDR outputs, This output must be connect to FB_INT. |
| 11 | FB_INT | IN | True single-ended feedback input, provides feedback signal to internal PLL for synchronization with CLK_INT to eliminate phase error. |
| 12 | FB_INC | IN | Complement single-ended feedback input, provides feedback signal to internal PLL for synchronization with CLK_INT to eliminate phase error. |
| 13 | VDD2.5 | PWR | Power supply, nominal 2.5V |
| 14 | DDRT1 | OUT | "True" Clock of differential pair output. |
| 15 | DDRC1 | OUT | "Complementary" Clock of differential pair output. |
| 16 | GND | PWR | Ground pin. |

Absolute Maximum Ratings

Supply Voltage: (VDD & AVDD) -0.5V to 3.6V
 Input clamp current: I_{IK} ($V_I < 0$ or $V_I > V_{DD}$) +/- 50mA
 Output clamp current: I_{OK} ($V_O < 0$ or $V_O > V_{DD}$) . . +/- 50mA
 Continuous output current: I_O ($V_O = 0$ to V_{DD}) +/- 50mA
 Package thermal impedance, theta JA: DGG package +89°C/Ω
 Storage Temperature -65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

TA = 0°C to +85°C; Supply Voltage AVDD, VDD = 2.5 V +/- 0.2V (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------------|-------------|--|----------------|-----|------|-------|
| Input High Current | I_{IH} | $V_I = V_{DD}$ or GND | 5 | | | μA |
| Input Low Current | I_{IL} | $V_I = V_{DD}$ or GND | | | 5 | μA |
| Operating Supply Current | $I_{DD2.5}$ | $C_L = 0pF, R_L = \infty\Omega$ | | | 160 | mA |
| | I_{DDPD} | $C_L = 0pF, R_L = \infty\Omega$ | | | 100 | μA |
| Output High Current | I_{OH} | $V_{DD} = 2.3V, V_{OUT} = 1V$ | -18 | | | mA |
| Output Low Current | I_{OL} | $V_{DD} = 2.3V, V_{OUT} = 1.2V$ | 26 | | | mA |
| High Impedance Output Current | I_{OZ} | $V_{DD}=2.7V, V_{out}=V_{DD}$ or GND | | | ±10 | μA |
| Input Clamp Voltage | V_{IK} | $I_{in} = -18mA$ | | | -1.2 | V |
| High-level output voltage | V_{OH} | $V_{DD} = \text{min to max}, I_{OH} = -1 \text{ mA}$ | $V_{DD} - 0.1$ | | | V |
| | | $V_{DD} = 2.3V, I_{OH} = -12 \text{ mA}$ | 1.7 | | | V |
| Low-level output voltage | V_{OL} | $V_{DD} = \text{min to max}, I_{OL}=1 \text{ mA}$ | | | 0.1 | |
| | | $V_{DD} = 2.3V, I_{OH}=12 \text{ mA}$ | | | 0.6 | V |
| Input Capacitance ¹ | C_{IN} | $V_I = V_{DD}$ or GND | | 3 | | pF |
| Output Capacitance ¹ | C_{OUT} | $V_I = V_{DD}$ or GND | | 3 | | pF |

¹Guaranteed by design and characterization, not 100% tested in production.

DC Electrical Characteristics

TA = 0°C to +85°C; Supply Voltage AVDD, VDD = 2.5 V +/- 0.2V (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-------------------------------------|----------------------------------|---------------------------|--------------------|---------------------------|-------|
| Supply Voltage | V _{DDQ} , A _{VDD} | | 2.3 | 2.5 | 2.7 | V |
| Low level input voltage | V _{IL} | CLK_INT, CLK_INC, FB_INC, FB_INT | | 0.4 | V _{DD} /2 - 0.18 | V |
| High level input voltage | V _{IH} | CLK_INT, CLK_INC, FB_INC, FB_INT | V _{DD} /2 + 0.18 | 2.1 | | V |
| DC input signal voltage (note 1,2) | V _{IN} | | -0.3 | | V _{DD} + 0.3 | V |
| Differential input signal voltage (note 3) | V _{ID} | CLK_INT, CLK_INC, FB_INC, FB_INT | 0.36 | | V _{DD} + 0.6 | V |
| Differential output voltage (note 3) | V _{OD} | CLK_INT, CLK_INC, FB_INC, FB_INT | 0.7 | | V _{DD} + 0.6 | V |
| Output differential cross-voltage (note 4) | V _{OX} | | V _{DD} /2 - 0.15 | | V _{DD} /2 + 0.15 | V |
| Input differential cross-voltage (note 4) | V _{IX} | | V _{DD} /2 - 0.2 | V _{DD} /2 | V _{DD} /2 + 0.2 | V |
| Operating free-air temperature | T _A | | 0 | | 85 | °C |

Notes:

- 1 Unused inputs must be held high or low to prevent them from floating.
- 2 DC input signal voltage specifies the allowable DC excursion of differential input.
- 3 Differential input signal voltage specifies the differential voltage [VTR-VCP] required for switching, where VTR is the true input level and VCP is the complementary input level.
- 4 Differential cross-point voltage is expected to track variations of VDD and is the voltage at which the differential signal must be crossing.

Timing Requirements

TA = 0°C to +85°C; Supply Voltage AVDD, VDD = 2.5 V +/- 0.2V (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS |
|--|---------------------|------------|-----|-----|-------|
| Max clock frequency ³ | freq _{op} | | 33 | 233 | MHz |
| Application Frequency Range ³ | freq _{App} | | 60 | 220 | MHz |
| Input clock duty cycle | d _{tin} | | 40 | 60 | % |
| CLK stabilization | T _{STAB} | | | 100 | µs |

Switching Characteristics

$T_A = 0^\circ\text{C}$ to $+85^\circ\text{C}$; Supply Voltage AVDD, VDD = 2.5 V +/- 0.2V (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITION | MIN | TYP | MAX | UNITS |
|--|-----------------------------------|--------------------------------------|-----|-----|-----|---------------|
| Max clock frequency ³ | freq_{op} | | 40 | | 333 | MHz |
| Application Frequency Range ³ | freq_{App} | | 60 | | 220 | MHz |
| Input clock duty cycle | d_{tin} | | 40 | | 60 | % |
| Input clock slew rate | $t_{\text{sl(l)}}$ | | 1 | | 2 | v/ns |
| CLK stabilization | T_{STAB} | | | | 100 | μs |
| Low-to-high level propagation delay time | t_{PLH}^1 | CLK_IN to any output | | | 5.5 | ns |
| High-to-low level propagation delay time | t_{PHL}^1 | CLK_IN to any output | | | 5.5 | ns |
| Output enable time | t_{en} | PD# to any output | | 5 | | ns |
| Output disable time | t_{dis} | PD# to any output | | 5 | | ns |
| Period jitter | $t_{\text{jit(per)}}$ | Over the application frequency range | -75 | | 75 | ps |
| Half-period jitter | $t_{\text{jit(hper)}}$ | | -75 | | 75 | ps |
| Output clock slew rate | $t_{\text{sl(o)}}$ | | 1 | | 2.5 | v/ns |
| Cycle to Cycle Jitter | $t_{\text{cyc}} - t_{\text{cyc}}$ | | -75 | | 75 | ps |
| Static Phase Offset | $t_{\text{(spo)}}$ | | -50 | | 50 | ps |
| Output to Output Skew | t_{skew} | | | 40 | 60 | ps |

Notes:

1. Refers to transition on noninverting output in PLL bypass mode.
2. While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies. This is due to the formula: $\text{duty cycle} = \frac{t_{\text{wH}}}{t_{\text{c}}}$, where the cycle (t_{c}) decreases as the frequency goes up.
3. Switching characteristics are guaranteed for application frequency range. The PLL Locks over the Max Clock Frequency range, but the device does not necessarily meet other timing parameters.
4. Does not include jitter.

Parameter Measurement Information

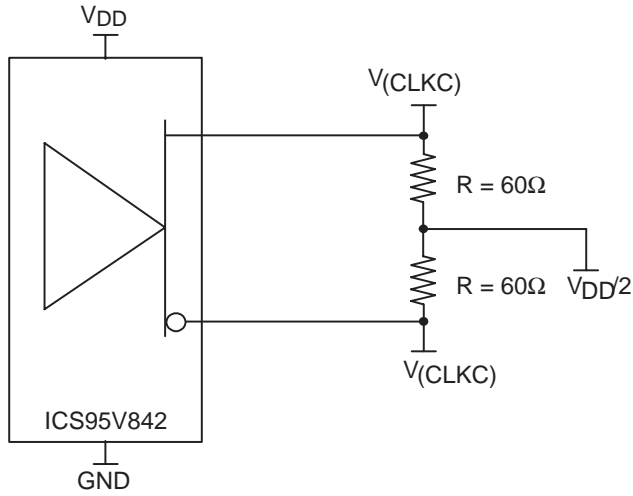


Figure 1. IBIS Model Output Load

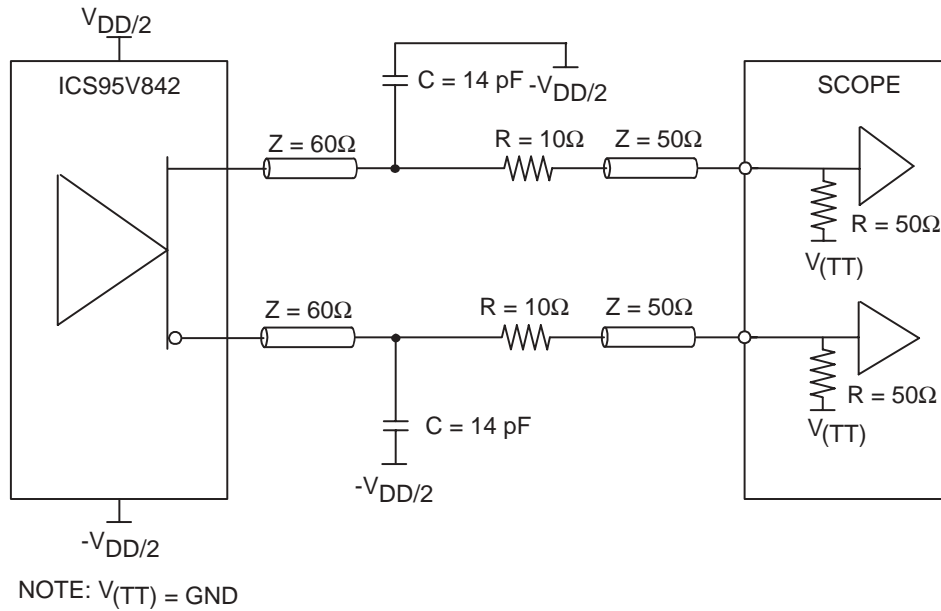


Figure 2. Output Load Test Circuit

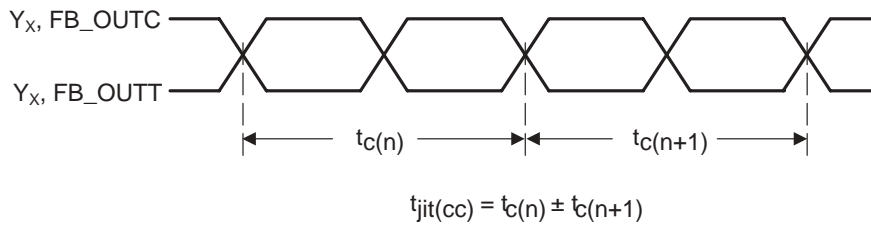


Figure 3. Cycle-to-Cycle Jitter

Parameter Measurement Information

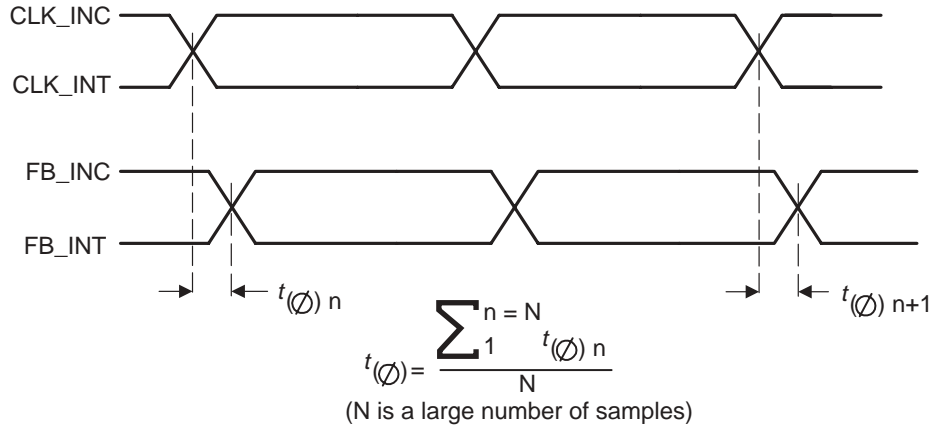


Figure 4. Static Phase Offset

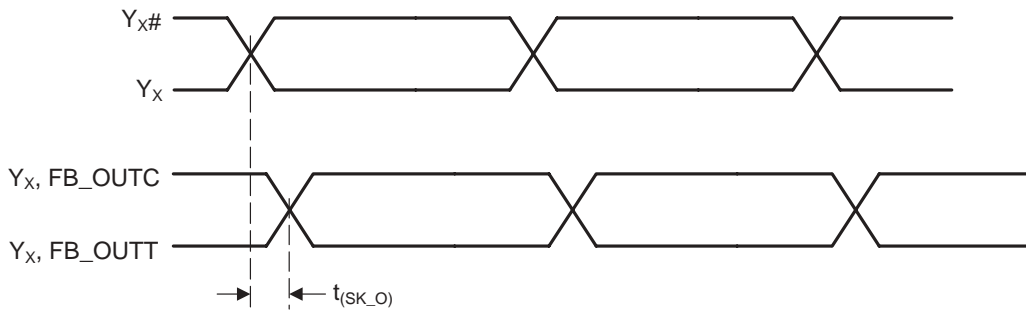


Figure 5. Output Skew

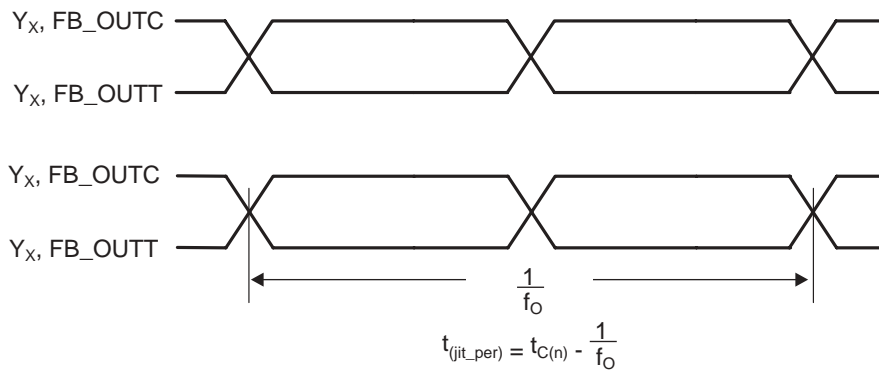


Figure 6. Period Jitter

Parameter Measurement Information

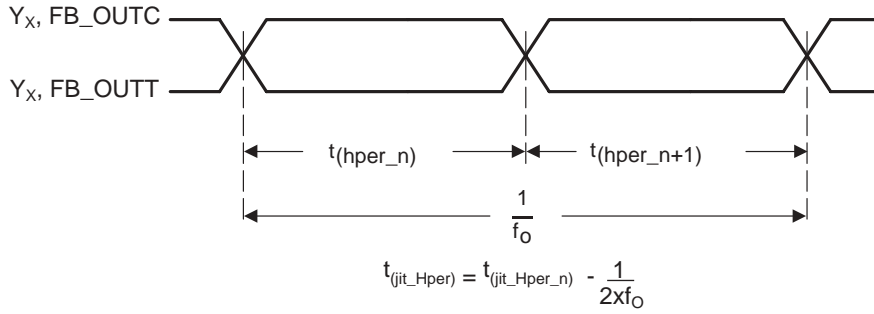


Figure 7. Half-Period Jitter

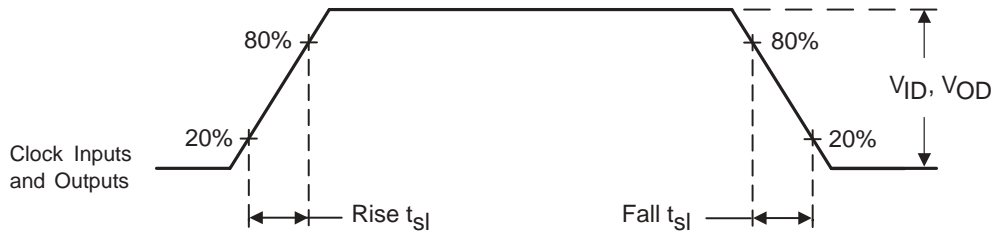
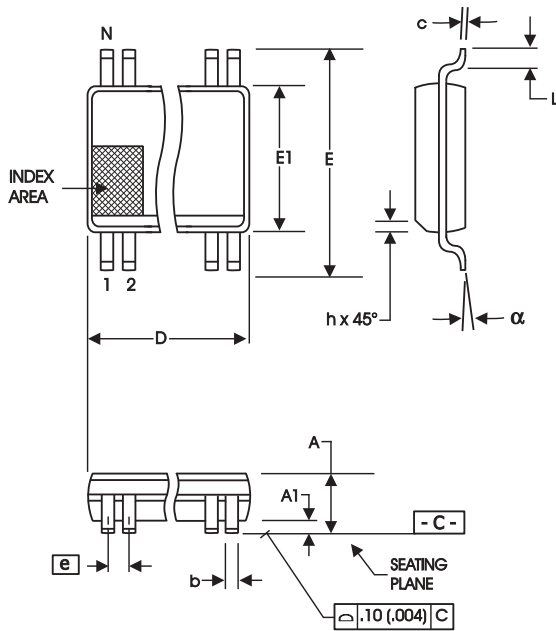


Figure 8. Input and Output Slew Rates



16-Lead, 150 mil SSOP (QSOP)

| SYMBOL | In Millimeters | | In Inches | |
|--------|-------------------|-------------------|-------------------|-------------------|
| | COMMON DIMENSIONS | COMMON DIMENSIONS | COMMON DIMENSIONS | COMMON DIMENSIONS |
| A | 1.35 | 1.75 | .053 | .069 |
| A1 | 0.10 | 0.25 | .004 | .010 |
| A2 | -- | 1.50 | -- | .059 |
| b | 0.20 | 0.30 | .008 | .012 |
| c | 0.18 | 0.25 | .007 | .010 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 5.80 | 6.20 | .228 | .244 |
| E1 | 3.80 | 4.00 | .150 | .157 |
| e | 0.635 BASIC | | 0.025 BASIC | |
| L | 0.40 | 1.27 | .016 | .050 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| a | 0° | 8° | 0° | 8° |
| ZD | SEE VARIATIONS | | SEE VARIATIONS | |

VARIATIONS

| N | D mm. | | ZD (Ref) | D (inch) | | ZD (Ref) |
|----|-------|------|-------------|----------|------|-------------|
| | MIN | MAX | | MIN | MAX | |
| 16 | 4.80 | 5.00 | 0.23 | .189 | .197 | .009 |

Reference Doc.: JEDEC Publication 95, MO-137

10-0032

Ordering Information

95V842yFzLF-T

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