

4-OUTPUT VERY LOW POWER PCIE GEN 1–4 CLOCK GENERATOR
9FGV0441
Description

The 9FGV0441 is an 4-output very low power clock generator for PCIe Gen 1, 2, 3 and 4 applications with integrated output terminations providing $Z_o = 100\Omega$. The device has 4 output enables for clock management and supports 2 different spread spectrum levels in addition to spread off.

Recommended Application

PCIe Gen1–4 clock generation for Riser Cards, Storage, Networking, JBOD, Communications, Access Points

Output Features

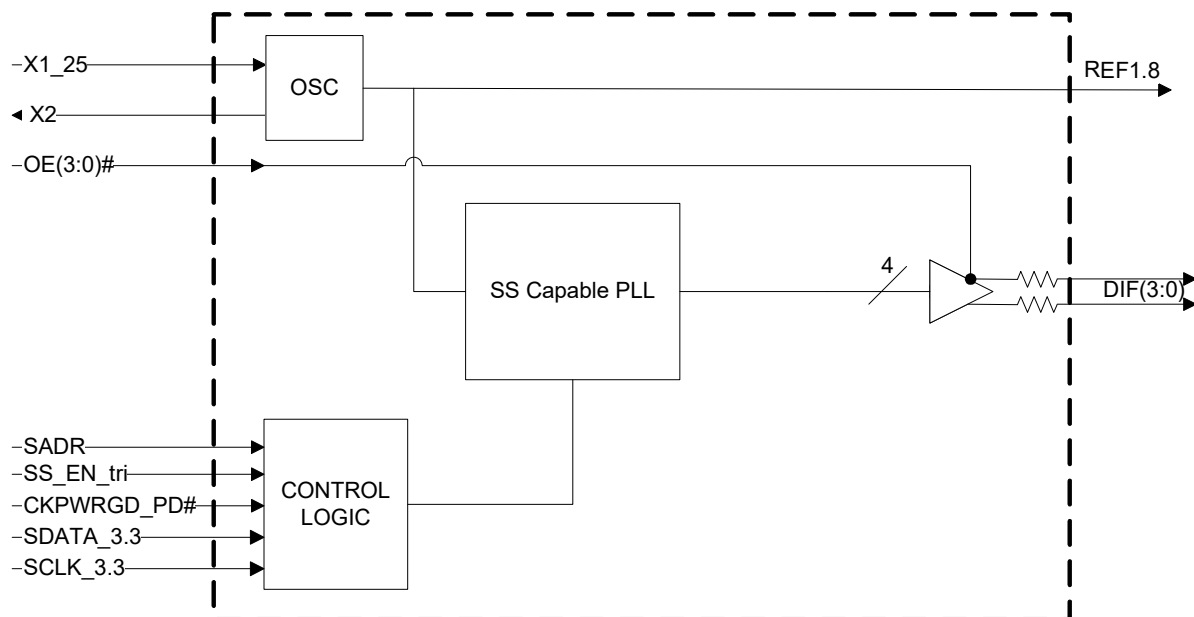
- 4 0.7V low-power HCSL-compatible (LP-HCSL) DIF pairs with $Z_o=100\Omega$
- 1 1.8V LVCMOS REF output with Wake-On-Lan (WOL) support

Key Specifications

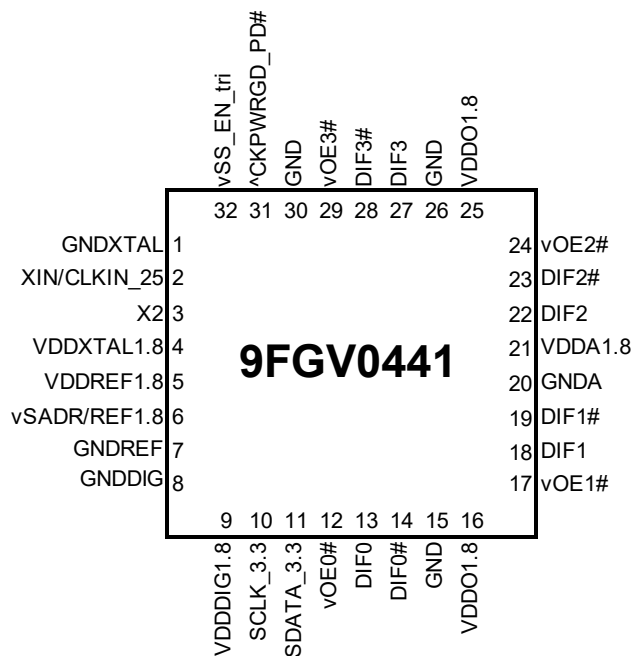
- DIF cycle-to-cycle jitter < 50ps
- DIF output-to-output skew < 50ps
- DIF phase jitter is PCIe Gen1–4 compliant
- REF phase jitter is < 1.5ps RMS

Features/Benefits

- Integrated terminations provide 100Ω differential Z_o ; reduced component count and board space
- 1.8V operation; reduced power consumption
- OE# pins; support DIF power management
- LP-HCSL differential clock outputs; reduced power and board space
- Programmable slew rate for each output; allows tuning for various line lengths
- Programmable output amplitude; allows tuning for various application environments
- DIF outputs blocked until PLL is locked; clean system start-up
- Selectable 0%, -0.25% or -0.5% spread on DIF outputs; reduces EMI
- External 25MHz crystal; supports tight ppm with 0 ppm synthesis error
- Configuration can be accomplished with strapping pins; SMBus interface not required for device control
- 3.3V tolerant SMBus interface works with legacy controllers
- Space saving 5 x 5 mm 32-VFQFPN; minimal board space
- Selectable SMBus addresses; multiple devices can easily share an SMBus segment

Block Diagram


Pin Configuration



32-VFQFPN, 5 x 5 mm, 0.5mm pitch

^ prefix indicates internal 120kOhm pull-up resistor
v prefix indicates internal 120kOhm pull down-resistor

SMBus Address Selection Table

| | SADR | Address | + Read/Write Bit |
|---|------|---------|------------------|
| State of SADR on first application of CKPWRGD_PD# | 0 | 1101000 | x |
| | 1 | 1101010 | x |

Power Management Table

| CKPWRGD_PD# | SMBus OE bit | DIFx | | | REF |
|-------------|--------------|------|----------|-----------|-------------------|
| | | OEx# | True O/P | Comp. O/P | |
| 0 | X | X | Low | Low | Hi-Z ¹ |
| 1 | 1 | 0 | Running | Running | Running |
| 1 | 0 | 1 | Low | Low | Low |

1. REF is Hi-Z until the 1st assertion of CKPWRGD_PD# high. After this, when CKPWRG_PD# is low, REF is Low.

Power Connections

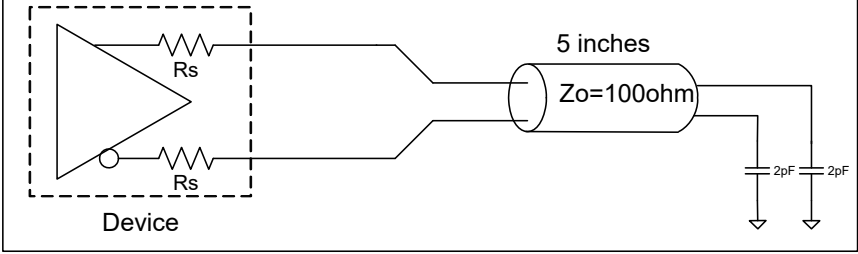
| Pin Number | VDD | GND | Description |
|------------|-----|--------|---------------|
| 4 | | 1 | XTAL Analog |
| 5 | | 7 | REF Output |
| 9 | | 8, 30 | Digital Power |
| 16, 25 | | 15, 26 | DIF outputs |
| 21 | | 20 | PLL Analog |

Pin Descriptions

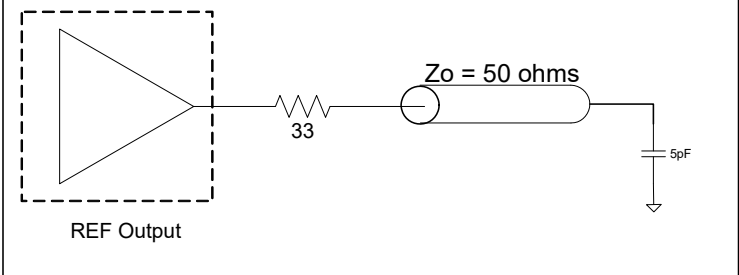
| Pin# | Pin Name | Type | Pin Description |
|------|--------------|-------------|---|
| 1 | GNDXTAL | GND | GND for XTAL |
| 2 | XIN/CLKIN_25 | IN | Crystal input or Reference Clock input. Nominally 25MHz. |
| 3 | X2 | OUT | Crystal output. |
| 4 | VDDXTAL1.8 | PWR | Power supply for XTAL, nominal 1.8V |
| 5 | VDDREF1.8 | PWR | VDD for REF output. nominal 1.8V. |
| 6 | vSADR/REF1.8 | LATCHED I/O | Latch to select SMBus Address/1.8V LVCMOS copy of X1 pin. |
| 7 | GNDREF | GND | Ground pin for the REF outputs. |
| 8 | GNDDIG | GND | Ground pin for digital circuitry |
| 9 | VDDDIG1.8 | PWR | 1.8V digital power (dirty power) |
| 10 | SCLK_3.3 | IN | Clock pin of SMBus circuitry, 3.3V tolerant. |
| 11 | SDATA_3.3 | I/O | Data pin for SMBus circuitry, 3.3V tolerant. |
| 12 | vOE0# | IN | Active low input for enabling DIF pair 0. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 13 | DIF0 | OUT | Differential true clock output |
| 14 | DIF0# | OUT | Differential Complementary clock output |
| 15 | GND | GND | Ground pin. |
| 16 | VDDO1.8 | PWR | Power supply for outputs, nominally 1.8V. |
| 17 | vOE1# | IN | Active low input for enabling DIF pair 1. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 18 | DIF1 | OUT | Differential true clock output |
| 19 | DIF1# | OUT | Differential Complementary clock output |
| 20 | GNDA | GND | Ground pin for the PLL core. |
| 21 | VDDA1.8 | PWR | 1.8V power for the PLL core. |
| 22 | DIF2 | OUT | Differential true clock output |
| 23 | DIF2# | OUT | Differential Complementary clock output |
| 24 | vOE2# | IN | Active low input for enabling DIF pair 2. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 25 | VDDO1.8 | PWR | Power supply for outputs, nominally 1.8V. |
| 26 | GND | GND | Ground pin. |
| 27 | DIF3 | OUT | Differential true clock output |
| 28 | DIF3# | OUT | Differential Complementary clock output |
| 29 | vOE3# | IN | Active low input for enabling DIF pair 3. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 30 | GND | GND | Ground pin. |
| 31 | ^CKPWRGD_PD# | IN | Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor. |
| 32 | vSS_EN_tri | LATCHED IN | Latched select input to select spread spectrum amount at initial power up : 1 = -0.5% spread, M = -0.25%, 0 = Spread Off |

Test Loads

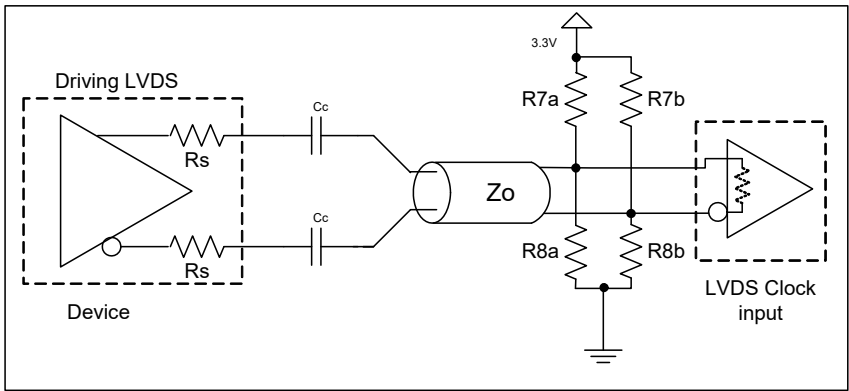
Low-Power HCSL Differential Output Test Load



REF Output Test Load



Alternate Terminations



Driving LVDS inputs with the 9FGV0441

| Component | Value | | Note |
|-----------|--------------------------|------------------------------------|------|
| | Receiver has termination | Receiver does not have termination | |
| R7a, R7b | 10K ohm | 140 ohm | |
| R8a, R8b | 5.6K ohm | 75 ohm | |
| Cc | 0.1 uF | 0.1 uF | |
| Vcm | 1.2 volts | 1.2 volts | |

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9FGV0441. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---------------------------|--------------------|---------------------------|------|-----|-----------------------|-------|-------|
| 1.8V Supply Voltage | VDDx1.8 | Applies to All VDD pins | -0.5 | | 2.5 | V | 1,2 |
| Input Voltage | V _{IN} | | -0.5 | | V _{DD} +0.3V | V | 1, 3 |
| Input High Voltage, SMBus | V _{IHSMB} | SMBus clock and data pins | | | 3.6V | V | 1 |
| Storage Temperature | T _s | | -65 | | 150 | °C | 1 |
| Junction Temperature | T _j | | | | 125 | °C | 1 |
| Input ESD protection | ESD prot | Human Body Model | 2000 | | | V | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Operation under these conditions is neither implied nor guaranteed.

³Not to exceed 2.5V.

Electrical Characteristics–Current Consumption

TA = T_{COM} or T_{IND}; Supply Voltage per VDD of normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|--------------------------|---------------------|--------------------------------------|-----|-----|-----|-------|-------|
| Operating Supply Current | I _{DDAOP} | VDDA, All outputs active @100MHz | | 6 | 8 | mA | 1 |
| | I _{DDOP} | VDD, All outputs active @100MHz | | 26 | 30 | mA | 1 |
| Suspend Supply Current | I _{DDSUSP} | VDDxxx, PD# = 0, Wake-On-LAN enabled | | 6 | 8 | mA | 1 |
| Powerdown Current | I _{DDPD} | PD#=0 | | 0.6 | 1 | mA | 1, 2 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Assuming REF is not running in power down state

Electrical Characteristics–Output Duty Cycle, Jitter, and Skew Characteristics

TA = T_{COM} or T_{IND}; Supply Voltage per VDD of normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|----------------------|-----------------------------------|-----|-----|-----|-------|-------|
| Duty Cycle | t _{DC} | Measured differentially, PLL Mode | 45 | 50 | 55 | % | 1 |
| Skew, Output to Output | t _{sk3} | V _T = 50% | | 34 | 50 | ps | 1 |
| Jitter, Cycle to cycle | t _{jcy-cyc} | PLL mode | | 14 | 50 | ps | 1,2 |

¹Guaranteed by design and characterization, not 100% tested in production.

² Measured from differential waveform

Electrical Characteristics–Input/Supply/Common Parameters–Normal Operating Conditions

TA = T_{COM} or T_{IND}; Supply Voltage per VDD of normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|--|---------------------|---|-----------------------|------|-----------------------|--------|-------|
| 1.8V Supply Voltage | VDD _{x1.8} | Supply voltage for core, analog and single-ended LVCMOS outputs | 1.7 | 1.8 | 1.9 | V | 1 |
| Ambient Operating Temperature | T _{IND} | Industrial range | -40 | 25 | 85 | °C | 1 |
| Input High Voltage | V _{IH} | Single-ended inputs, except SMBus | 0.75 V _{DD} | | V _{DD} + 0.3 | V | 1 |
| Input Mid Voltage | V _{IM} | Single-ended tri-level inputs ('_tri' suffix, if present) | 0.4 V _{DD} | | 0.6 V _{DD} | V | 1 |
| Input Low Voltage | V _{IL} | Single-ended inputs, except SMBus | -0.3 | | 0.25 V _{DD} | V | 1 |
| Schmitt Trigger Positive Going Threshold Voltage | V _{T+} | Single-ended inputs, where indicated | 0.4 V _{DD} | | 0.7 V _{DD} | V | 1 |
| Schmitt Trigger Negative Going Threshold Voltage | V _{T-} | Single-ended inputs, where indicated | 0.1 V _{DD} | | 0.4 V _{DD} | V | 1 |
| Hysteresis Voltage | V _H | V _{T+} - V _{T-} | 0.1 V _{DD} | | 0.4 V _{DD} | V | 1 |
| Output High Voltage | V _{IH} | Single-ended outputs, except SMBus. I _{OH} = -2mA | V _{DD} -0.45 | | | V | 1 |
| Output Low Voltage | V _{IL} | Single-ended outputs, except SMBus. I _{OL} = -2mA | | | 0.45 | V | 1 |
| Input Current | I _{IN} | Single-ended inputs, V _{IN} = GND, V _{IN} = VDD | -5 | | 5 | uA | 1 |
| | I _{INP} | Single-ended inputs V _{IN} = 0 V; Inputs with internal pull-up resistors V _{IN} = VDD; Inputs with internal pull-down resistors | -20 | | 20 | uA | 1 |
| Input Frequency | F _{in} | XTAL, or X1 input | 23 | 25 | 27 | MHz | 1 |
| Pin Inductance | L _{pin} | | | | 7 | nH | 1 |
| Capacitance | C _{IN} | Logic Inputs, except DIF_IN | 1.5 | | 5 | pF | 1 |
| | C _{OUT} | Output pin capacitance | | | 6 | pF | 1 |
| Clk Stabilization | T _{STAB} | From V _{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock | | 0.6 | 1.8 | ms | 1,2 |
| SS Modulation Frequency | f _{MOD} | Allowable Frequency (Triangular Modulation) | 31 | 31.6 | 32 | kHz | 1 |
| OE# Latency | t _{LATOE#} | DIF start after OE# assertion DIF stop after OE# deassertion | 2 | 3 | 4 | clocks | 1,3 |
| Tdrive_PD# | t _{DRVPD} | DIF output enable after PD# de-assertion | | 4 | 300 | us | 1,3 |
| Tfall | t _F | Fall time of single-ended control inputs | | | 5 | ns | 1,2 |
| Trise | t _R | Rise time of single-ended control inputs | | | 5 | ns | 1,2 |
| SMBus Input Low Voltage | V _{ILSMB} | V _{DD} SMB = 3.3V, see note 4 for V _{DD} SMB < 3.3V | | | 0.8 | V | 1,4 |
| SMBus Input High Voltage | V _{IHSMB} | V _{DD} SMB = 3.3V, see note 5 for V _{DD} SMB < 3.3V | 2.1 | | 3.6 | V | 1,5 |
| SMBus Output Low Voltage | V _{OLSMB} | @ I _{PULLUP} | | | 0.4 | V | 1 |
| SMBus Sink Current | I _{PULLUP} | @ V _{OL} | 4 | | | mA | 1 |
| Nominal Bus Voltage | V _{DD} SMB | | 1.7 | | 3.6 | V | 1 |
| SCLK/SDATA Rise Time | t _{RSMB} | (Max V _{IL} - 0.15) to (Min V _{IH} + 0.15) | | | 1000 | ns | 1 |
| SCLK/SDATA Fall Time | t _{FSMB} | (Min V _{IH} + 0.15) to (Max V _{IL} - 0.15) | | | 300 | ns | 1 |
| SMBus Operating Frequency | f _{MAXSMB} | Maximum SMBus operating frequency | | | 400 | kHz | 1 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Control input must be monotonic from 20% to 80% of input swing.

³ Time from deassertion until outputs are > 200mV.

⁴ For V_{DD}SMB < 3.3V, V_{ILSMB} ≤ 0.35V_{DD}SMB.

⁵ For V_{DD}SMB < 3.3V, V_{IHSMB} ≥ 0.65V_{DD}SMB.

Electrical Characteristics–DIF 0.7V Low Power HCSL Outputs

$T_A = T_{COM}$ or T_{IND} ; supply voltage per VDD of normal operation conditions; see Test Loads for loading conditions.

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|--------------------|---|------|------|------|-------|---------|
| Slew Rate | Trf | Scope averaging on 3.0V/ns setting. | 2.3 | 3.1 | 4 | V/ns | 1, 2, 3 |
| | | Scope averaging on 2.0V/ns setting. | 1.6 | 2.3 | 3.3 | V/ns | 1, 2, 3 |
| Slew Rate Matching | ΔT_{rf} | Single-ended measurement. | | 3 | 20 | % | 1, 4 |
| Voltage High | V_{HIGH} | Statistical measurement on single-ended signal using oscilloscope math function (scope averaging on). | 660 | 794 | 850 | mV | 1, 7 |
| Voltage Low | V_{LOW} | | -150 | 21 | 150 | | 1 |
| Max Voltage | Vmax | Measurement on single-ended signal using absolute value (scope averaging off). | | 816 | 1150 | mV | 1 |
| Min Voltage | Vmin | | -300 | -15 | | | 1 |
| Vswing | Vswing | Scope averaging off. | 300 | 1551 | | mV | 1, 2 |
| Crossing Voltage (abs) | Vcross_abs | Scope averaging off. | 300 | 397 | 550 | mV | 1, 5 |
| Crossing Voltage (var) | ΔV_{cross} | Scope averaging off. | | 15 | 140 | mV | 1, 6 |

¹Guaranteed by design and characterization, not 100% tested in production.

² Measured from differential waveform.

³ Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

⁴ Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

⁵ Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

⁶ The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting ΔV_{cross} to be smaller than Vcross absolute.

⁷ At default SMBus settings.

Electrical Characteristics–Filtered Phase Jitter Parameters - PCIe Common Clocked (CC) Architectures

T_{AMB} = over the specified operating range. Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | Specification Limit | UNITS | NOTES |
|--------------------|------------------------|--|-----|------|------|---------------------|----------|---------|
| $t_{jphPCIeG1-CC}$ | Phase Jitter, PLL Mode | PCIe Gen 1 | 21 | 25 | 35 | 86 | ps (p-p) | 1, 2, 3 |
| $t_{jphPCIeG2-CC}$ | | PCIe Gen 2 Low Band 10kHz < f < 1.5MHz (PLL BW of 5-16MHz, 8-16MHz, CDR = 5MHz) | 0.9 | 0.9 | 1.1 | 3 | ps (rms) | 1, 2 |
| | | PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5-16MHz, 8-16MHz, CDR = 5MHz) | 1.5 | 1.6 | 1.9 | 3.1 | ps (rms) | 1, 2 |
| $t_{jphPCIeG3-CC}$ | | PCIe Gen 3 (PLL BW of 2-4MHz, 2-5MHz, CDR = 10MHz) | 0.3 | 0.37 | 0.44 | 1 | ps (rms) | 1, 2 |
| $t_{jphPCIeG4-CC}$ | | PCIe Gen 4 (PLL BW of 2-4MHz, 2-5MHz, CDR = 10MHz) | 0.3 | 0.37 | 0.44 | 0.5 | ps (rms) | 1, 2 |

Notes on PCIe Filtered Phase Jitter Table

¹ Applies to all differential outputs, guaranteed by design and characterization.

² Calculated from Intel-supplied Clock Jitter Tool, with spread on and off.

³ Sample size of at least 100K cycles. This figure extrapolates to 108ps pk-pk at 1M cycles for a BER of 1^{-12} .

Electrical Characteristics–REF

TA = T_{COM} or T_{IND}; Supply Voltage per VDD of normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | Notes |
|------------------------|----------------------|---|-----|------|------|-------------|-------|
| Long Accuracy | ppm | see T _{period} min-max values | 0 | | | ppm | 1,2 |
| Clock period | T _{period} | 25 MHz output nominal | | 40 | | ns | 1,2 |
| Rise/Fall Slew Rate | t _{rf1} | Byte 3 = 1F, V _{OH} = VDD-0.45V, V _{OL} = 0.45V | 0.6 | 1 | 1.8 | V/ns | 1,3 |
| Rise/Fall Slew Rate | t _{rf1} | Byte 3 = 5F, V _{OH} = VDD-0.45V, V _{OL} = 0.45V | 1.0 | 1.6 | 2.5 | V/ns | 1,3 |
| Rise/Fall Slew Rate | t _{rf1} | Byte 3 = 9F, V _{OH} = VDD-0.45V, V _{OL} = 0.45V | 1.3 | 2 | 3.0 | V/ns | 1,3 |
| Rise/Fall Slew Rate | t _{rf1} | Byte 3 = DF, V _{OH} = VDD-0.45V, V _{OL} = 0.45V | 1.4 | 2.1 | 3.1 | V/ns | 1,3 |
| Duty Cycle | d _{t1} | V _T = VDD/2 V | 45 | 53.2 | 55 | % | 1,4 |
| Duty Cycle Distortion | d _{tcd} | V _T = VDD/2 V | 0 | 2 | 4 | % | 1,5 |
| Jitter, cycle to cycle | t _{jcc-cyc} | V _T = VDD/2 V | | 0 | 75 | ps | 1,4 |
| Noise floor | t _{dBc1k} | 1kHz offset | | -130 | -105 | dBc | 1,4 |
| Noise floor | t _{dBc10k} | 10kHz offset to Nyquist | | -140 | -120 | dBc | 1,4 |
| Jitter, phase | t _{phREF} | 12kHz to 5MHz | | 0.68 | 1.5 | ps (rms) | 1,4 |

¹Guaranteed by design and characterization, not 100% tested in production.

²All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF is trimmed to 25.00 MHz

³Typical value occurs when REF slew rate is set to default value

⁴When driven by a crystal.

⁵When driven by an external oscillator via the X1 pin. X2 should be floating in this case.

Clock Periods–Differential Outputs with Spread Spectrum Disabled

| SSC OFF | Center Freq. MHz | Measurement Window | | | | | | | Units | Notes |
|---------|------------------|------------------------------|--------------------------------------|--------------------------------------|----------------------------|--------------------------------------|--------------------------------------|------------------------------|-------|-------|
| | | 1 Clock | 1us | 0.1s | 0.1s | 0.1s | 1us | 1 Clock | | |
| | | -c2c jitter AbsPer Min | -SSC Short-Term Average Min | - ppm Long-Term Average Min | 0 ppm Period Nominal | + ppm Long-Term Average Max | +SSC Short-Term Average Max | +c2c jitter AbsPer Max | | |
| DIF | 100.00 | 9.94900 | | 9.99900 | 10.00000 | 10.00100 | | 10.05100 | ns | 1,2 |

Clock Periods–Differential Outputs with -0.5% Spread Spectrum Enabled

| SSC ON | Center Freq. MHz | Measurement Window | | | | | | | Units | Notes |
|--------|------------------|------------------------------|--------------------------------------|--------------------------------------|----------------------------|--------------------------------------|--------------------------------------|------------------------------|-------|-------|
| | | 1 Clock | 1us | 0.1s | 0.1s | 0.1s | 1us | 1 Clock | | |
| | | -c2c jitter AbsPer Min | -SSC Short-Term Average Min | - ppm Long-Term Average Min | 0 ppm Period Nominal | + ppm Long-Term Average Max | +SSC Short-Term Average Max | +c2c jitter AbsPer Max | | |
| DIF | 99.75 | 9.94906 | 9.99906 | 10.02406 | 10.02506 | 10.02607 | 10.05107 | 10.10107 | ns | 1,2 |

¹Guaranteed by design and characterization, not 100% tested in production.

²All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF is trimmed to 25.00 MHz

General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte N through Byte N+X-1
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

| Index Block Write Operation | | |
|-----------------------------|-----------|----------------------|
| Controller (Host) | | IDT (Slave/Receiver) |
| T | starT bit | |
| Slave Address | | |
| WR | WRite | |
| Beginning Byte = N | | ACK |
| Data Byte Count = X | | ACK |
| Beginning Byte N | | ACK |
| O | X Byte | O |
| O | | O |
| O | | O |
| Byte N + X - 1 | | ACK |
| P | stoP bit | |

Note: Read/Write address is latched on SADR pin.

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte N+X-1
- IDT clock sends **Byte 0 through Byte X (if X_(H) was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation | | |
|----------------------------|-----------------|----------------------|
| Controller (Host) | | IDT (Slave/Receiver) |
| T | starT bit | |
| Slave Address | | |
| WR | WRite | |
| Beginning Byte = N | | ACK |
| Repeat starT | | ACK |
| Slave Address | | |
| RD | ReaD | |
| Data Byte Count=X | | ACK |
| Beginning Byte N | | ACK |
| O | X Byte | O |
| O | | O |
| O | | O |
| O | | O |
| Byte N + X - 1 | | ACK |
| N | Not acknowledge | |
| P | stoP bit | |

SMBus Table: Output Enable Register

| Byte 0 | Name | Control Function | Type | 0 | 1 | Default |
|--------|---------|------------------|------|---------|---------|---------|
| Bit 7 | | Reserved | | | | 1 |
| Bit 6 | | Reserved | | | | 1 |
| Bit 5 | | Reserved | | | | 1 |
| Bit 4 | | Reserved | | | | 1 |
| Bit 3 | DIF OE3 | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 2 | DIF OE3 | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 1 | DIF OE2 | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 0 | DIF OE1 | Output Enable | RW | Low/Low | Enabled | 1 |

SMBus Table: SS Readback and Vhigh Control Register

| Byte 1 | Name | Control Function | Type | 0 | 1 | Default |
|--------|--------------|-----------------------------|-----------------|--|--------------------------------------|---------|
| Bit 7 | SSENRB1 | SS Enable Readback Bit1 | R | 00' for SS_EN_tri = 0, '01' for SS_EN_tri = 'M', '11 for SS_EN_tri = '1' | | Latch |
| Bit 6 | SSENRB1 | SS Enable Readback Bit0 | R | | | Latch |
| Bit 5 | SSEN_SWCNTRL | Enable SW control of SS | RW | SS control locked | Values in B1[4:3] control SS amount. | 0 |
| Bit 4 | SSENSW1 | SS Enable Software Ctl Bit1 | RW ¹ | 00' = SS Off, '01' = -0.25% SS, | | 0 |
| Bit 3 | SSENSW0 | SS Enable Software Ctl Bit0 | RW ¹ | '10' = Reserved, '11' = -0.5% SS | | 0 |
| Bit 2 | | Reserved | | | | 1 |
| Bit 1 | AMPLITUDE 1 | Controls Output Amplitude | RW | 00 = 0.6V | 01 = 0.7V | 1 |
| Bit 0 | AMPLITUDE 0 | | RW | 10 = 0.8V | 11 = 0.9V | 0 |

1. B1[5] must be set to a 1 for these bits to have any effect on the part.

SMBus Table: DIF Slew Rate Control Register

| Byte 2 | Name | Control Function | Type | 0 | 1 | Default |
|--------|------------------|--------------------------|------|---------|---------|---------|
| Bit 7 | | Reserved | | | | 1 |
| Bit 6 | | Reserved | | | | 1 |
| Bit 5 | | Reserved | | | | 1 |
| Bit 4 | | Reserved | | | | 1 |
| Bit 3 | SLEWRATESEL DIF3 | Adjust Slew Rate of DIF3 | RW | 2.0V/ns | 3.0V/ns | 1 |
| Bit 2 | SLEWRATESEL DIF2 | Adjust Slew Rate of DIF2 | RW | 2.0V/ns | 3.0V/ns | 1 |
| Bit 1 | SLEWRATESEL DIF1 | Adjust Slew Rate of DIF3 | RW | 2.0V/ns | 3.0V/ns | 1 |
| Bit 0 | SLEWRATESEL DIF0 | Adjust Slew Rate of DIF1 | RW | 2.0V/ns | 3.0V/ns | 1 |

SMBus Table: REF Control Register

| Byte 3 | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------------------------|----------------------------|------|--------------------------------|------------------------|---------|
| Bit 7 | REF | Slew Rate Control | RW | 00 = Slowest | 01 = Slow | 0 |
| Bit 6 | | | RW | 10 = Fast | 11 = Faster | 1 |
| Bit 5 | REF Power Down Function | Wake-on-Lan Enable for REF | RW | REF does not run in Power Down | REF runs in Power Down | 0 |
| Bit 4 | REF OE | REF Output Enable | RW | Low | Enabled | 1 |
| Bit 3 | | Reserved | | | | 1 |
| Bit 2 | | Reserved | | | | 1 |
| Bit 1 | | Reserved | | | | 1 |
| Bit 0 | | Reserved | | | | 1 |

Byte 4 is reserved and reads back 'hFF'.

SMBus Table: Revision and Vendor ID Register

| Byte 5 | Name | Control Function | Type | 0 | 1 | Default |
|--------|------|------------------|------|--------------|---|---------|
| Bit 7 | RID3 | Revision ID | R | A rev = 0000 | | 0 |
| Bit 6 | RID2 | | R | | | 0 |
| Bit 5 | RID1 | | R | | | 0 |
| Bit 4 | RID0 | | R | | | 0 |
| Bit 3 | VID3 | VENDOR ID | R | 0001 = IDT | | 0 |
| Bit 2 | VID2 | | R | | | 0 |
| Bit 1 | VID1 | | R | | | 0 |
| Bit 0 | VID0 | | R | | | 1 |

SMBus Table: Device Type/Device ID

| Byte 6 | Name | Control Function | Type | 0 | 1 | Default |
|--------|--------------|------------------|------|--|---|---------|
| Bit 7 | Device Type1 | Device Type | R | 00 = FGV, 01 = DBV, 10 = DMV, 11 = Reserved | | 0 |
| Bit 6 | Device Type0 | | R | | | 0 |
| Bit 5 | Device ID5 | Device ID | R | 000100 binary or 04 hex | | 0 |
| Bit 4 | Device ID4 | | R | | | 0 |
| Bit 3 | Device ID3 | | R | | | 0 |
| Bit 2 | Device ID2 | | R | | | 1 |
| Bit 1 | Device ID1 | | R | | | 0 |
| Bit 0 | Device ID0 | | R | | | 0 |

SMBus Table: Byte Count Register

| Byte 7 | Name | Control Function | Type | 0 | 1 | Default |
|--------|------|------------------------|------|---|---|---------|
| Bit 7 | | Reserved | | | | 0 |
| Bit 6 | | Reserved | | | | 0 |
| Bit 5 | | Reserved | | | | 0 |
| Bit 4 | BC4 | Byte Count Programming | RW | Writing to this register will configure how many bytes will be read back, default is = 8 bytes. | | 0 |
| Bit 3 | BC3 | | RW | | | 1 |
| Bit 2 | BC2 | | RW | | | 0 |
| Bit 1 | BC1 | | RW | | | 0 |
| Bit 0 | BC0 | | RW | | | 0 |

Recommended Crystal Characteristics (3225 package)

| PARAMETER | VALUE | UNITS | NOTES |
|--|-------------|---------|-------|
| Frequency | 25 | MHz | 1 |
| Resonance Mode | Fundamental | - | 1 |
| Frequency Tolerance @ 25°C | ±20 | PPM Max | 1 |
| Frequency Stability, ref @ 25°C Over Operating Temperature Range | ±20 | PPM Max | 1 |
| Temperature Range (commercial) | 0~70 | °C | 1 |
| Temperature Range (industrial) | -40~85 | °C | 2 |
| Equivalent Series Resistance (ESR) | 50 | Ω Max | 1 |
| Shunt Capacitance (C _O) | 7 | pF Max | 1 |
| Load Capacitance (C _L) | 8 | pF Max | 1 |
| Drive Level | 0.3 | mW Max | 1 |
| Aging per year | ±5 | PPM Max | 1 |

Notes:

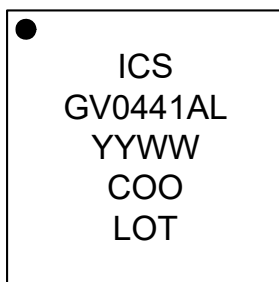
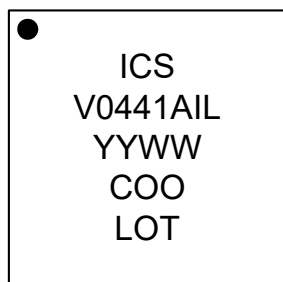
1. FOX 603-25-150.
2. For I-temp, FOX 603-25-261.

Thermal Characteristics

| PARAMETER | SYMBOL | CONDITIONS | PKG | TYP. | UNITS | NOTES |
|--------------------|----------------|---------------------------------|-------|------|-------|-------|
| Thermal Resistance | θ_{JC} | Junction to Case | NLG32 | 42 | °C/W | 1 |
| | θ_{Jb} | Junction to Base | | 2.4 | °C/W | 1 |
| | θ_{JA0} | Junction to Air, still air | | 39 | °C/W | 1 |
| | θ_{JA1} | Junction to Air, 1 m/s air flow | | 33 | °C/W | 1 |
| | θ_{JA3} | Junction to Air, 3 m/s air flow | | 28 | °C/W | 1 |
| | θ_{JA5} | Junction to Air, 5 m/s air flow | | 27 | °C/W | 1 |

¹ePad soldered to board

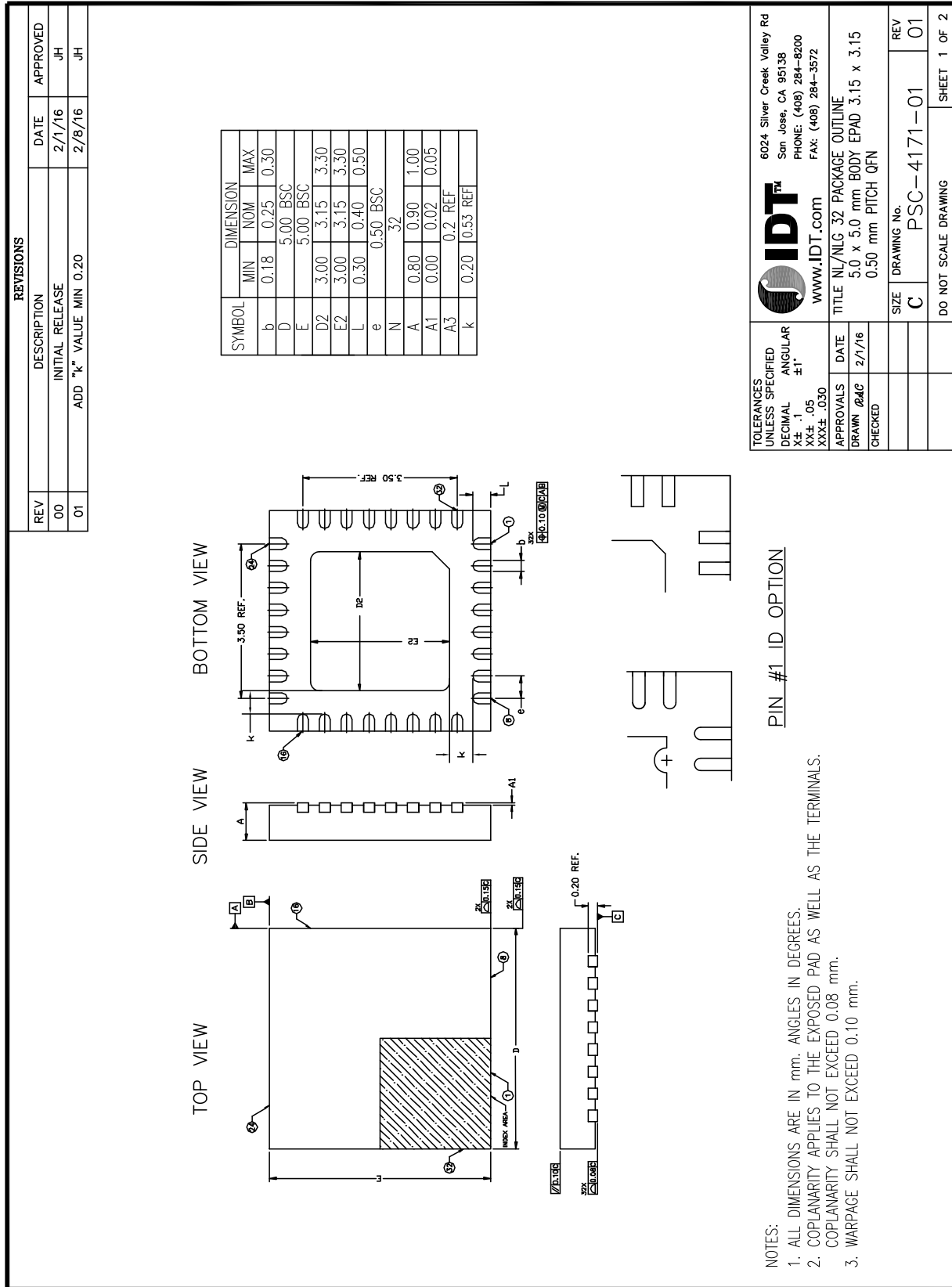
Marking Diagrams



Notes:

1. Line 2 is the truncated part number.
2. 'L' denotes RoHS compliant package.
3. 'I' denotes industrial temperature grade.
4. 'YYWW' is the last two digits of the year and week that the part was assembled.
5. 'COO' denotes country of origin.
6. 'LOT' is the lot number.

Package Outline and Dimensions (NLG32P1)

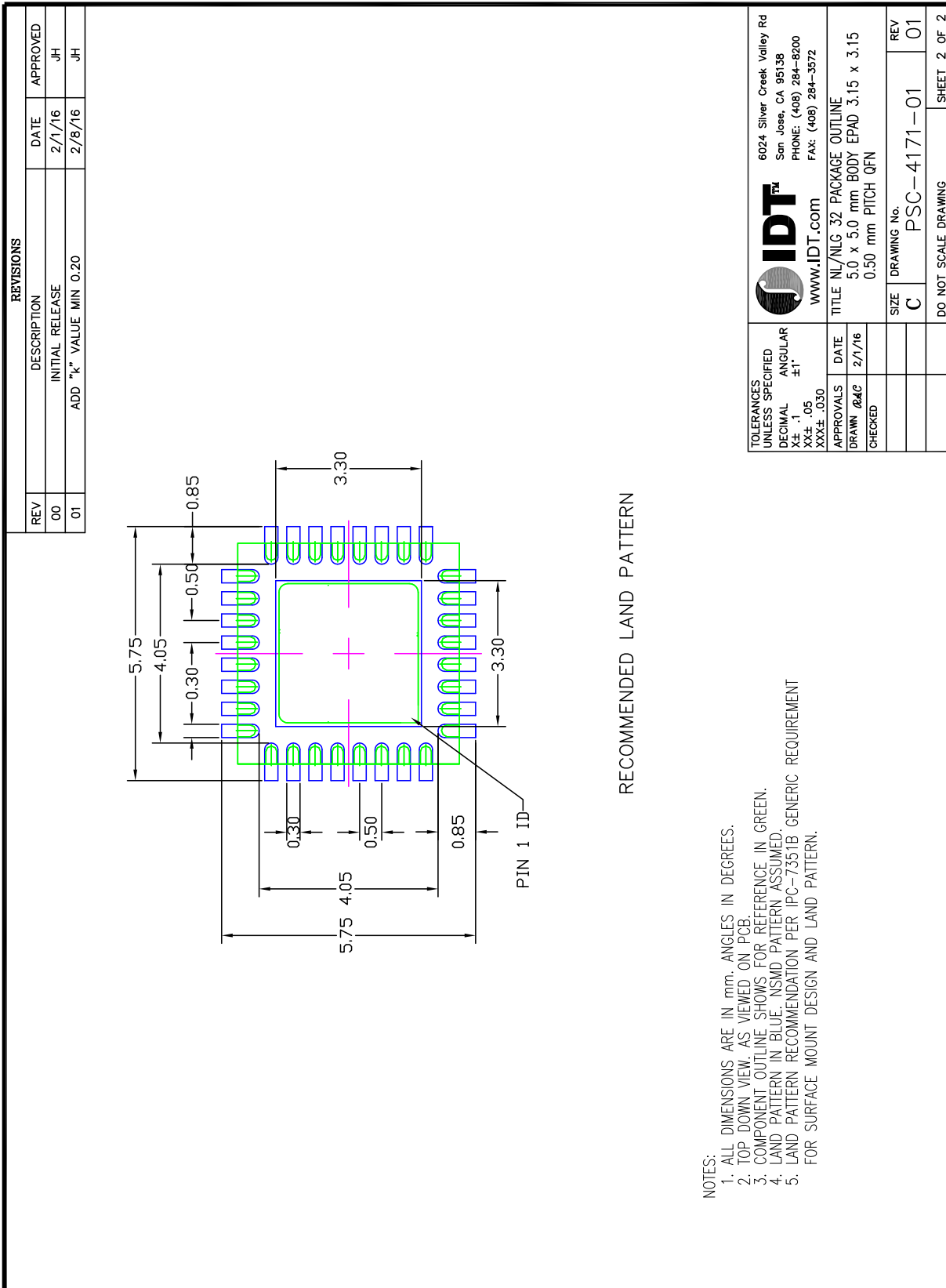


| | | |
|------------------------------------|-------------|--------------|
| TOLERANCES UNLESS SPECIFIED | DECIMAL | ANGULAR |
| | XX± .05 | ±1° |
| DRAWN | DATE | APPROVALS |
| CHECKED | 2/1/16 | |
| TITLE NL/NLG 32 PACKAGE OUTLINE | | |
| 5.0 x 5.0 mm BODY EPAD 3.15 x 3.15 | | |
| 0.50 mm PITCH QFN | | |
| SIZE | DRAWING No. | REV |
| C | PSC-4171-01 | 01 |
| DO NOT SCALE DRAWING | | SHEET 1 OF 2 |

PIN #1 ID OPTION

NOTES:
 1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
 2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
 COPLANARITY SHALL NOT EXCEED 0.08 mm.
 3. WARPAGE SHALL NOT EXCEED 0.10 mm.

Package Outline and Dimensions (NLG32P1), cont.



Ordering Information

| Part / Order Number | Shipping Packaging | Package | Temperature |
|---------------------|--------------------|---------------------------------|---------------|
| 9FGV0441AKLF | Trays | 5 x 5 mm, 0.5mm pitch 32-VFQFPN | 0 to +70° C |
| 9FGV0441AKLFT | Tape and Reel | 5 x 5 mm, 0.5mm pitch 32-VFQFPN | 0 to +70° C |
| 9FGV0441AKILF | Trays | 5 x 5 mm, 0.5mm pitch 32-VFQFPN | -40 to +85° C |
| 9FGV0441AKILFT | Tape and Reel | 5 x 5 mm, 0.5mm pitch 32-VFQFPN | -40 to +85° C |

“LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

“A” is the device revision designator (will not correlate with the datasheet revision).

Revision History

| Issue Date | Description |
|------------------|--|
| October 18, 2016 | Removed IDT crystal part number. |
| June 22, 2017 | Updated front page general description to reflect the PCIe Gen4 updates. Updated Electrical Characteristics - Filtered Phase Jitter Parameters - PCIe Common Clocked (CC) Architectures and added PCIe Gen4 data. |
| October 11, 2017 | Corrected typographical error in slew rate specifications of differential outputs. |
| June 6, 2019 | Changed Input Current minimum and maximum values from -200/200uA to -20/20uA. |

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