## Description

The 9FGV0841 is a member of IDT's SOC-friendly 1.8V very low-power PCIe clock family. It has integrated output terminations providing Zo = 100Ω for direction connection to 100Ω transmission lines. The device has 8 output enables for clock management, 2 different spread spectrum levels in addition to spread off, and 2 selectable SMBus addresses.

## Typical Applications

- PCIe Gen1–4 clock generation for Riser Cards
- Storage
- Networking
- JBOD
- Communications
- Access Points

## Output Features

- Eight 100MHz Low-Power HCSL (LP-HCSL) DIF pairs with Zo = 100Ω
- One 1.8V LVCMOS REF output with Wake-On-LAN (WOL) support

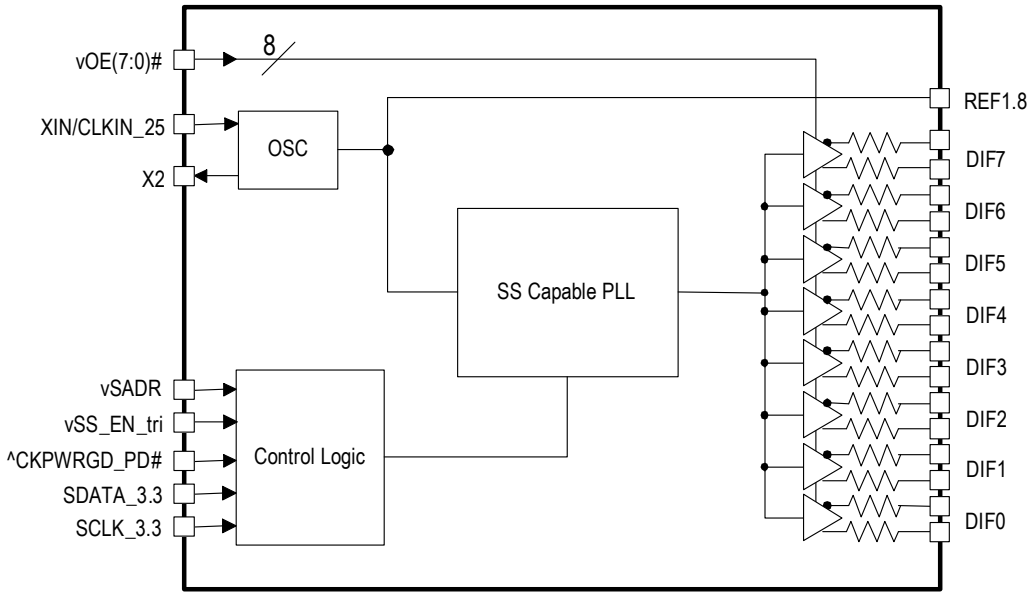
## Key Specifications

- DIF cycle-to-cycle jitter < 50ps
- DIF output-to-output skew < 50ps
- DIF phase jitter is PCIe Gen1–4 compliant
- REF phase jitter is < 1.5ps RMS

## Features

- Direct connection to 100Ω transmission lines; saves 32 resistors compared to standard PCIe devices
- 62mW typical power consumption; reduced thermal concerns
- Outputs can optionally be supplied from any voltage between 1.05V and 1.8V; maximum power savings
- OE# pins; support DIF power management
- LP-HCSL differential clock outputs; reduced power and board space
- Programmable slew rate for each output; allows tuning for various line lengths
- Programmable output amplitude; allows tuning for various application environments
- DIF outputs blocked until PLL is locked; clean system start-up
- Selectable 0%, -0.25% or -0.5% spread on DIF outputs; reduces EMI
- External 25MHz crystal; supports tight ppm with 0 ppm synthesis error
- Configuration can be accomplished with strapping pins; SMBus interface not required for device control
- 3.3V tolerant SMBus interface works with legacy controllers
- Selectable SMBus addresses; multiple devices can easily share an SMBus segment
- Space saving 6 x 6 mm 48-VFQFPN; minimal board space
- Available in Commercial (0° to +70°C), Industrial (-40°C to +85°C) and Automotive Grade 2 (-40°C to +105°C) temperature ranges

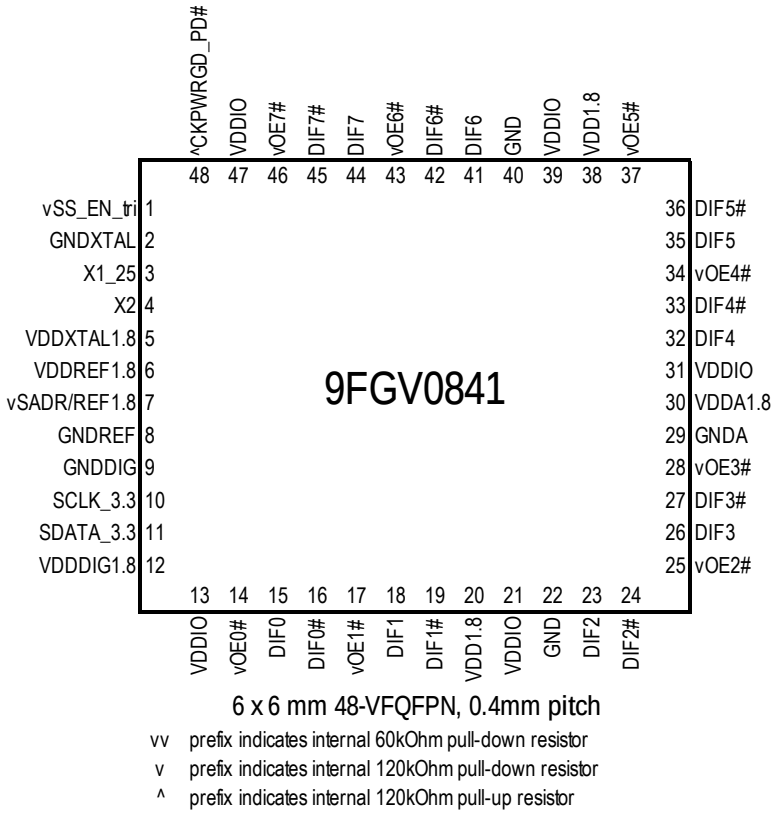
## Block Diagram



# Contents

# Pin Assignments

Figure 1. Pin Assignments for 6 x 6 mm 48-VFQFPN Package – Top View




6 x 6 mm 48-VFQFPN, 0.4mm pitch

vv prefix indicates internal 60kOhm pull-down resistor

v prefix indicates internal 120kOhm pull-down resistor

^ prefix indicates internal 120kOhm pull-up resistor

# Pin Descriptions

Table 1. Pin Descriptions

| Number | Name | Type | Description |
|---|---|---|---|
| 1 | vSS_EN_tri | Latched In | Latched select input to select spread spectrum amount at initial power-up:<br>1 = -0.5% spread, M = -0.25%, 0 = spread off |
| 2 | GNDXTAL | GND | Ground for XTAL. |
| 3 | X1_25 | Input | Crystal input, nominally 25.00MHz. |
| 4 | X2 | Output | Crystal output. |
| 5 | VDDXTAL1.8 | Power | Power supply for XTAL, nominal 1.8V. |
| 6 | VDDREF1.8 | Power | VDD for REF output, nominal 1.8V. |
| 7 | vSADR/REF1.8 | Latched I/O | Latch to select SMBus address/1.8V LVCMOS copy of X1/REFIN pin. |
| 8 | GNDREF | GND | Ground pin for the REF outputs. |
| 9 | GNDDIG | GND | Ground pin for digital circuitry. |
| 10 | SCLK_3.3 | Input | Clock pin of SMBus circuitry, 3.3V tolerant. |
| 11 | SDATA_3.3 | I/O | Data pin for SMBus circuitry, 3.3V tolerant. |
| 12 | VDDDIG1.8 | Power | 1.8V digital power (dirty power). |
| 13 | VDDIO | Power | Power supply for differential outputs. |

Table 1. Pin Descriptions (Cont.)

| Number | Name | Type | Description |
|---|---|---|---|
| 14 | vOE0# | Input | Active low input for enabling DIF pair 0. This pin has an internal pull-down.<br>1 =disable outputs, 0 = enable outputs |
| 15 | DIF0 | Output | Differential true clock output. |
| 16 | DIF0# | Output | Differential complementary clock output. |
| 17 | vOE1# | Input | Active low input for enabling DIF pair 1. This pin has an internal pull-down.<br>1 =disable outputs, 0 = enable outputs |
| 18 | DIF1 | Output | Differential true clock output. |
| 19 | DIF1# | Output | Differential complementary clock output. |
| 20 | VDD1.8 | Power | Power supply, nominal 1.8V. |
| 21 | VDDIO | Power | Power supply for differential outputs. |
| 22 | GND | GND | Ground pin. |
| 23 | DIF2 | Output | Differential true clock output. |
| 24 | DIF2# | Output | Differential complementary clock output. |
| 25 | vOE2# | Input | Active low input for enabling DIF pair 2. This pin has an internal pull-down.<br>1 =disable outputs, 0 = enable outputs |
| 26 | DIF3 | OUT | Differential true clock output. |
| 27 | DIF3# | OUT | Differential complementary clock output. |
| 28 | vOE3# | Input | Active low input for enabling DIF pair 3. This pin has an internal pull-down.<br>1 =disable outputs, 0 = enable outputs |
| 29 | GNDA | GND | Ground pin for the PLL core. |
| 30 | VDDA1.8 | Power | 1.8V power for the PLL core. |
| 31 | VDDIO | Power | Power supply for differential outputs. |
| 32 | DIF4 | Output | Differential true clock output. |
| 33 | DIF4# | Output | Differential complementary clock output. |
| 34 | vOE4# | Input | Active low input for enabling DIF pair 4. This pin has an internal pull-down.<br>1 =disable outputs, 0 = enable outputs |
| 35 | DIF5 | Output | Differential true clock output. |
| 36 | DIF5# | Output | Differential complementary clock output. |
| 37 | vOE5# | Input | Active low input for enabling DIF pair 5. This pin has an internal pull-down.<br>1 =disable outputs, 0 = enable outputs |
| 38 | VDD1.8 | Power | Power supply, nominal 1.8V. |
| 39 | VDDIO | Power | Power supply for differential outputs. |
| 40 | GND | GND | Ground pin. |
| 41 | DIF6 | Output | Differential true clock output. |
| 42 | DIF6# | Output | Differential complementary clock output. |
| 43 | vOE6# | Input | Active low input for enabling DIF pair 6. This pin has an internal pull-down.<br>1 =disable outputs, 0 = enable outputs |
| 44 | DIF7 | Output | Differential true clock output. |

Table 1. Pin Descriptions (Cont.)

| Number | Name | Type | Description |
|---|---|---|---|
| 45 | DIF7# | Output | Differential complementary clock output. |
| 46 | vOE7# | Input | Active low input for enabling DIF pair 7. This pin has an internal pull-down.<br>1 =disable outputs, 0 = enable outputs |
| 47 | VDDIO | Power | Power supply for differential outputs. |
| 48 | ^CKPWRGD_PD# | Input | Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor. |

# Power Management

Table 2. Power Management

| CKPWRGD_PD# | SMBus OE bit | DIFx | | | REF |
|---|---|---|---|---|---|
| | | OEx# | True Output | Complementary Output | |
| 0 | X | X | Low | Low | Hi-Z[1] |
| 1 | 1 | 0 | Running | Running | Running |
| 1 | 0 | 1 | Low | Low | Low |

[1] REF is Hi-Z until the 1st assertion of CKPWRGD_PD# high. After this, when CKPWRG_PD# is low, REF is Low.

Table 3. SMBus Address Selection

| | SADR | Address | + Read/Write Bit |
|---|---|---|---|
| State of SADR on first application of CKPWRGD_PD# | 0 | 1101000 | X |
| | 1 | 1101010 | X |

Table 4. Power Connections

| Pin Number | | | Description |
|---|---|---|---|
| VDD | VDDIO | GND | |
| 5 | | 2 | XTAL OSC |
| 6 | | 8 | REF Power |
| 12 | | 9 | Digital (dirty) Power |
| 20, 38 | 13, 21, 31, 39, 47 | 22, 29, 40 | DIF Outputs |
| 30 | | 29 | PLL Analog |

# Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 9FGV0841 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 5. Absolute Maximum Ratings

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|---|---|
| Supply Voltage | VDDxx | Applies to all $V_{DD}$ pins. | -0.5 | | 2.5 | V | 1,2 |
| Input Voltage | $V_{IN}$ | | -0.5 | | $V_{DD}$ + 0.5V | V | 1,3 |
| Input High Voltage, SMBus | $V_{IHSMB}$ | SMBus clock and data pins. | | | 3.6V | V | 1 |
| Storage Temperature | Ts | | -65 | | 150 | °C | 1 |
| Junction Temperature | Tj | | | | 125 | °C | 1 |
| Input ESD protection | ESD prot | Human Body Model. | 2000 | | | V | 1 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

[3] Not to exceed 2.5V.

# Thermal Characteristics

Table 6. Thermal Characteristics

| Parameter | Symbol | Conditions | Package | Typical Values | Units | Notes |
|---|---|---|---|---|---|---|
| Thermal Resistance | $\theta_{JC}$ | Junction to case. | NDG48 | 33 | °C/W | 1 |
| | $\theta_{Jb}$ | Junction to base. | | 2.1 | °C/W | 1 |
| | $\theta_{JA0}$ | Junction to air, still air. | | 37 | °C/W | 1 |
| | $\theta_{JA1}$ | Junction to air, 1 m/s air flow. | | 30 | °C/W | 1 |
| | $\theta_{JA3}$ | Junction to air, 3 m/s air flow. | | 27 | °C/W | 1 |
| | $\theta_{JA5}$ | Junction to air, 5 m/s air flow. | | 26 | °C/W | 1 |

[1] EPAD soldered to board.

# Electrical Characteristics

$T_A = T_{AMB}$; supply voltages per normal operation conditions. See ITest Loads for loading conditions

Table 7. Common Electrical Characteristics

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|---|---|
| Supply Voltage | VDDxx | Supply voltage for core, analog and single-ended LVCMOS outputs. | 1.7 | 1.8 | 1.9 | V | |
| Output Supply Voltage | VDDIO | Supply voltage for differential Low Power outputs. | 0.9975 | 1.05–1.8 | 1.9 | V | |
| Ambient Operating Temperature | $T_{AMB}$ | Commercial range. | 0 | 25 | 70 | °C | |
| | | Industrial range. | -40 | 25 | 85 | °C | |

Table 7. Common Electrical Characteristics (Cont.)

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|---|---|
| Input High Voltage | $V_{IH}$ | Single-ended inputs, except SMBus. | 0.75 $V_{DD}$ | | $V_{DD}$ + 0.3 | V | |
| Input Mid Voltage | $V_{IM}$ | Single-ended tri-level inputs ('_tri' suffix). | 0.4 $V_{DD}$ | 0.5 $V_{DD}$ | 0.6 $V_{DD}$ | V | |
| Input Low Voltage | $V_{IL}$ | Single-ended inputs, except SMBus. | -0.3 | | 0.25 $V_{DD}$ | V | |
| Output High Voltage | $V_{OH}$ | Single-ended outputs, except SMBus. $I_{OH}$ = -2mA | $V_{DD}$-0.45 | | | V | |
| Output Low Voltage | $V_{OL}$ | Single-ended outputs, except SMBus. $I_{OL}$ = -2mA | | | 0.45 | V | |
| Input Current | $I_{IN}$ | Single-ended inputs, $V_{IN}$ = GND, $V_{IN}$ = VDD. | -5 | | 5 | µA | |
| | $I_{INP}$ | Single-ended inputs. $V_{IN}$ = 0 V; Inputs with internal pull-up resistors. $V_{IN}$ = VDD; Inputs with internal pull-down resistors. | -20 | | 20 | µA | |
| Input Frequency | $F_{in}$ | XTAL, or X1 input. | 23 | 25 | 27 | MHz | |
| Pin Inductance | $L_{pin}$ | | | | 7 | nH | 1 |
| Capacitance | $C_{IN}$ | Logic Inputs, except DIF_IN. | 1.5 | | 5 | pF | 1 |
| | $C_{OUT}$ | Output pin capacitance. | | | 6 | pF | 1 |
| Clk Stabilization | $T_{STAB}$ | From $V_{DD}$ Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock. | | 0.6 | 1.8 | ms | 1,2 |
| SS Modulation Frequency | $f_{MOD}$ | Allowable Frequency. (Triangular Modulation) | 30 | 31.6 | 33 | kHz | 1 |
| OE# Latency | $t_{LATOE\#}$ | DIF start after OE# assertion. DIF stop after OE# deassertion | 1 | 3 | 3 | clocks | 1,3 |
| Tdrive_PD# | $t_{DRVPD}$ | DIF output enable after PD# de-assertion. | | 20 | 300 | us | 1,3 |
| Tfall | $t_F$ | Fall time of single-ended control inputs. | | | 5 | ns | 2 |
| Trise | $t_R$ | Rise time of single-ended control inputs. | | | 5 | ns | 2 |
| SMBus Input Low Voltage | $V_{ILSMB}$ | $V_{DDSMB}$ = 3.3V, see note 4 for $V_{DDSMB}$ < 3.3V. | | | 0.6 | V | |
| SMBus Input High Voltage | $V_{IHSMB}$ | $V_{DDSMB}$ = 3.3V, see note 5 for $V_{DDSMB}$ < 3.3V. | 2.1 | | 3.6 | V | 4 |
| SMBus Output Low Voltage | $V_{OLSMB}$ | At $I_{PULLUP}$. | | | 0.4 | V | |
| SMBus Sink Current | $I_{PULLUP}$ | At $V_{OL}$. | 4 | | | mA | |
| Nominal Bus Voltage | $V_{DDSMB}$ | | 1.7 | | 3.6 | V | |
| SCLK/SDATA Rise Time | $t_{RSMB}$ | (Max $V_{IL}$ - 0.15V) to (Min $V_{IH}$ + 0.15V). | | | 1000 | ns | 1 |
| SCLK/SDATA Fall Time | $t_{FSMB}$ | (Min $V_{IH}$ + 0.15V) to (Max $V_{IL}$ - 0.15V). | | | 300 | ns | 1 |
| SMBus Operating Frequency | $f_{MAXSMB}$ | Maximum SMBus operating frequency. | | | 400 | kHz | 1 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are > 200mV.

[4] For $V_{DDSMB}$ < 3.3V, $V_{IHSMB}$ > = 0.65 x $V_{DDSMB}$.

Table 8. DIF Low-Power HCSL (LP-HCSL) Outputs

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|---|---|
| Slew Rate | Trf | Scope averaging on fast setting. | 1.6 | 2.3 | 3.5 | V/ns | 1,2,3 |
| | | Scope averaging on slow setting. | 1.3 | 1.9 | 2.9 | V/ns | 1,2,3 |
| Slew Rate Matching | ΔTrf | Slew rate matching, scope averaging on. | | 7 | 20 | % | 1,2,4 |
| Voltage High | $V_{HIGH}$ | Statistical measurement on single-ended signal using oscilloscope math function (scope averaging on). | 660 | 784 | 850 | mV | 7 |
| Voltage Low | $V_{LOW}$ | | -150 | -33 | 150 | | 7 |
| Max Voltage | Vmax | Measurement on single-ended signal using absolute value (scope averaging off). | | 816 | 1150 | mV | 7 |
| Min Voltage | Vmin | | -300 | -42 | | | 7 |
| Vswing | Vswing | Scope averaging off. | 300 | 1634 | | mV | 1,2,7 |
| Crossing Voltage (abs) | Vcross_abs | Scope averaging off. | 250 | 427 | 550 | mV | 1,5,7 |
| Crossing Voltage (var) | Δ-Vcross | Scope averaging off. | | 12 | 140 | mV | 1,6,7 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform.

[3] Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a ±150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a ±75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations

[5] $V_{CROSS}$ is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of $V_{CROSS}$_min/max ($V_{CROSS}$ absolute) allowed. The intent is to limit $V_{CROSS}$ induced modulation by setting Δ-$V_{CROSS}$ to be smaller than $V_{CROSS}$ absolute.

[7] At default SMBus amplitude settings.

Table 9. Current Consumption

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|---|---|
| Operating Supply Current | $I_{DDAOP}$ | VDDA, All outputs active at100MHz. | | 6 | 9 | mA | |
| | $I_{DDOP}$ | All VDD, except VDDA and VDDIO, All outputs active at100MHz. | | 12 | 16 | mA | |
| | $I_{DDIOOP}$ | VDDIO, All outputs active at100MHz. | | 28 | 35 | mA | |
| Wake-on-LAN Current (CKPWRGD_PD# = '0' Byte 3, bit 5 = '1') | $I_{DDAPD}$ | VDDA, DIF outputs off, REF output running. | | 0.4 | 1 | mA | 2 |
| | $I_{DDPD}$ | All VDD, except VDDA and VDDIO, DIF outputs off, REF output running. | | 5.3 | 8 | mA | 2 |
| | $I_{DDIOPD}$ | VDDIO, DIF outputs off, REF output running. | | 0.04 | 0.1 | mA | 2 |
| Powerdown Current (CKPWRGD_PD# = '0' Byte 3, bit 5 = '0') | $I_{DDAPD}$ | VDDA, all outputs off. | | 0.4 | 1 | mA | |
| | $I_{DDPD}$ | All VDD, except VDDA and VDDIO, all outputs off. | | 0.6 | 1 | mA | |
| | $I_{DDIOPD}$ | VDDIO, all outputs off. | | 0.0005 | 0.1 | mA | |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] This is the current required to have the REF output running in Wake-on-LAN mode (Byte 3, bit 5 = 1).

Table 10. DIF Output Duty Cycle, Jitter, and Skew Characteristics

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|---|---|
| Duty Cycle | $t_{DC}$ | Measured differentially, PLL Mode. | 45 | 50 | 55 | % | 1,2 |
| Skew, Output to Output | $t_{sk3}$ | Averaging on, $V_T$ = 50%. | | 43 | 50 | ps | 1,2 |
| Jitter, Cycle to Cycle | $t_{jcyc-cyc}$ | | | 14 | 50 | ps | 1,2 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform.

Table 11. Filtered Phase Jitter Parameters – PCIe Common Clocked (CC) Architectures

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Specification Limits | Units | Notes |
|---|---|---|---|---|---|---|---|---|
| Phase Jitter, PLL Mode | $t_{jphPCIeG1-CC}$ | PCIe Gen1. | 21 | 25 | 35 | 86 | ps (p-p) | 1,2,3 |
| | $t_{jphPCIeG2-CC}$ | PCIe Gen2 Low Band 10kHz < f < 1.5MHz (PLL BW of 5–16MHz, 8–16MHz, CDR = 5MHz). | 0.9 | 0.9 | 1.1 | 3 | ps (rms) | 1,2 |
| | | PCIe Gen2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5–16MHz, 8–16MHz, CDR = 5MHz). | 1.5 | 1.6 | 1.9 | 3.1 | ps (rms) | 1,2 |
| | $t_{jphPCIeG3-CC}$ | PCIe Gen3 (PLL BW of 2–4MHz, 2–5MHz, CDR = 10MHz). | 0.3 | 0.37 | 0.44 | 1 | ps (rms) | 1,2 |
| | $t_{jphPCIeG4-CC}$ | PCIe Gen4 (PLL BW of 2–4MHz, 2–5MHz, CDR = 10MHz). | 0.3 | 0.37 | 0.44 | 0.5 | ps (rms) | 1,2 |

Table 12. REF

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|---|---|
| Long Accuracy | ppm | See Tperiod min–max values. | 0 | | | ppm | 1,2 |
| Clock Period | $T_{period}$ | 25MHz output. | | 40 | | ns | 2 |
| Rise/Fall Slew Rate | $t_{rf1}$ | Byte 3 = 1F, 20% to 80% of $V_{DDREF}$. | 0.6 | 1 | 1.6 | V/ns | 1 |
| Rise/Fall Slew Rate | $t_{rf1}$ | Byte 3 = 5F, 20% to 80% of $V_{DDREF}$. | 0.9 | 1.4 | 2.2 | V/ns | 1,3 |
| Rise/Fall Slew Rate | $t_{rf1}$ | Byte 3 = 9F, 20% to 80% of $V_{DDREF}$. | 1.1 | 1.7 | 2.7 | V/ns | 1 |
| Rise/Fall Slew Rate | $t_{rf1}$ | Byte 3 = DF, 20% to 80% of $V_{DDREF}$. | 1.1 | 1.8 | 2.9 | V/ns | 1 |
| Duty Cycle | $d_{t1X}$ | $V_T = V_{DD}/2$ V. | 45 | 49.1 | 55 | % | 1,4 |
| Duty Cycle Distortion | $d_{tcd}$ | $V_T = V_{DD}/2$ V. | 0 | 2 | 4 | % | 1,5 |
| Jitter, Cycle to Cycle | $t_{jcyc-cyc}$ | $V_T = V_{DD}/2$ V. | | 19.1 | 250 | ps | 1,4 |

Table 12. REF (Cont.)

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|---|---|
| Noise Floor | $t_{jdBc1k}$ | 1kHz offset. | | -129.8 | -105 | dBc | 1,4 |
| Noise Floor | $t_{jdBc10k}$ | 10kHz offset to Nyquist. | | -143.6 | -115 | dBc | 1,4 |
| Jitter, Phase | $t_{jphREF}$ | 12kHz to 5MHz. | | 0.63 | 1.5 | ps (rms) | 1,4 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF is trimmed to 25.00MHz.

[3] Default SMBus value.

[4] When driven by a crystal.

[5] When driven by an external oscillator via the X1 pin, X2 should be floating.

## Clock Periods

Table 13. Clock Periods - Differential Outputs with Spread Spectrum Disabled

| SSC OFF | Center Frequency MHz | Measurement Window | | | | | | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | | 1 Clock | 1µs | 0.1s | 0.1s | 0.1s | 1µs | 1 Clock | | |
| | | -c2cjitter AbsPer Min | -SSC Short-Term Average Min | -ppm Long-Term Average Min | 0 ppm Period Nominal | +ppm Long-Term Average Max | +SSC Short-Term Average Max | +c2cjitter AbsPer Max | | |
| DIF | 100.00 | 9.94900 | — | 9.99900 | 10.00000 | 10.00100 | — | 10.05100 | ns | 1,2 |

Table 14. Clock Periods - Differential Outputs with Spread Spectrum Enabled

| SSC ON | Center Frequency MHz | Measurement Window | | | | | | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | | 1 Clock | 1µs | 0.1s | 0.1s | 0.1s | 1µs | 1 Clock | | |
| | | -c2cjitter AbsPer Min | -SSC Short-Term Average Min | -ppm Long-Term Average Min | 0 ppm Period Nominal | +ppm Long-Term Average Max | +SSC Short-Term Average Max | +c2cjitter AbsPer Max | | |
| DIF | 99.75 | 9.94906 | 9.99906 | 10.02406 | 10.02506 | 10.02607 | 10.05107 | 10.10107 | ns | 1,2 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF is trimmed to 0ppm.

## Crystal Characteristics

Table 15. Recommended Crystal Characteristics

| Parameter | Value | Units |
|---|---|---|
| Frequency | 25 | MHz |
| Resonance Mode | Fundamental | – |
| Frequency Tolerance at 25°C | ±20 | ppm maximum |
| Frequency Stability, REF at 25°C Over Operating Temperature Range | ±20 | ppm maximum |
| Temperature Range (commercial) | 0–70 | °C |
| Temperature Range (industrial) | -40–85 | °C |
| Equivalent Series Resistance (ESR) | 50 | Ω maximum |
| Shunt Capacitance ($C_O$) | 7 | pF maximum |
| Load Capacitance ($C_L$) | 8 | pF maximum |
| Drive Level | 0.1 | mW maximum |
| Aging Per Year | ±5 | ppm maximum |

## ITest Loads

Figure 2. Low-Power HCSL (LP-HCSL) Differential Output Test Load

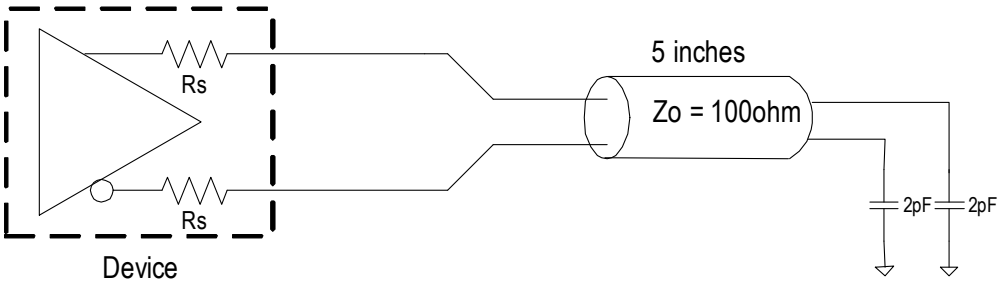
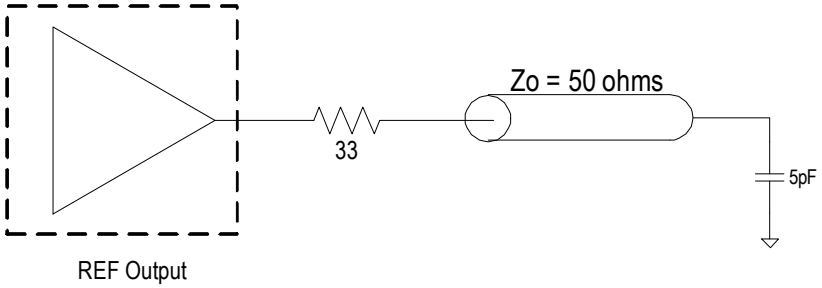



Figure 3. REF Output Test Load



# Alternate Terminations

Figure 4. Driving LVDS

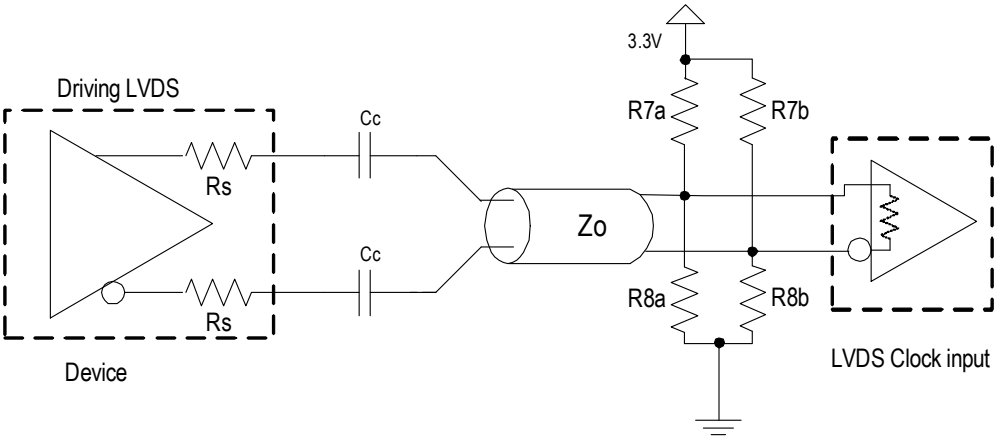



Table 16. Driving LVDS Inputs

| Component | Value | |
|---|---|---|
| | Receiver has termination | Receiver does not have termination |
| R7a, R7b | 10kΩ | 140Ω |
| R8a, R8b | 5.6kΩ | 75Ω |
| Cc | 0.1uF | 0.1uF |
| Vcm | 1.2 Volts | 1.2 Volts |

# General SMBus Serial Interface Information

## How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will acknowledge
- Controller (host) sends the beginning byte location = N
- IDT clock will acknowledge
- Controller (host) sends the byte count = X
- IDT clock will acknowledge
- Controller (host) starts sending Byte N through Byte N+X-1
- IDT clock will acknowledge each byte one at a time
- Controller (host) sends a stop bit

| Index Block Write Operation | | | |
|---|---|---|---|
| Controller (Host) | | | IDT (Slave/Receiver) |
| T | starT bit | | |
| Slave Address | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| Data Byte Count = X | | | |
| | | | ACK |
| Beginning Byte N | | X Byte | |
| | | | ACK |
| O | | | |
| O | | | O |
| O | | | O |
| | | | O |
| Byte N + X - 1 | | | |
| | | | ACK |
| P | stoP bit | | |

Note: SMBus address is latched on SADR pin.

## How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will acknowledge
- Controller (host) sends the beginning byte location = N
- IDT clock will acknowledge
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will acknowledge
- IDT clock will send the data byte count = X
- IDT clock sends Byte N+X-1
- IDT clock sends Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation | | | |
|---|---|---|---|
| Controller (Host) | | | IDT (Slave/Receiver) |
| T | starT bit | | |
| Slave Address | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| RT | Repeat starT | | |
| Slave Address | | | |
| RD | ReaD | | |
| | | | ACK |
| | | | |
| | | | Data Byte Count=X |
| ACK | | | |
| | | X Byte | Beginning Byte N |
| ACK | | | |
| | | | O |
| O | | | O |
| O | | | O |
| O | | | |
| | | | Byte N + X - 1 |
| N | Not acknowledge | | |
| P | stoP bit | | |

SMBus Table: Output Enable Register[1]

| Byte 0 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | DIF OE7 | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 6 | DIF OE6 | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 5 | DIF OE5 | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 4 | DIF OE4 | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 3 | DIF OE3 | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 2 | DIF OE2 | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 1 | DIF OE1 | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 0 | DIF OE0 | Output Enable | RW | Low/Low | Enabled | 1 |

[1] A low on these bits will override the OE# pin and force the differential output Low/Low.

SMBus Table: SS Readback and Control Register

| Byte 1 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | SSENRB1 | SS Enable Readback Bit1 | R | 00' for SS_EN_tri = 0, '01' for SS_EN_tri = 'M', '11 for SS_EN_tri = '1' | | Latch |
| Bit 6 | SSENRB1 | SS Enable Readback Bit0 | R | | | Latch |
| Bit 5 | SSEN_SWCNTRL | Enable SW control of SS | RW | Values in B1[7:6] control SS amount | Values in B1[4:3] control SS amount. | 0 |
| Bit 4 | SSENSW1 | SS Enable Software Ctl Bit1 | RW[1] | 00' = SS Off, '01' = -0.25% SS, '10' = Reserved, '11'= -0.5% SS | | 0 |
| Bit 3 | SSENSW0 | SS Enable Software Ctl Bit0 | RW[1] | | | 0 |
| Bit 2 | Reserved | | | | | 1 |
| Bit 1 | AMPLITUDE 1 | Controls Output Amplitude | RW | 00 = 0.6V | 01 = 0.7V | 1 |
| Bit 0 | AMPLITUDE 0 | | RW | 10= 0.8V | 11 = 0.9V | 0 |

[1] B1[5] must be set to a 1 for these bits to have any effect on the part.

SMBus Table: DIF Slew Rate Control Register

| Byte 2 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | SLEWRATESEL DIF7 | Adjust Slew Rate of DIF7 | RW | Slow Setting | Fast Setting | 1 |
| Bit 6 | SLEWRATESEL DIF6 | Adjust Slew Rate of DIF6 | RW | Slow Setting | Fast Setting | 1 |
| Bit 5 | SLEWRATESEL DIF5 | Adjust Slew Rate of DIF5 | RW | Slow Setting | Fast Setting | 1 |
| Bit 4 | SLEWRATESEL DIF4 | Adjust Slew Rate of DIF4 | RW | Slow Setting | Fast Setting | 1 |
| Bit 3 | SLEWRATESEL DIF3 | Adjust Slew Rate of DIF3 | RW | Slow Setting | Fast Setting | 1 |
| Bit 2 | SLEWRATESEL DIF2 | Adjust Slew Rate of DIF2 | RW | Slow Setting | Fast Setting | 1 |
| Bit 1 | SLEWRATESEL DIF1 | Adjust Slew Rate of DIF1 | RW | Slow Setting | Fast Setting | 1 |
| Bit 0 | SLEWRATESEL DIF0 | Adjust Slew Rate of DIF0 | RW | Slow Setting | Fast Setting | 1 |

SMBus Table: Nominal $V_{HIGH}$ Amplitude Control / REF Control Register

| Byte 3 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | REF | Slew Rate Control | RW | 00 = Slowest | 01 = Slow | 0 |
| Bit 6 | | | RW | 10 = Fast | 11 = Faster | 1 |
| Bit 5 | REF Power Down Function | Wake-on-Lan Enable for REF | RW | REF does not run in Power Down | REF runs in Power Down | 0 |
| Bit 4 | REF OE | REF Output Enable | RW | Low | Enabled | 1 |
| Bit 3 | Reserved | | | | | 1 |
| Bit 2 | Reserved | | | | | 1 |
| Bit 1 | Reserved | | | | | 1 |
| Bit 0 | Reserved | | | | | 1 |

Byte 4 is Reserved.

SMBus Table: Revision and Vendor ID Register

| Byte 5 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | RID3 | Revision ID | R | Industrial: 0001 (revision A)<br>Automotive; 1000 (revision A) | | 0 |
| Bit 6 | RID2 | | R | | | 0 |
| Bit 5 | RID1 | | R | | | 0 |
| Bit 4 | RID0 | | R | | | 1 |
| Bit 3 | VID3 | VENDOR ID | R | 0001 = IDT | | 0 |
| Bit 2 | VID2 | | R | | | 0 |
| Bit 1 | VID1 | | R | | | 0 |
| Bit 0 | VID0 | | R | | | 1 |

SMBus Table: Device Type/Device ID Register

| Byte 6 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Device Type1 | Device Type | R | 00 = FGx, 01 = DBx ZDB/FOB,<br>10 = DMx, 11= DBx FOB | | 0 |
| Bit 6 | Device Type0 | | R | | | 0 |
| Bit 5 | Device ID5 | Device ID | R | 001000 binary or 08 hex | | 0 |
| Bit 4 | Device ID4 | | R | | | 0 |
| Bit 3 | Device ID3 | | R | | | 1 |
| Bit 2 | Device ID2 | | R | | | 0 |
| Bit 1 | Device ID1 | | R | | | 0 |
| Bit 0 | Device ID0 | | R | | | 0 |

SMBus Table: Revision and Vendor ID Register

| Byte 7 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | | | | 0 |
| Bit 6 | Reserved | | | | | 0 |
| Bit 5 | Reserved | | | | | 0 |
| Bit 4 | BC4 | Byte Count Programming | RW | Writing to this register will configure how many bytes will be read back, default is = 8 bytes. | | 0 |
| Bit 3 | BC3 | | RW | | | 1 |
| Bit 2 | BC2 | | RW | | | 0 |
| Bit 1 | BC1 | | RW | | | 0 |
| Bit 0 | BC0 | | RW | | | 0 |

## Package Outline Drawings

The package outline drawings are appended at the end of this document and are also accessible from the link below. The package information is the most current data available and is subject to change without notice or revision of this document.

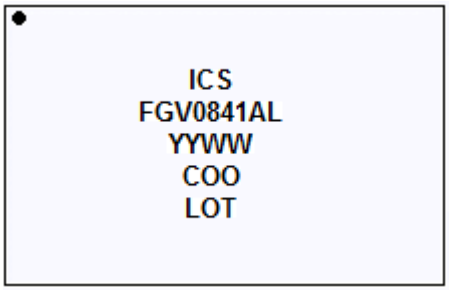
### Commercial and Industrial Devices

www.idt.com/document/psc/48-vfqfpn-package-outline-drawing-60-x-60-x-090-mm-body-epad-42-x-42-mm-040mm-pitch-ndg48p2

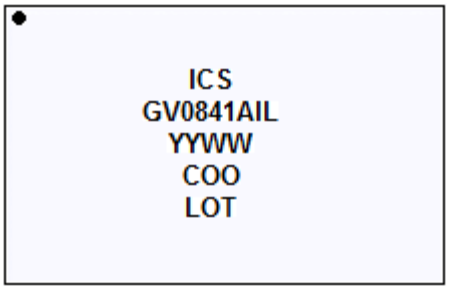
### Automotive Devices

www.idt.com/document/psc/48-vfqfpn-package-outline-drawing-48-vfqfpn-package-outline-drawing-ndg48s1-wettable-flank

## Marking Diagrams




Commercial




Industrial


Automotive

- Lines 1 and 2: truncated part number
- “YYWW” denotes the last digits of the year and work week the part was assembled.
- “#” denotes the stepping sequence.
- “$” denotes mark code.
- “COO” denotes country of origin/
- “LOT” denotes the lot number.

# Ordering Information

| Orderable Part Number | Package | Carrier Type | Temperature |
|---|---|---|---|
| 9FGV0841AKLF | 6 × 6 mm, 0.4mm pitch 48-VFQFPN | Tray | 0 to +70°C |
| 9FGV0841AKLFT | 6 × 6 mm, 0.4mm pitch 48-VFQFPN | Reel | 0 to +70°C |
| 9FGV0841AKILF | 6 × 6 mm, 0.4mm pitch 48-VFQFPN | Tray | -40 to +85°C |
| 9FGV0841AKILFT | 6 × 6 mm, 0.4mm pitch 48-VFQFPN | Reel | -40 to +85°C |
| 9FGV0841ANDG2 | 6 × 6 mm, 0.4mm pitch 48-VFQFPN (wettable flank) | Tray | -40 to +105°C |
| 9FGV0841ANDG28 | 6 × 6 mm, 0.4mm pitch 48-VFQFPN (wettable flank) | Reel | -40 to +105°C |

"LF" indicates Pb-free, RoHS compliant.

"A" is the device revision designator (will not correlate to with the datasheet revision).

# Revision History

| Revision Date | Description of Change |
|---|---|
| June 6, 2019 | Changed Input Current minimum and maximum values from -200/200µA to -20/20µA. |
| May 16, 2019 | Added automotive information. |
| January 24, 2018 | Corrected Byte 5 bit 4 to be '1' instead of '0'. |
| June 26, 2017 | ▪ Updated front page general description to reflect the PCIe Gen4 updates.<br>▪ Updated *Electrical Characteristics - Filtered Phase Jitter Parameters - PCIe Common Clocked (CC) Architectures* table and added PCIe Gen4 Data. |
| October 18, 2016 | Removed IDT crystal part number. |
| November 12, 2015 | Updated Package outline drawings. |

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