

## Description

This document details the custom configuration that is programmed into the one-time-programmable (OTP) memory of the 9FGV1006Q505LTGI. Please refer to the device datasheet for further information about the device.

## General Configuration

Parameter	Value	Units
Device I <sup>2</sup> C Address	Primary 0xD0	—
Crystal Load Capacitance	9.29	pF

## Frequency Overview

Parameter	Configuration 0	Configuration 1	Configuration 2	Configuration 3	Units
Internal Crystal	50	50	50	50	MHz
REF 0	Off	Off	Off	Off	MHz
Output 0	100	100	100	100	MHz
Output 1	100	100	100	100	MHz

## Configuration 0 Parameters: SEL[1:0] = 00

Parameter	REF 0	Output 0	Output 1	Units
Crystal Frequency	50	50	50	MHz
Default Output Status	Off	On	On	
VDDO Voltage	3.3	3.3	3.3	V
Output Type	LVC MOS	LP-HCSL	LP-HCSL	
Frequency	—	100	100	MHz
Spread Spectrum	—	Off	Off	%
Spread Modulation Rate	—	—	—	kHz
LP-HCSL Impedance	—	100	100	Ω

Configuration 1 Parameters: SEL[1:0] = 01

Parameter	REF 0	Output 0	Output 1	Units
Crystal Frequency	50	50	50	MHz
Default Output Status	Off	On	On	
VDDO Voltage	3.3	3.3	3.3	V
Output Type	LVC MOS	LP-HCSL	LP-HCSL	
Frequency	—	100	100	MHz
Spread Spectrum	—	-0.10	-0.10	%
Spread Modulation Rate	—	31.5	31.5	kHz
LP-HCSL Impedance	—	100	100	Ω

Configuration 2 Parameters: SEL[1:0] = 10

Parameter	REF 0	Output 0	Output 1	Units
Crystal Frequency	50	50	50	MHz
Default Output Status	Off	On	On	
VDDO Voltage	3.3	3.3	3.3	V
Output Type	LVC MOS	LP-HCSL	LP-HCSL	
Frequency	—	100	100	MHz
Spread Spectrum	—	-0.30	-0.30	%
Spread Modulation Rate	—	31.5	31.5	kHz
LP-HCSL Impedance	—	100	100	Ω

Configuration 3 Parameters: SEL[1:0] = 11

Parameter	REF 0	Output 0	Output 1	Units
Crystal Frequency	50	50	50	MHz
Default Output Status	Off	On	On	
VDDO Voltage	3.3	3.3	3.3	V
Output Type	LVC MOS	LP-HCSL	LP-HCSL	
Frequency	—	100	100	MHz
Spread Spectrum	—	-0.50	-0.50	%
Spread Modulation Rate	—	31.5	31.5	kHz
LP-HCSL Impedance	—	100	100	Ω

Typical 12kHz–20MHz Phase Jitter with SSC Off

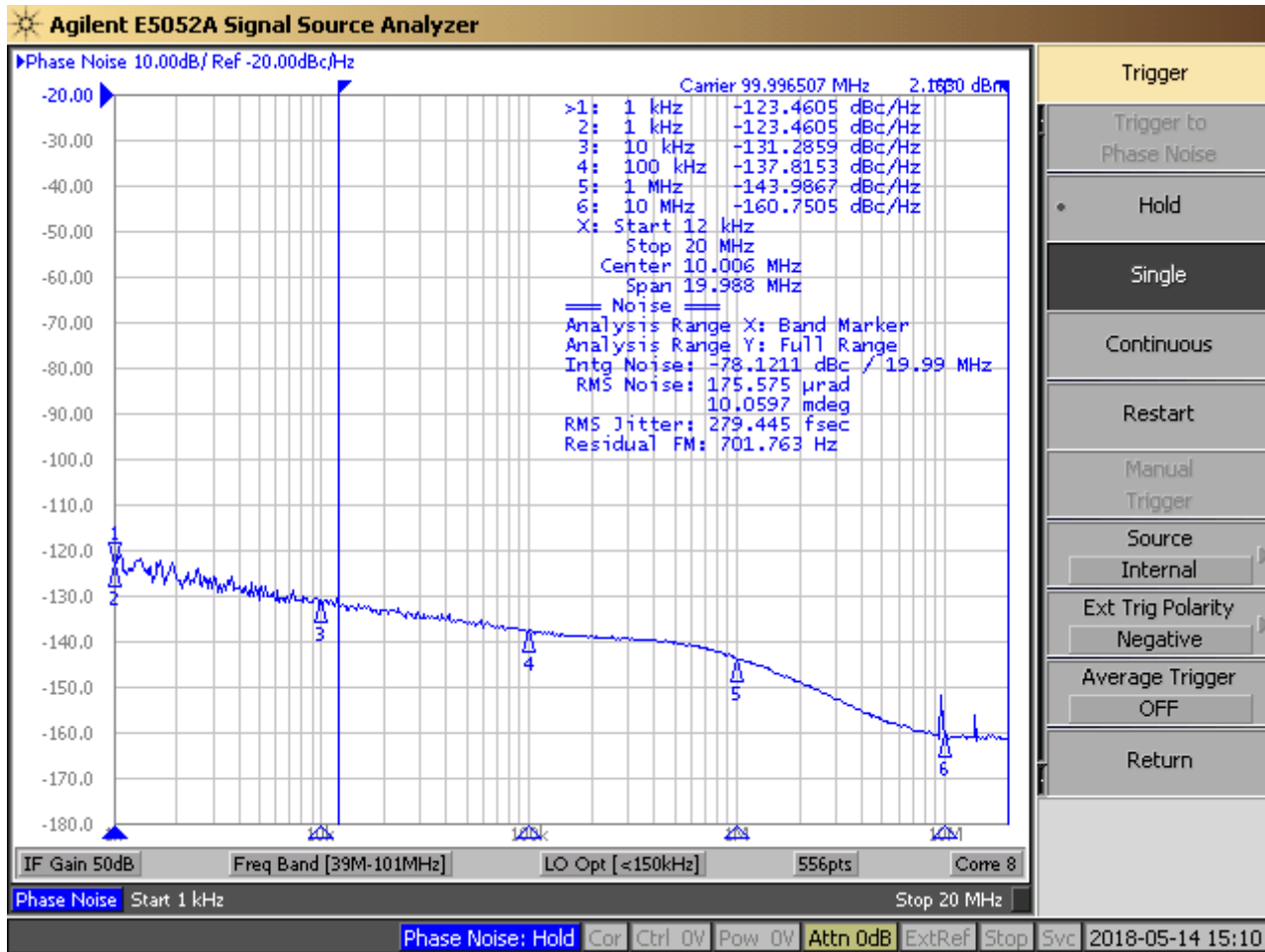


Table 1. Typical PCIe Phase Jitter at -0.5% Spread

PCIe Common Clock Generation	ps
Gen1: pk-pk (ps) Spec = 86 ps	20.71
PCIe Gen2 RMS Low Band (ps) Spec = 3 ps	0.462
PCIe Gen2 RMS High Band (ps) Spec = 3.1 ps	0.949
PCIe Gen3 RMS (ps) Spec = 1 ps	0.285
PCIe Gen4 RMS (ps) Spec = 0.5 ps	0.285

## 9FGV1006Q505LTGI Ordering Information

Orderable Part Number	Marking	Package	Carrier Type	Temperature
9FGV1006Q505LTGI	6505I YWW xxx	3 × 3 mm, 0.5mm pitch 16-LGA	Tray	-40° to +85°C
9FGV1006Q505LTGI8	6505I YWW xxx	3 × 3 mm, 0.5mm pitch 16-LGA	Reel	-40° to +85°C

### Marking notes:

<sup>1</sup> Line 1: truncated part number.

<sup>2</sup> “YWW” is the last digit of the year and work week that the part was assembled.

<sup>3</sup> “xxx” denotes the lot number.

## Revision History

Revision Date	Description of Change
May 21, 2018	Initial release.

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(Rev.4.0-1 November 2017)

## Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

## Contact Information

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