# Low Power Programmable Timing Control Hub™ for P4™ processor

**Recommended Application:**

Low Power CK505 Compliant Main Clock

**Output Features:**

- 2 - 0.8V push-pull differential CPU pairs
- 7 - 0.8V push-pull differential PCIEX pairs
- 1 - 0.8V push-pull differential SATA pair
- 1 - 0.8V push-pull differential CPU/PCIEX selectable pair
- 1 - 0.8V push-pull differential 27MHz/LCDCLK/PCIEX selectable pair
- 4 - PCI (33MHz)
- 2 - PCICLK_F, (33MHz) free-running
- 1 - USB, 48MHz
- 1 - DOT96/PCIEX selectable pair
- 2 - REF, 14.318MHz

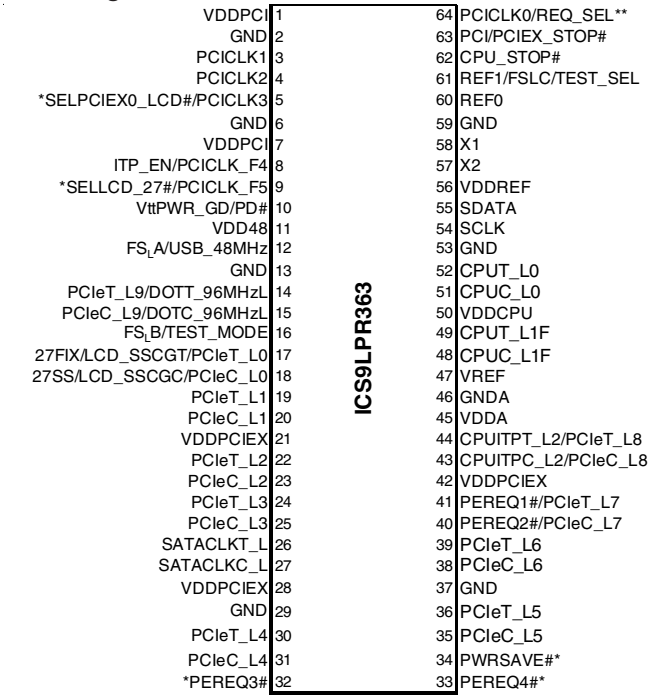
**Key Specifications:**

- CPU outputs cycle-cycle jitter < 85ps
- PCIEX outputs cycle-cycle jitter < 125ps
- SATA outputs cycle-cycle jitter < 125ps
- PCI outputs cycle-cycle jitter < 500ps
- +/- 100ppm frequency accuracy on CPU, PCIEX and SATA clocks
- +/- 100ppm frequency accuracy on USB clocks

**Features/Benefits:**

- Supports tight ppm accuracy clocks for Serial-ATA and PCIEX
- Supports programmable spread percentage and frequency
- Uses external 14.318MHz crystal, external crystal load caps are required for frequency tuning
- PEREQ# pins to support PCIEX power management.
- Low power differential clock outputs (No 50Ω resistor to GND needed)
- iAMT support

**Pin Configuration**




**64-TSSOP**

* Internal Pull-Up Resistor

** Internal Pull-Down Resistor

Note: Please add an external resistor for pull up or down, never rely on an internal resistor when the pin is connected to a device

**Latch Select Table**

| Pin5 | Pin9 | Pin14/15 | Pin17/18 |
|---|---|---|---|
| SELPCIEX0_LCD#/ PCI3 = 0 (low) | SELLCD_27#=0 | PCIEX9 | 27FIX/SS |
| | SELLCD_27#=1 | DOT96 | LCD |
| SELPCIEX0_LCD#/ PCI3 = 1 (high) | SELLCD_27#=0 | PCIEX9 | PCIEX0 |
| | SELLCD_27#=1 | DOT96 | PCIEX0 |

**Functionality Table**

| $FS_LC$ | $FS_LB$ | $FS_LA$ | CPU MHz | PCI MHz | PCIEX MHz | Spread % |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 266.66 | 33.33 | 100.00 | 0.5% Down |
| 0 | 0 | 1 | 133.33 | 33.33 | 100.00 | 0.5% Down |
| 0 | 1 | 0 | 200.00 | 33.33 | 100.00 | 0.5% Down |
| 0 | 1 | 1 | 166.66 | 33.33 | 100.00 | 0.5% Down |
| 1 | 0 | 0 | 333.33 | 33.33 | 100.00 | 0.5% Down |
| 1 | 0 | 1 | 100.00 | 33.33 | 100.00 | 0.5% Down |
| 1 | 1 | 0 | 400.00 | 33.33 | 100.00 | 0.5% Down |
| 1 | 1 | 1 | 200.00 | 33.33 | 100.00 | 0.5% Down |

## Pin Description

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| 1 | VDDPCI | PWR | Power supply for PCI clocks, nominal 3.3V |
| 2 | GND | PWR | Ground pin. |
| 3 | PCICLK1 | OUT | PCI clock output. |
| 4 | PCICLK2 | OUT | PCI clock output. |
| 5 | *SELPCIEX0_LCD#/PCICLK3 | #N/A | #N/A |
| 6 | GND | PWR | Ground pin. |
| 7 | VDDPCI | PWR | Power supply for PCI clocks, nominal 3.3V |
| 8 | ITP_EN/PCICLK_F4 | I/O | Free running PCI clock not affected by PCI_STOP#.<br>ITP_EN: latched input to select CPU_ITP/SRC output functionality<br>1 = CPU_ITP pair<br>0 = SRC pair |
| 9 | *SELLCD_27#/PCICLK_F5 | I/O | Free running PCI clock not affected by PCI_STOP#.<br>SELLCD_27#: latched input to select pin functionality. See Latch Select Table |
| 10 | VttPWR_GD/PD# | IN | This 3.3V LVTTL input is a level sensitive strobe used to determine when latch inputs are valid and are ready to be sampled. This is an active high input. / Asynchronous active low input pin used to power down the device into a low power state. |
| 11 | VDD48 | PWR | Power pin for the 48MHz output.3.3V |
| 12 | FSLA/USB_48MHz | I/O | 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. / Fixed 48MHz USB clock output. 3.3V. |
| 13 | GND | PWR | Ground pin. |
| 14 | PCIeT_L9/DOTT_96MHzL | OUT | True clock of 0.8V differential push-pull PCI_Express pair / True clock of differential DOT96 output pair. (no 50ohm resistor to GND needed) |
| 15 | PCIeC_L9/DOTC_96MHzL | OUT | Complement clock of 0.8V differential push-pull PCI_Express pair. / Complement clock of differential DOT96 push-pull output . (no 50ohm resistor to GND needed) |
| 16 | FSLB/TEST_MODE | IN | 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table. |
| 17 | 27FIX/LCD_SSCGT/PCIeT_L0 | OUT | 27MHz Non-Spread Push-Pull output / True clock of low power LCDCLK output / True clock of low power PCIEXCLK differential pair/ selected by SELPCIEX0_LCD# and SELLCD_27#. No 50ohm resistor to GND needed for differential outputs. |
| 18 | 27SS/LCD_SSCGC/PCIeC_L0 | OUT | 27MHz Spreading Push-Pull output / Complementary clock of LCDCLK_SS output / Complementary clock of PCIEXCLK differential pair/ selected by SELPCIEX0_LCD# and SELLCD_27#. No 50ohm resistor to GND needed for differential outputs. |
| 19 | PCIeT_L1 | OUT | True clock of 0.8V differential push-pull PCI_Express pair (no 50ohm resistor to GND needed) |
| 20 | PCIeC_L1 | OUT | Complement clock of 0.8V differential push-pull PCI_Express pair. (no 50ohm resistor to GND needed) |
| 21 | VDDPCIEX | PWR | Power supply for PCI Express clocks, nominal 3.3V |
| 22 | PCIeT_L2 | OUT | True clock of 0.8V differential push-pull PCI_Express pair (no 50ohm resistor to GND needed) |
| 23 | PCIeC_L2 | OUT | Complement clock of 0.8V differential push-pull PCI_Express pair. (no 50ohm resistor to GND needed) |
| 24 | PCIeT_L3 | OUT | True clock of 0.8V differential push-pull PCI_Express pair (no 50ohm resistor to GND needed) |
| 25 | PCIeC_L3 | OUT | Complement clock of 0.8V differential push-pull PCI_Express pair. (no 50ohm resistor to GND needed) |
| 26 | SATACLKT_L | OUT | True clock of 0.8V push-pull differential SATA pair. (no 50ohm resistor to GND needed) |
| 27 | SATACLKC_L | OUT | Complement clock of 0.8V push-pull differential SATA pair. (no 50ohm resistor to GND needed) |
| 28 | VDDPCIEX | PWR | Power supply for PCI Express clocks, nominal 3.3V |
| 29 | GND | PWR | Ground pin. |
| 30 | PCIeT_L4 | OUT | True clock of 0.8V differential push-pull PCI_Express pair (no 50ohm resistor to GND needed) |
| 31 | PCIeC_L4 | OUT | Complement clock of 0.8V differential push-pull PCI_Express pair. (no 50ohm resistor to GND needed) |
| 32 | *PEREQ3# | IN | Real-time input pin that controls PCIEXCLK outputs that are selected through the I2c. 1 = disabled, 0 = enabled. |

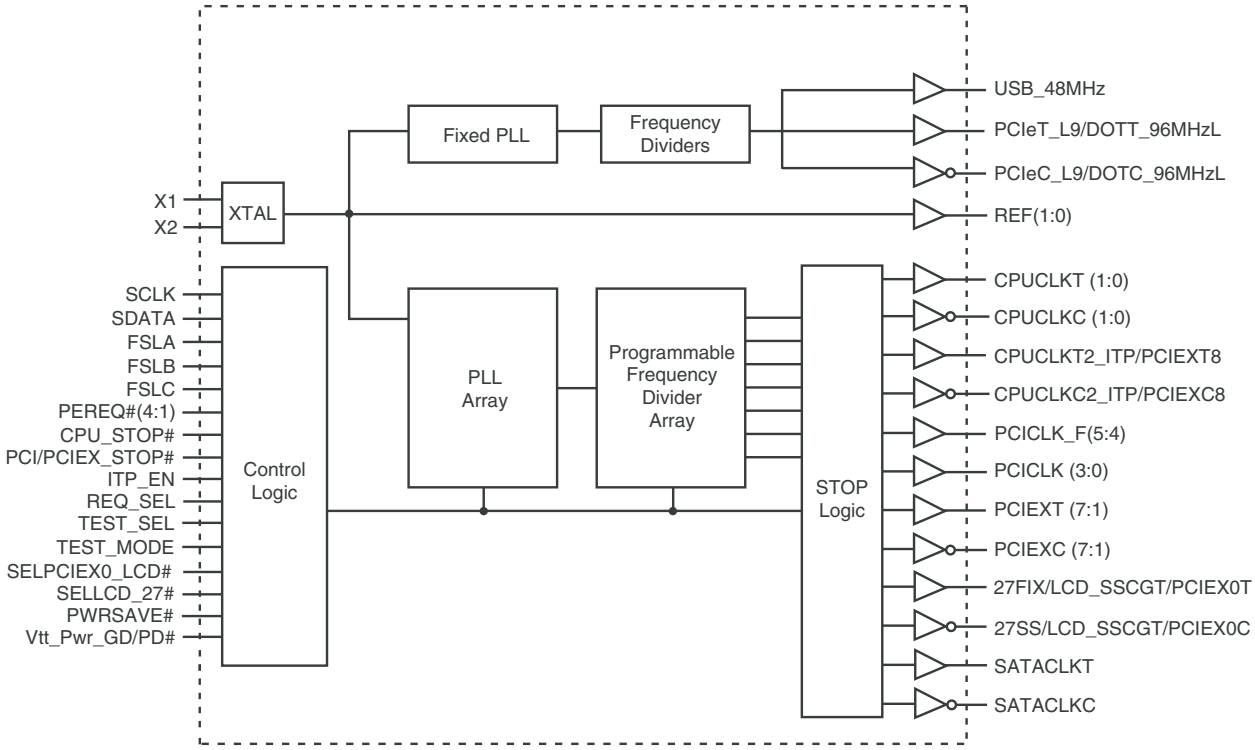
## Pin Description (Continued)

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| 33 | PEREQ4#* | IN | Real-time input pin that controls PCIEXCLK outputs that are selected through the I2c. 1 = disabled, 0 = enabled. |
| 34 | PWRSAVE#* | IN | Active-low input pin used to change frequency to underclocked entries in the ROM table that can be pre-programmed through Byte 6 of the I2c. |
| 35 | PCIeC_L5 | OUT | Complement clock of 0.8V differential push-pull PCI_Express pair. (no 50ohm resistor to GND needed) |
| 36 | PCIeT_L5 | OUT | True clock of 0.8V differential push-pull PCI_Express pair (no 50ohm resistor to GND needed) |
| 37 | GND | PWR | Ground pin. |
| 38 | PCIeC_L6 | OUT | Complement clock of 0.8V differential push-pull PCI_Express pair. (no 50ohm resistor to GND needed) |
| 39 | PCIeT_L6 | OUT | True clock of 0.8V differential push-pull PCI_Express pair (no 50ohm resistor to GND needed) |
| 40 | PEREQ2#/PCIeC_L7 | I/O | Real-time input pin that controls PCIEXCLK outputs that are selected through the I2c. 1 = disabled, 0 = enabled. / Complement clock of differential low power PCI Express output. No 50ohm resistor to GND needed. |
| 41 | PEREQ1#/PCIeT_L7 | I/O | Real-time input pin that controls PCIEXCLK outputs that are selected through the I2c. 1 = disabled, 0 = enabled. / True clock of differential low power PCI Express output. No 50ohm resistor to GND needed. |
| 42 | VDDPCIEX | PWR | Power supply for PCI Express clocks, nominal 3.3V |
| 43 | CPUITPC_L2/PCIeC_L8 | OUT | Complement clock of differential pair CPU output. / Complement clock of differential PCIEX pair. These are 0.8V push pull outputs. No 50ohm resistor to GND needed. |
| 44 | CPUITPT_L2/PCIeT_L8 | OUT | True clock of differential pair CPU output. / True clock of differential PCIEX pair. These are 0.8V push pull outputs. No 50ohm resistor to GND needed. |
| 45 | VDDA | PWR | 3.3V power for the PLL core. |
| 46 | GNDA | PWR | Ground pin for the PLL core. |
| 47 | VREF | PWR | Voltage reference for low power outputs. |
| 48 | CPUC_L1F | OUT | Complementary clock of differential pair of low power CPU outputs. Free running during iAMT. No 50ohm resistor to GND needed. |
| 49 | CPUT_L1F | OUT | True clock of differential pair of low power CPU outputs. Free running during iAMT. No 50ohm resistor to GND needed. |
| 50 | VDDCPU | PWR | Supply for CPU clocks, 3.3V nominal |
| 51 | CPUC_L0 | OUT | Complementary clock of differential pair 0.8V push-pull CPU outputs. No 50ohm resistor to GND needed. |
| 52 | CPUT_L0 | OUT | True clock of differential pair 0.8V push-pull CPU outputs. No 50ohm resistor to GND needed. |
| 53 | GND | PWR | Ground pin. |
| 54 | SCLK | IN | Clock pin of SMBus circuitry, 5V tolerant. |
| 55 | SDATA | I/O | Data pin for SMBus circuitry, 5V tolerant. |
| 56 | VDDREF | PWR | Ref, XTAL power supply, nominal 3.3V |
| 57 | X2 | OUT | Crystal output, Nominally 14.318MHz |
| 58 | X1 | IN | Crystal input, Nominally 14.318MHz. |
| 59 | GND | PWR | Ground pin. |
| 60 | REF0 | OUT | 14.318 MHz reference clock. |
| 61 | REF1/FSLC/TEST_SEL | I/O | 14.318 MHz reference clock./ 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. /TEST_Sel: 3-level latched input to enable test mode. Refer to Test Clarification Table |
| 62 | CPU_STOP# | IN | Stops all CPUCLK, except those set to be free running clocks |
| 63 | PCI/PCIEX_STOP# | IN | Stops all PCICLKs and PCIEXCLKs besides the free-running clocks at logic 0 level, when input low |
| 64 | PCICLK0/REQ_SEL** | I/O | 3.3V PCI clock output / Latch select input pin. 0 = PCIEXCLK, 1 = PEREQ# |

## General Description

**ICS9LPR363** is a low power CK505-compliant clock specification. This clock synthesizer provides a single chip solution for next generation P4 Intel processors and Intel chipsets. **ICS9LPR363** is driven with a 14.318MHz crystal.

## Block Diagram




Note: 1. VREF is not connected unless differential amplitude needs to be tuned

### Power Supply

| PIN NUMBER | | Description |
|---|---|---|
| VDD | GND | |
| 1,7 | 2,6 | PCICLK outputs |
| 11 | 13 | 48MHz,96Mhz, LCDCLK, Fix Digital, Fix Analog |
| 45 | 46 | Master clock, CPU Analog |
| 28, 42 | 21, 29, 37 | PCIEXT/C outputs |
| 50 | 53 | CPUT/C output |
| 56 | 59 | Xtal, REF |

## Differential Amplitude control using VREF.

Rpull-up: Connected between Vref and Vdd=3.3V;
Rpull-down: Connected between Vref and GND
Keep Rpull-up=1K ohm and variable Rpull-down to measure CPU and PCIEX Vtop

| Rpull-up (ohm) | Rpull-down (ohm) | CPU-T Vtop (mV) | PCIEX-T Vtop (mV) | SATA-T Vtop (mV) |
|---|---|---|---|---|
| 1K | 200 | 1155 | 1149 | 1136 |
| 1K | 221 | 1092 | 1060 | 1063 |
| 1K | 239 | 1054 | 1028 | 1040 |
| 1K | 270 | 996 | 991 | 984 |
| 1K | 301 | 943 | 946 | 931 |
| 1K | 330 | 924 | 913 | 912 |
| 1K | 360 | 898 | 888 | 885 |
| 1K | 375 | 871 | 860 | 865 |
| 1K | 390 | 867 | 837 | 822 |
| 1K | 414 | 812 | 822 | 801 |

*Measurement based on Vtop-avg
**Test board trace impedance is 50ohms

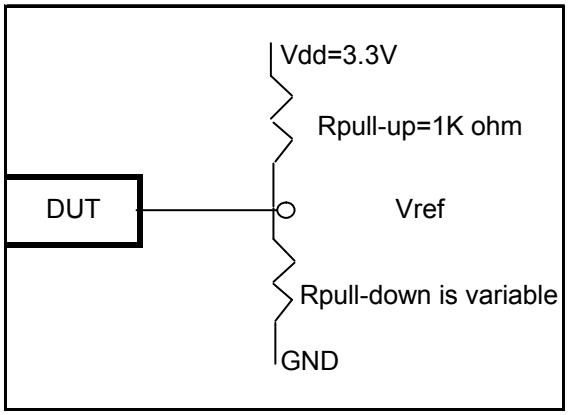


**Table 1: CPU/PCIEX Frequency Selection Table**

| FS4 | FS3 | $FS_LC$ | $FS_LB$ | $FS_LA$ | CPU MHz | PCI MHz | PCIEX MHz | Spread % |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 266.66 | 33.33 | 100.00 | 0.5% Down |
| 0 | 0 | 0 | 0 | 1 | 133.33 | 33.33 | 100.00 | 0.5% Down |
| 0 | 0 | 0 | 1 | 0 | 200.00 | 33.33 | 100.00 | 0.5% Down |
| 0 | 0 | 0 | 1 | 1 | 166.66 | 33.33 | 100.00 | 0.5% Down |
| 0 | 0 | 1 | 0 | 0 | 333.33 | 33.33 | 100.00 | 0.5% Down |
| 0 | 0 | 1 | 0 | 1 | 100.00 | 33.33 | 100.00 | 0.5% Down |
| 0 | 0 | 1 | 1 | 0 | 400.00 | 33.33 | 100.00 | 0.5% Down |
| 0 | 0 | 1 | 1 | 1 | 200.00 | 33.33 | 100.00 | 0.5% Down |
| 0 | 1 | 0 | 0 | 0 | 266.66 | 33.33 | 100.00 | +/- 0.25 Center |
| 0 | 1 | 0 | 0 | 1 | 133.33 | 33.33 | 100.00 | +/- 0.25 Center |
| 0 | 1 | 0 | 1 | 0 | 200.00 | 33.33 | 100.00 | +/- 0.25 Center |
| 0 | 1 | 0 | 1 | 1 | 166.66 | 33.33 | 100.00 | +/- 0.25 Center |
| 0 | 1 | 1 | 0 | 0 | 333.33 | 33.33 | 100.00 | +/- 0.25 Center |
| 0 | 1 | 1 | 0 | 1 | 100.00 | 33.33 | 100.00 | +/- 0.25 Center |
| 0 | 1 | 1 | 1 | 0 | 400.00 | 33.33 | 100.00 | +/- 0.25 Center |
| 0 | 1 | 1 | 1 | 1 | 200.00 | 33.33 | 100.00 | +/- 0.25 Center |
| 1 | 0 | 0 | 0 | 0 | 261.33 | 32.66 | 98 | +/- 0.25 Center |
| 1 | 0 | 0 | 0 | 1 | 130.66 | 32.66 | 98 | +/- 0.25 Center |
| 1 | 0 | 0 | 1 | 0 | 196.00 | 32.66 | 98 | +/- 0.25 Center |
| 1 | 0 | 0 | 1 | 1 | 163.33 | 32.66 | 98 | +/- 0.25 Center |
| 1 | 0 | 1 | 0 | 0 | 253.33 | 31.66 | 95 | +/- 0.25 Center |
| 1 | 0 | 1 | 0 | 1 | 126.66 | 31.66 | 95 | +/- 0.25 Center |
| 1 | 0 | 1 | 1 | 0 | 190.00 | 31.66 | 95 | +/- 0.25 Center |
| 1 | 0 | 1 | 1 | 1 | 158.33 | 31.66 | 95 | +/- 0.25 Center |
| 1 | 1 | 0 | 0 | 0 | 247.99 | 31.00 | 93 | +/- 0.25 Center |
| 1 | 1 | 0 | 0 | 1 | 124.00 | 31.00 | 93 | +/- 0.25 Center |
| 1 | 1 | 0 | 1 | 0 | 186.00 | 31.00 | 93 | +/- 0.25 Center |
| 1 | 1 | 0 | 1 | 1 | 154.99 | 31.00 | 93 | +/- 0.25 Center |
| 1 | 1 | 1 | 0 | 0 | 239.99 | 30.00 | 90 | +/- 0.25 Center |
| 1 | 1 | 1 | 0 | 1 | 120.00 | 30.00 | 90 | +/- 0.25 Center |
| 1 | 1 | 1 | 1 | 0 | 180.00 | 30.00 | 90 | +/- 0.25 Center |
| 1 | 1 | 1 | 1 | 1 | 149.99 | 30.00 | 90 | +/- 0.25 Center |

**Table2: LCDCLK Spread and Frequency Selection Table**

| SELDOT_27# | Byte 9b7 SS3 | Byte9b6 SS2 | Byte 9b5 SS1 | Byte 9b4 SS0 | Pin 17/18 | Spread | |
|---|---|---|---|---|---|---|---|
| | | | | | MHz | % | |
| 0 | 0 | 0 | 0 | 0 | 27.00 | +/-0.25 | Center |
| 0 | 0 | 0 | 0 | 1 | 27.00 | +/-0.50 | Center |
| 0 | 0 | 0 | 1 | 0 | 27.00 | +/-0.75 | Center |
| 0 | 0 | 0 | 1 | 1 | 27.00 | +/-1.0 | Center |
| 0 | 0 | 1 | 0 | 0 | 27.00 | +/-1.25 | Center |
| 0 | 0 | 1 | 0 | 1 | 27.00 | +/-1.5 | Center |
| 0 | 0 | 1 | 1 | 0 | 27.00 | +/-1.75 | Center |
| 0 | 0 | 1 | 1 | 1 | 27.00 | +/-2 | Center |
| 0 | 1 | 0 | 0 | 0 | 27.00 | -0.5 | Down |
| 0 | 1 | 0 | 0 | 1 | 27.00 | -1 | Down |
| 0 | 1 | 0 | 1 | 0 | 27.00 | -1.25 | Down |
| 0 | 1 | 0 | 1 | 1 | 27.00 | -1.5 | Down |
| 0 | 1 | 1 | 0 | 0 | 27.00 | -1.75 | Down |
| 0 | 1 | 1 | 0 | 1 | 27.00 | -2 | Down |
| 0 | 1 | 1 | 1 | 0 | 27.00 | -2.5 | Down |
| 0 | 1 | 1 | 1 | 1 | 27.00 | -3 | Down |
| 1 | 0 | 0 | 0 | 0 | 96.00 | +/-1.5 | Center |
| 1 | 0 | 0 | 0 | 1 | 96.00 | +/-1.25 | Center |
| 1 | 0 | 0 | 1 | 0 | 96.00 | +/-1.0 | Center |
| 1 | 0 | 0 | 1 | 1 | 96.00 | +/-0.8 | Center |
| 1 | 0 | 1 | 0 | 0 | 96.00 | +/-0.6 | Center |
| 1 | 0 | 1 | 0 | 1 | 96.00 | +/-0.5 | Center |
| 1 | 0 | 1 | 1 | 0 | 96.00 | +/-0.4 | Center |
| 1 | 0 | 1 | 1 | 1 | 96.00 | +/-0.3 | Center |
| 1 | 1 | 0 | 0 | 0 | 96.00 | 3 | Down |
| 1 | 1 | 0 | 0 | 1 | 96.00 | 2.5 | Down |
| 1 | 1 | 0 | 1 | 0 | 96.00 | 2 | Down |
| 1 | 1 | 0 | 1 | 1 | 96.00 | 1.75 | Down |
| 1 | 1 | 1 | 0 | 0 | 96.00 | 1.5 | Down |
| 1 | 1 | 1 | 0 | 1 | 96.00 | 1.25 | Down |
| 1 | 1 | 1 | 1 | 0 | 96.00 | 1 | Down |
| 1 | 1 | 1 | 1 | 1 | 96.00 | 0.8 | Down |

**Table3: SATA Spread and Frequency Selection Table**

| SEL_SATA | Byte 16b3 SS3 | Byte16b2 SS2 | Pin 27/26 | Spread | |
|---|---|---|---|---|---|
| | | | MHz | % | |
| 1 | 0 | 0 | 100.00 | -0.2 | Down |
| 1 | 0 | 1 | 100.00 | -0.3 | Down |
| 1 | 1 | 0 | 100.00 | -0.4 | Down |
| 1 | 1 | 1 | 100.00 | -0.5 | Down |

**CPU Power Management Table**

| PWRDWN# | CPU_STOP# | PCI_STOP# | PEREQ# | SMBus Register OE | CPU1 | CPU1# | CPU0 | CPU0# |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | |
| 1 | 1 | 1 | X | Enable | Running | Running | Running | Running |
| 0 | X | X | X | Enable | Low/20K | Low | Low/20K | Low |
| 1 | 0 | X | X | Enable | High | Low | High | Low |
| 1 | X | X | X | Disable | Low/20K | Low | Low/20K | Low |
| M1 | | | | | Running | Running | Low/20K | Low |

**PCIe, LCD, DOT Power Management Table**

| PWRDWN# | CPU_STOP# | PCI_STOP# | PEREQ# | | PCIe/LCD | PCIe#/LCD# | PCIe/LCD | PCIe#/LCD# | DOT | DOT# |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Free-Run | | PCI Stoppable/ PEREQ Selected | | | |
| 1 | X | 1 | 0 | Enable | Running | Running | Running | Running | Running | Running |
| 0 | X | X | X | Enable | Low/20K | Low | Low/20K | Low | Low/20K | Low |
| 1 | X | 0 | X | Enable | Running | Running | High | Low | Running | Running |
| 1 | X | X | 1 | Enable | Running | Running | Low/20K | Low | Running | Running |
| 1 | X | X | X | Disable | Low/20K | Low | Low/20K | Low | Low/20K | Low |
| M1 | | | | | Low/20K | Low | Low/20K | Low | Low/20K | Low |

**Singled-ended Power Management Table**

| PWRDWN# | CPU_STOP# | PCI_STOP# | PEREQ# | SMBus Register OE | PCIF/PCI | PCIF/PCI | USB | REF |
|---|---|---|---|---|---|---|---|---|
| | | | | | Free-run | Stoppable | | |
| 1 | X | 1 | X | Enable | Running | Running | Running | Running |
| 0 | X | X | X | Enable | Low | Low | Low | Low |
| 1 | X | 0 | X | Enable | Running | Low | Running | Running |
| 1 | X | X | X | Disable | Low | Low | Low | Low |
| M1 | | | | | Low | Low | Low | Low |

# General I²C serial interface information for the ICS9LPR363

## How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the beginning byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

## How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if X (H) was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

**Index Block Write Operation**

| Controller (Host) | | | ICS (Slave/Receiver) |
|---|---|---|---|
| T | starT bit | | |
| Slave Address D2(H) | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| Data Byte Count = X | | | |
| | | | ACK |
| Beginning Byte N | | X Byte | |
| | | | ACK |
| | ○ | | |
| | ○ | | ○ |
| | ○ | | ○ |
| | | | ○ |
| Byte N + X - 1 | | | |
| | | | ACK |
| P | stoP bit | | |

**Index Block Read Operation**

| Controller (Host) | | ICS (Slave/Receiver) | |
|---|---|---|---|
| T | starT bit | | |
| Slave Address D2(H) | | | |
| WR | WRite | | |
| | | ACK | |
| Beginning Byte = N | | | |
| | | ACK | |
| RT | Repeat starT | | |
| Slave Address D3(H) | | | |
| RD | ReaD | | |
| | | ACK | |
| | | | |
| | | Data Byte Count = X | |
| ACK | | | |
| | | X Byte | Beginning Byte N |
| ACK | | | |
| | | | ○ |
| | ○ | | ○ |
| | ○ | | ○ |
| | ○ | | |
| | | | Byte N + X - 1 |
| N | Not acknowledge | | |
| P | stoP bit | | |

**I2C Table: Output Control Register**

| Byte 0 | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | CPUCLK2_ITP/PCIEX8 Enable | Output Enable | RW | Disable (HiZ) | Enable | 1 |
| Bit 6 | PCIEX7 Enable | Output Enable | RW | Disable (HiZ) | Enable | 1 |
| Bit 5 | PCIEX5 Enable | Output Enable | RW | Disable (HiZ) | Enable | 1 |
| Bit 4 | PCIEX4 Enable | Output Enable | RW | Disable (HiZ) | Enable | 1 |
| Bit 3 | PCIEX3 Enable | Output Enable | RW | Disable (HiZ) | Enable | 1 |
| Bit 2 | PCIEX2 Enable | Output Enable | RW | Disable (HiZ) | Enable | 1 |
| Bit 1 | PCIEX1 Enable | Output Enable | RW | Disable (HiZ) | Enable | 1 |
| Bit 0 | LCD/PCIEX0 Enable | Output Enable | RW | Disable (HiZ) | Enable | 1 |

**I2C Table: Output Control Register**

| Byte 1 | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PCICLK_2 | Output Enable | RW | Disable | Enable | 1 |
| Bit 6 | PCIEX9/DOT_96MHz Enable | Output Enable | RW | Disable (HiZ) | Enable | 1 |
| Bit 5 | USB_48MHz Enable | Output Enable | RW | Disable | Enable | 1 |
| Bit 4 | REF1 Enable | Output Enable | RW | Disable | Enable | 1 |
| Bit 3 | PCIEX6 Enable | Output Enable | RW | Disable (HiZ) | Enable | 1 |
| Bit 2 | CPUCLK_1 Enable | Output Enable | RW | Disable (HiZ) | Enable | 1 |
| Bit 1 | CPUCLK_0 Enable | Output Enable | RW | Disable (HiZ) | Enable | 1 |
| Bit 0 | Spread Spectrum Mode (CPU, PCIEX, PCIF, PCI) | Spread Control for PLL1 | RW | SPREAD OFF | SPREAD ON | 1 |

**I2C Table: Output Control Register**

| Byte 2 | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PCICLK1 | Output Enable | RW | Disable | Enable | 1 |
| Bit 6 | PCICLK0 | Output Enable | RW | Disable | Enable | 1 |
| Bit 5 | PCICLK_F5 | Output Enable | RW | Disable | Enable | 1 |
| Bit 4 | PCICLK_F4 | Output Enable | RW | Disable | Enable | 1 |
| Bit 3 | PCICLK3 | Output Enable | RW | Disable | Enable | 1 |
| Bit 2 | 27MHz (Fixed) | Output Enable | RW | Disable | Enable | 1 |
| Bit 1 | 27MHz (SS) | Output Enable | RW | Disable | Enable | 1 |
| Bit 0 | SATACLK | Output Enable | RW | Disable (HiZ) | Enable | 1 |

**I2C Table: Output Control Register**

| Byte 3 | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PCIEX6 | Allow assertion of PCI_STOP# or setting of PCI_STOP control bit in I2C register to stop PCIEX clocks. | RW | Free-Running | Stoppable | 0 |
| Bit 6 | PCIEX5 | | RW | Free-Running | Stoppable | 0 |
| Bit 5 | PCIEX4 | | RW | Free-Running | Stoppable | 0 |
| Bit 4 | SATACLK | | RW | Free-Running | Stoppable | 0 |
| Bit 3 | PCIEX3 | | RW | Free-Running | Stoppable | 0 |
| Bit 2 | PCIEX2 | | RW | Free-Running | Stoppable | 0 |
| Bit 1 | PCIEX1 | | RW | Free-Running | Stoppable | 0 |
| Bit 0 | PCIEX0 | | RW | Free-Running | Stoppable | 0 |

**I2C Table: Output Control Register**

| Byte 4 | Name | Control Function | | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PCIEX7 | Free-Running Control | RW | Free-Running | Stoppable | 0 |
| Bit 6 | PCIEX9 | Free-Running Control | RW | Free-Running | Stoppable | 0 |
| Bit 5 | PCIEX8 | Free-Running Control | RW | Free-Running | Stoppable | 0 |
| Bit 4 | PCICLK_F5 | Allow assertion of PCI_STOP# or setting of PCI_STOP control bit in SMBus register to stop PCI clocks. | RW | Free-Running | Stoppable | 0 |
| Bit 3 | PCICLK_F4 | | RW | Free-Running | Stoppable | 0 |
| Bit 2 | CPUCLK_2/ITP | Allow assertion of CPU_STOP# to stop CPU clocks. | RW | Free-Running | Stoppable | 0 |
| Bit 1 | CPUCLK_1 | | RW | Free-Running | Stoppable | 0 |
| Bit 0 | CPUCLK_0 | | RW | Free-Running | Stoppable | 0 |

**I2C Table: Output Control Register**

| Byte 5 | Name | Control Function | | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | Reserved | RW | - | - | 0 |
| Bit 6 | PCICLK0 | Strength Control | RW | 1x | 2x | 0 |
| Bit 5 | Reserved | Reserved | RW | - | - | 0 |
| Bit 4 | Reserved | Reserved | RW | - | - | 0 |
| Bit 3 | Reserved | Reserved | RW | - | - | 0 |
| Bit 2 | PCICLK1 | Strength Control | RW | 1x | 2x | 0 |
| Bit 1 | Reserved | Reserved | RW | - | - | 0 |
| Bit 0 | Reserved | Reserved | RW | - | - | 0 |

**I2C Table: Frequency Select Register**

| Byte 6 | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PWRSAVE | PWR_SAVE programming | RW | IIC | PWR_SAVE programming | 0 |
| Bit 6 | FS4 | Frequency Select bit | RW | See Table 1: Frequency Selection Table | | 0 |
| Bit 5 | FS3 | Frequency Select bit | RW | | | 0 |
| Bit 4 | REF0 STRENGTH | Strength Prog | RW | 1X | 2X | 0 |
| Bit 3 | PCI/SRC_STOP# | Stop all PCI and SRC clocks | RW | Outputs Stopped | Outputs Active | 1 |
| Bit 2 | FSL_C | Frequency Select bit | RW | See Table 1: Frequency Selection Table | | latch |
| Bit 1 | FSL_B | Frequency Select bit | RW | | | latch |
| Bit 0 | FSL_A | Frequency Select bit | RW | | | latch |

**I2C Table: Revision and Vendor ID Register**

| Byte 7 | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | RID3 | Revision ID | R | - | - | 0 |
| Bit 6 | RID2 | | R | - | - | 0 |
| Bit 5 | RID1 | | R | - | - | 0 |
| Bit 4 | RID0 | | R | - | - | 0 |
| Bit 3 | VID3 | VENDOR ID | R | - | - | 0 |
| Bit 2 | VID2 | | R | - | - | 0 |
| Bit 1 | VID1 | | R | 001 = ICS | - | 0 |
| Bit 0 | VID0 | | R | - | - | 1 |

**I2C Table: PEREQ Control Register**

| Byte 8 | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PEREQ2# Control | PCIEX8 is controlled | RW | Not Controlled | Controlled | 0 |
| Bit 6 | PEREQ2# Control | PCIEX1 is controlled | RW | Not Controlled | Controlled | 0 |
| Bit 5 | iAMT_EN | Set via SMBus or dynamically by CK505 if detects dynamic M1 | RW | Legacy Mode | iAMT Enabled | 0 |
| Bit 4 | PD_Restore | If config saved, on deassert return to last known state else clear all config as if cold power on and go to latches open state | RW | Configuration Not Saved | Configuration Saved | 1 |
| Bit 3 | Reserved | Reserved | RW | - | - | 1 |
| Bit 2 | PEREQ1# Control | SATACLK is controlled | RW | Not Controlled | Controlled | 0 |
| Bit 1 | PEREQ1# Control | PCIEX6 is controlled | RW | Not Controlled | Controlled | 0 |
| Bit 0 | PEREQ1# Control | PCIEX0 is controlled | RW | Not Controlled | Controlled | 0 |

**I2C Table: LCDCLK and M/N Control Register**

| Byte 9 | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | LCDCLK_SS3 | Bit S3 | RW | See LCDCLK_SS and 27Mhz Spread Select Table 2 | | 0 |
| Bit 6 | LCDCLK_SS2 | Bit S2 | RW | | | 1 |
| Bit 5 | LCDCLK_SS1 | Bit S1 | RW | | | 1 |
| Bit 4 | LCDCLK_SS0 | Bit S0 | RW | | | 1 |
| Bit 3 | *SEL SRC_LCDCLK# | Selects SRC or LCD/27MHz on pins 17 and 18 | R | LCDCLK | PCIEX0 | latch |
| Bit 2 | REF 0 | Output Enable | RW | Disable | Enable | 1 |
| Bit 1 | LCDCLK_SS Spread Enable | Enable SS | RW | OFF | ON | 1 |
| Bit 0 | M/N Enable | PLL M/N Programming Enable | RW | Disable | Enable | 0 |

**I2C Table: Byte Count Register**

| Byte 10 | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | Reserved | RW | - | - | X |
| Bit 6 | Reserved | Reserved | RW | - | - | X |
| Bit 5 | Reserved | Reserved | RW | - | - | X |
| Bit 4 | BC4 | Byte Count Programming b(7:0) | RW | Writing to this register will configure how many bytes will be read back, default is 15 = 21 Bytes. | | 1 |
| Bit 3 | BC3 | | RW | | | 0 |
| Bit 2 | BC2 | | RW | | | 1 |
| Bit 1 | BC1 | | RW | | | 0 |
| Bit 0 | BC0 | | RW | | | 1 |

**I²C Table: PLL1 Frequency Control Register**

| Byte 11 | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | N Div8 | N Divider Prog bit 8 | RW | The decimal representation of M and N Divier in Byte 11 and 12 will configure the VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2] | | X |
| Bit 6 | N Div 9 | N Divider Prog bit 9 | RW | | | X |
| Bit 5 | M Div5 | M Divider Programming bits | RW | | | X |
| Bit 4 | M Div4 | | RW | | | X |
| Bit 3 | M Div3 | | RW | | | X |
| Bit 2 | M Div2 | | RW | | | X |
| Bit 1 | M Div1 | | RW | | | X |
| Bit 0 | M Div0 | | RW | | | X |

**I²C Table: PLL1 Frequency Control Register**

| Byte 12 | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | N Div7 | N Divider Programming b(8:0) | RW | The decimal representation of M and N Divier in Byte 11 and 12 will configure the VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2] | | X |
| Bit 6 | N Div6 | | RW | | | X |
| Bit 5 | N Div5 | | RW | | | X |
| Bit 4 | N Div4 | | RW | | | X |
| Bit 3 | N Div3 | | RW | | | X |
| Bit 2 | N Div2 | | RW | | | X |
| Bit 1 | N Div1 | | RW | | | X |
| Bit 0 | N Div0 | | RW | | | X |

**I²C Table: PLL1 Spread Spectrum Control Register**

| Byte 13 | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | SSP7 | Spread Spectrum Programming bit(7:0) | RW | These Spread Spectrum bits in Byte 13 and 14 will program the spread percentage of PLL1 | | X |
| Bit 6 | SSP6 | | RW | | | X |
| Bit 5 | SSP5 | | RW | | | X |
| Bit 4 | SSP4 | | RW | | | X |
| Bit 3 | SSP3 | | RW | | | X |
| Bit 2 | SSP2 | | RW | | | X |
| Bit 1 | SSP1 | | RW | | | X |
| Bit 0 | SSP0 | | RW | | | X |

**I²C Table: PLL1 Spread Spectrum Control Register**

| Byte 14 | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | Reserved | R | - | - | 0 |
| Bit 6 | SSP14 | Spread Spectrum Programming bit(14:8) | RW | These Spread Spectrum bits in Byte 13 and 14 will program the spread percentage of PLL1 | | X |
| Bit 5 | SSP13 | | RW | | | X |
| Bit 4 | SSP12 | | RW | | | X |
| Bit 3 | SSP11 | | RW | | | X |
| Bit 2 | SSP10 | | RW | | | X |
| Bit 1 | SSP9 | | RW | | | X |
| Bit 0 | SSP8 | | RW | | | X |

**I2C Table: PEREQ Control Register**

| Byte 15 | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | PEREQ4# Control | PCIEX7 is controlled | RW | Not Controlled | Controlled | 0 |
| Bit 6 | PEREQ4# Control | PCIEX5 is controlled | RW | Not Controlled | Controlled | 0 |
| Bit 5 | PEREQ4# Control | PCIEX3 is controlled | RW | Not Controlled | Controlled | 0 |
| Bit 4 | Reserved | Reserved | RW | - | - | 0 |
| Bit 3 | Reserved | Reserved | RW | - | - | 0 |
| Bit 2 | Reserved | Reserved | RW | - | - | 0 |
| Bit 1 | PEREQ3# Control | PCIEX4 is controlled | RW | Not Controlled | Controlled | 0 |
| Bit 0 | PEREQ3# Control | PCIEX2 is controlled | RW | Not Controlled | Controlled | 0 |

**I2C Table: SATACLK Control Register**

| Byte 16 | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | SEL_SATA | SATACLK Spread Control | RW | PCIEX PLL | SATA PLL | 1 |
| Bit 6 | SEL_LCD(27#) | Select LCD or 27MHz for pins 17 and 18 | RW | 27MHz/PCIEX9 | LCDCLK/DOT96 | latch |
| Bit 5 | PCIEX source | PCIEX comes from | RW | PCIEX PLL | SATA PLL | 0 |
| Bit 4 | SATA SS ENABLE | SPREAD ENABLE SATA PLL | RW | OFF | ON | 1 |
| Bit 3 | SATA_SS1 | Bit S1 | RW | See SATA_SS Frequency Select Table 3 | | 1 |
| Bit 2 | SATA_SS0 | Bit S0 | RW | | | 1 |
| Bit 1 | PCI source | PCI comes from | RW | PCIEX PLL | SATA PLL | 0 |
| Bit 0 | PCICLK2 | Strength Control | RW | 1x | 2x | 0 |

**I²C Table: PLL2 Frequency Control Register**

| Byte 17 | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | N Div8 | N Divider Prog bit 8 | RW | The decimal representation of M and N Divider in Byte 17 and 18 will configure the VCO frequency. Default at power up = Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2] | | X |
| Bit 6 | N Div9 | N Divider Prog bit 9 | RW | | | X |
| Bit 5 | M Div5 | M Divider Programming bits | RW | | | X |
| Bit 4 | M Div4 | | RW | | | X |
| Bit 3 | M Div3 | | RW | | | X |
| Bit 2 | M Div2 | | RW | | | X |
| Bit 1 | M Div1 | | RW | | | X |
| Bit 0 | M Div0 | | RW | | | X |

**I²C Table: PLL2 Frequency Control Register**

| Byte 18 | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | N Div7 | N Divider Programming b(8:0) | R | The decimal representation of M and N Divider in Byte 17 and 18 will configure the VCO frequency. Default at power up = Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2] | | X |
| Bit 6 | N Div6 | | RW | | | X |
| Bit 5 | N Div5 | | RW | | | X |
| Bit 4 | N Div4 | | RW | | | X |
| Bit 3 | N Div3 | | RW | | | X |
| Bit 2 | N Div2 | | RW | | | X |
| Bit 1 | N Div1 | | RW | | | X |
| Bit 0 | N Div0 | | RW | | | X |

**I2C Table: PLL 2 Spread Spectrum Control Register**

| Byte 19 | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | SSP7 | Spread Spectrum Programming b(7:0) | RW | These Spread Spectrum bits in Byte 19 and 20 will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming. | | X |
| Bit 6 | SSP6 | | RW | | | X |
| Bit 5 | SSP5 | | RW | | | X |
| Bit 4 | SSP4 | | RW | | | X |
| Bit 3 | SSP3 | | RW | | | X |
| Bit 2 | SSP2 | | RW | | | X |
| Bit 1 | SSP1 | | RW | | | X |
| Bit 0 | SSP0 | | RW | | | X |

**I2C Table: PLL 2 Spread Spectrum Control Register**

| Byte 20 | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | Reserved | RW | These Spread Spectrum bits in Byte 19 and 20 will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming. | | 0 |
| Bit 6 | SSP14 | Spread Spectrum Programming b(14:8) | RW | | | X |
| Bit 5 | SSP13 | | RW | | | X |
| Bit 4 | SSP12 | | RW | | | X |
| Bit 3 | SSP11 | | RW | | | X |
| Bit 2 | SSP10 | | RW | | | X |
| Bit 1 | SSP9 | | RW | | | X |
| Bit 0 | SSP8 | | RW | | | X |

## Test Clarification Table

| Comments | HW | | |
|---|---|---|---|
| | FSLC/ TEST_SEL HW PIN | FSLB/ TEST_MODE HW PIN | OUTPUT |
| | <1.14V | X | NORMAL |
| Power-up w/ TEST_SEL = 1 to enter test mode<br>Cycle power to disable test mode<br>FSLC./TEST_SEL -->3-level latched input<br>If power-up w/ V>1.14V then use TEST_SEL<br>If power-up w/ V<1.14V then use FSLC<br>FSLB/TEST_MODE -->low Vth input<br>TEST_MODE is a real time input | >1.14V | 0 | HI-Z |
| | >1.14V | 1 | REF/N |

## Absolute Maximum Ratings

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | Notes |
|---|---|---|---|---|---|---|
| Maximum Supply Voltage | VDDxxx | Supply Voltage | | 4.6 | V | 1,3 |
| Maximum Input Voltage | $V_{IH}$ | 3.3V LVCMOS Inputs | | 4.6 | V | 1,3,4 |
| Minimum Input Voltage | $V_{IL}$ | Any Input | GND - 0.5 | | V | 1,3 |
| Storage Temperature | Ts | - | -65 | 150 | °C | 1,3 |
| Case Temperature | Tcase | - | | 115 | °C | 1,3 |
| Input ESD protection | ESD prot | Human Body Model | 2000 | | V | 1,3 |

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Input frequency should be measured at the REF pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.

[3] Operation under these conditions is neither implied, nor guaranteed.

[4] Maximum input voltage is not to exceed VDD

## Electrical Characteristics - Input/Supply/Common Output Parameters

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | Notes |
|---|---|---|---|---|---|---|
| Ambient Operating Temp | Tambient | - | 0 | 70 | °C | 1 |
| Supply Voltage | VDDxxx | Supply Voltage | 3.135 | 3.465 | V | 1 |
| Input High Voltage | $V_{IHSE}$ | Single-ended inputs | 2 | $V_{DD}$ + 0.3 | V | 1 |
| Input Low Voltage | $V_{ILSE}$ | Single-ended inputs | $V_{SS}$ - 0.3 | 0.8 | V | 1 |
| Input Leakage Current | $I_{IN}$ | $V_{IN} = V_{DD}$ , $V_{IN}$ = GND | -5 | 5 | uA | 1 |
| Input Leakage Current | $I_{INRES}$ | Inputs with pull or pull down resistors $V_{IN} = V_{DD}$ , $V_{IN}$ = GND | -200 | 200 | uA | 1 |
| Output High Voltage | $V_{OHSE}$ | Single-ended outputs, $I_{OH}$ = -1mA | 2.4 | | V | 1 |
| Output Low Voltage | $V_{OLSE}$ | Single-ended outputs, $I_{OL}$ = 1 mA | | 0.4 | V | 1 |
| Output High Voltage | $V_{OHDIF}$ | Differential Outputs, $I_{OH}$ = TBD mA | | | V | 1 |
| Output Low Voltage | $V_{OLDIF}$ | Differential Outputs, $I_{OL}$ = TBD mA | | 0.4 | V | 1 |
| Low Threshold Input-High Voltage | $V_{IH\_FS}$ | 3.3 V +/-5% | 0.7 | $V_{DD}$ + 0.3 | V | 1 |
| Low Threshold Input-Low Voltage | $V_{IL\_FS}$ | 3.3 V +/-5% | $V_{SS}$ - 0.3 | 0.35 | V | 1 |
| Operating Supply Current | $I_{DD3.3OP}$ | Full Active, $C_L$ = Full load; | | TBD | mA | 1 |
| iAMT Mode Current | $I_{DDiAMT}$ | | | TBD | mA | 1 |
| Powerdown Current | $I_{DDPD}$ | | | TBD | mA | 1 |
| Input Frequency | $F_i$ | $V_{DD}$ = 3.3 V | | TBD | MHz | 2 |
| Pin Inductance | $L_{pin}$ | | | 7 | nH | 1 |
| Input Capacitance | $C_{IN}$ | Logic Inputs | 1.5 | 5 | pF | 1 |
| | $C_{OUT}$ | Output pin capacitance | | 6 | pF | 1 |
| | $C_{INX}$ | X1 & X2 pins | | TBD | pF | 1 |
| Clk Stabilization | $T_{STAB}$ | From VDD Power-Up or de-assertion of PD to 1st clock | | 1.8 | ms | 1 |
| | | | | | | |
| Tdrive_SRC | $T_{DRSRC}$ | SRC output enable after PCI_STOP# de-assertion | | 15 | ns | 1 |
| Tdrive_PD | $T_{DRPD}$ | Differential output enable after PD de-assertion | | 300 | us | 1 |
| Tdrive_CPU | $T_{DRSRC}$ | CPU output enable after PCI_STOP# de-assertion | | 10 | ns | 1 |
| Tfall_PD | $T_{FALL}$ | Fall/rise time of PD, PCI_STOP# and CPU_STOP# inputs | | 5 | ns | 1 |
| Trise_PD | $T_{RISE}$ | | | 5 | ns | |
| SMBus Voltage | $V_{DD}$ | | 2.7 | 5.5 | V | 1 |
| Low-level Output Voltage | $V_{OLSMB}$ | @ $I_{PULLUP}$ | | 0.4 | V | 1 |
| Current sinking at $V_{OLSMB}$ = 0.4 V | $I_{PULLUP}$ | SMB Data Pin | 4 | | mA | 1 |
| SCLK/SDATA Clock/Data Rise Time | $T_{RI2C}$ | (Max VIL - 0.15) to (Min VIH + 0.15) | | 1000 | ns | 1 |
| SCLK/SDATA Clock/Data Fall Time | $T_{FI2C}$ | (Min VIH + 0.15) to (Max VIL - 0.15) | | 300 | ns | 1 |
| Maximum SMBus Operating Frequency | $F_{SMBUS}$ | | | 100 | kHz | 1 |
| Spread Spectrum Modulation Frequency | $f_{SSMOD}$ | Triangular Modulation | 30 | 33 | kHz | 1 |

[1]Guaranteed by design and characterization, not 100% tested in production.

## AC Electrical Characteristics - Low Power Differential (CPUCLK, SATACLK, PCIEX, DOT96Mhz) Outputs

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Rising Edge Slew Rate | $t_{SLR}$ | Differential Measurement | 2.5 | 8 | V/ns | 1,2 |
| Falling Edge Slew Rate | $t_{FLR}$ | Differential Measurement | 2.5 | 8 | V/ns | 1,2 |
| Slew Rate Variation | $t_{SLVAR}$ | Single-ended Measurement | | 20 | % | 1 |
| Maximum Output Voltage | $V_{HIGH}$ | Includes overshoot | | 1150 | mV | 1 |
| Minimum Output Voltage | $V_{LOW}$ | Includes undershoot | -300 | | mV | 1 |
| Differential Voltage Swing | $V_{SWING}$ | Differential Measurement | 300 | | mV | 1 |
| Crossing Point Voltage | $V_{XABS}$ | Single-ended Measurement | 300 | 550 | mV | 1,3,4 |
| Crossing Point Variation | $V_{XABSVAR}$ | Single-ended Measurement | | 140 | mV | 1,3,5 |
| Duty Cycle | $D_{CYC}$ | Differential Measurement | 45 | 55 | % | 1 |
| CPU Jitter - Cycle to Cycle | $CPUJ_{C2C}$ | Differential Measurement | | 85 | ps | 1 |
| SRC Jitter - Cycle to Cycle | $SRCJ_{C2C}$ | Differential Measurement | | 125 | ps | 1 |
| DOT Jitter - Cycle to Cycle | $DOTJ_{C2C}$ | Differential Measurement | | 250 | ps | 1 |
| CPU[1:0] Skew | $CPU_{SKEW10}$ | Differential Measurement | | 100 | ps | 1 |
| CPU[2_ITP:0] Skew | $CPU_{SKEW20}$ | Differential Measurement | | 150 | ps | 1 |
| SRC[10:0] Skew | $SRC_{SKEW}$ | Differential Measurement | | TBD | ps | 1 |

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through Vswing centered around differential zero

[3] Vxabs is defined as the voltage where CLK = CLK#

[4] Only applies to the differential rising edge (CLK rising and CLK# falling)

[5] Defined as the total variation of all crossing voltages of CLK rising and CLK# falling. Matching applies to rising edge rate of CLK and falling edge of CLK#. It is measured using a +/-75mV window centered on the average cross point where CLK meets CLK#. The average cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

## Electrical Characteristics - PCICLK/PCICLK_F

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Long Accuracy | ppm | see Tperiod min-max values | -100 | 100 | ppm | 1,2 |
| Clock period | $T_{period}$ | 33.33MHz output nominal | 29.99100 | 30.00900 | ns | 2 |
| | | 33.33MHz output spread | | 30.15980 | ns | 2 |
| Absolute min/max period | $T_{abs}$ | 33.33MHz output nominal/spread | 29.49100 | 30.65980 | ns | 2 |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -1 mA | 2.4 | | V | 1 |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 1 mA | | 0.4 | V | 1 |
| Output High Current | $I_{OH}$ | $V_{OH}$@MIN = 1.0 V | -33 | | mA | 1 |
| | | $V_{OH}$@MAX = 3.135 V | | -33 | mA | 1 |
| Output Low Current | $I_{OL}$ | $V_{OL}$ @ MIN = 1.95 V | 30 | | mA | 1 |
| | | $V_{OL}$ @ MAX = 0.4 V | | 38 | mA | 1 |
| Rising Edge Slew Rate | $t_{SLR}$ | Measured from 0.8 to 2.0 V | 1 | 4 | V/ns | 1 |
| Falling Edge Slew Rate | $t_{FLR}$ | Measured from 2.0 to 0.8 V | 1 | 4 | V/ns | 1 |
| Duty Cycle | $d_{t1}$ | $V_T$ = 1.5 V | 45 | 55 | % | 1 |
| Skew | $t_{skew}$ | $V_T$ = 1.5 V | | TBD | ps | 1 |
| Jitter, Cycle to cycle | $t_{jcyc-cyc}$ | $V_T$ = 1.5 V | | 500 | ps | 1 |

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

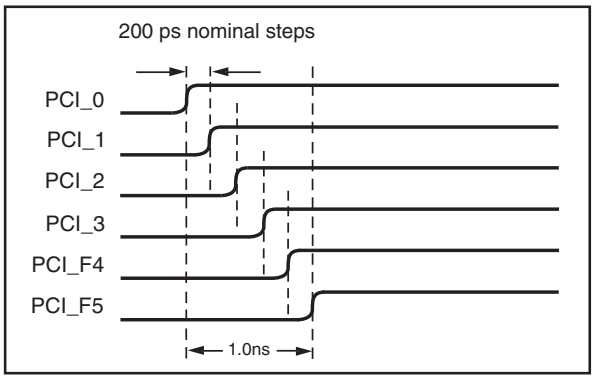
## Electrical Characteristics - USB48MHz

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Long Accuracy | ppm | see Tperiod min-max values | -100 | 100 | ppm | 1,2 |
| Clock period | $T_{period}$ | 48.00MHz output nominal | 20.83125 | 20.83542 | ns | 2 |
| Absolute min/max period | $T_{abs}$ | 48.00MHz output nominal | 20.48130 | 21.18540 | ns | 2 |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -1 mA | 2.4 | | V | 1 |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 1 mA | | 0.4 | V | 1 |
| Output High Current | $I_{OH}$ | $V_{OH}$ @MIN = 1.0 V | -29 | | mA | 1 |
| | | $V_{OH}$@MAX = 3.135 V | | -23 | mA | 1 |
| Output Low Current | $I_{OL}$ | $V_{OL}$ @ MIN = 1.95 V | 29 | | mA | 1 |
| | | $V_{OL}$ @ MAX = 0.4 V | | 27 | mA | 1 |
| Rising Edge Slew Rate | $t_{SLR}$ | Measured from 0.8 to 2.0 V | 1 | 2 | V/ns | 1 |
| Falling Edge Slew Rate | $t_{FLR}$ | Measured from 2.0 to 0.8 V | 1 | 2 | V/ns | 1 |
| Duty Cycle | $d_{t1}$ | $V_T$ = 1.5 V | 45 | 55 | % | 1 |
| Jitter, Cycle to cycle | $t_{jcyc-cyc}$ | $V_T$ = 1.5 V | | 350 | ps | 1 |

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

## Intentional PCI Clock to Clock Delay




## Electrical Characteristics - 27MHz

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | Notes |
|---|---|---|---|---|---|---|---|
| Long Accuracy | ppm | see Tperiod min-max values | -50 | 0 | 50 | ppm | 1,2 |
| | | | -15 | 0 | 15 | | 1,2,3 |
| Clock period | $T_{period}$ | 27.000MHz output nominal | 37.0365 | 37.0370 | 37.0376 | ns | 2 |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -1 mA | 2.4 | 3.25 | | V | 1 |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 1 mA | | 0.05 | 0.55 | V | 1 |
| Output High Current | $I_{OH}$ | $V_{OH}$ @MIN = 1.0 V | -29 | -73 | | mA | 1 |
| | | $V_{OH}$@MAX = 3.135 V | | -10 | -23 | mA | 1 |
| Output Low Current | $I_{OL}$ | $V_{OL}$ @ MIN = 1.95 V | 29 | 72 | | mA | 1 |
| | | $V_{OL}$ @ MAX = 0.4 V | | 27 | 27 | mA | 1 |
| Edge Rate | $t_{slewr/f}$ | Rising/Falling edge rate | 1 | 2.35 | 4 | V/ns | 1 |
| Rise Time | $t_{r1}$ | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V | 0.5 | 0.83333333 | 2 | ns | 1 |
| Fall Time | $t_{f1}$ | $V_{OH}$ = 2.4 V, $V_{OL}$ = 0.4 V | 0.5 | 0.86956522 | 2 | ns | 1 |
| Duty Cycle | $d_{t1}$ | $V_T$ = 1.5 V | 45 | 50.5 | 55 | % | 1 |
| Jitter | $t_{ltj}$ | Long Term (10us) | | 500 | 800 | ps | 1 |
| | $t_{jpk-pk}$ | | -250 | 117.5 | 250 | ps | 1 |
| | $t_{jcyc-cyc}$ | $V_T$ = 1.5 V | | 170 | 500 | ps | 1 |

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 20 pF with Rs = 7Ω

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3] At nominal voltage and temperature

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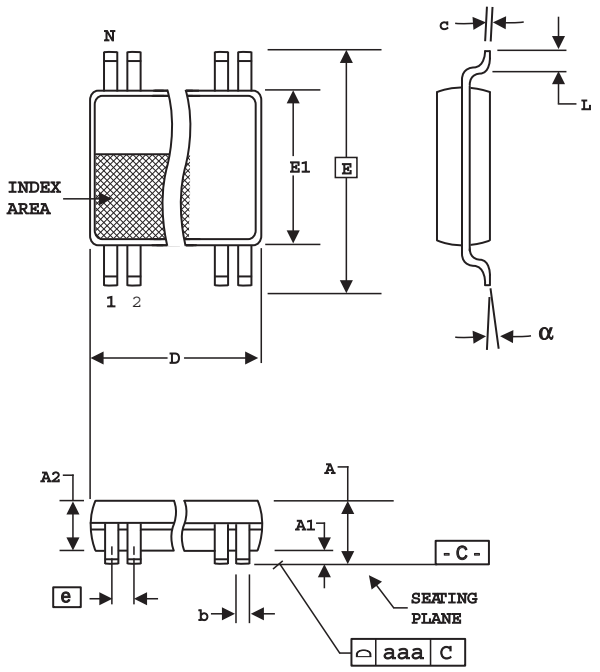
## Electrical Characteristics - REF-14.318MHz

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | Notes |
|---|---|---|---|---|---|---|
| Long Accuracy | ppm | see Tperiod min-max values | -100 | 100 | ppm | 1,2 |
| Clock period | $T_{period}$ | 14.318MHz output nominal | 69.8203 | 69.8622 | ns | 2 |
| Absolute min/max period | $T_{abs}$ | 14.318MHz output nominal | 69.8203 | 70.86224 | ns | 2 |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -1 mA | 2.4 | | V | 1 |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 1 mA | | 0.4 | V | 1 |
| Output High Current | $I_{OH}$ | $V_{OH}$ @MIN = 1.0 V, $V_{OH}$@MAX = 3.135 V | -33 | -33 | mA | 1 |
| Output Low Current | $I_{OL}$ | $V_{OL}$ @MIN = 1.95 V, $V_{OL}$ @MAX = 0.4 V | 30 | 38 | mA | 1 |
| Rising Edge Slew Rate | $t_{SLR}$ | Measured from 0.8 to 2.0 V | 1 | 4 | V/ns | 1 |
| Falling Edge Slew Rate | $t_{FLR}$ | Measured from 2.0 to 0.8 V | 1 | 4 | V/ns | 1 |
| Duty Cycle | $d_{t1}$ | $V_T$ = 1.5 V | 45 | 55 | % | 1 |
| Jitter | $t_{jcyc-cyc}$ | $V_T$ = 1.5 V | | 1000 | ps | 1 |

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz




**6.10 mm. Body, 0.50 mm. Pitch TSSOP**
**(240 mil) (20 mil)**

| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | -- | 1.20 | -- | .047 |
| A1 | 0.05 | 0.15 | .002 | .006 |
| A2 | 0.80 | 1.05 | .032 | .041 |
| b | 0.17 | 0.27 | .007 | .011 |
| c | 0.09 | 0.20 | .0035 | .008 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 8.10 BASIC | | 0.319 BASIC | |
| E1 | 6.00 | 6.20 | .236 | .244 |
| e | 0.50 BASIC | | 0.020 BASIC | |
| L | 0.45 | 0.75 | .018 | .030 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| α | 0° | 8° | 0° | 8° |
| aaa | -- | 0.10 | -- | .004 |

VARIATIONS

| N | D mm. | | D (inch) | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 64 | 16.90 | 17.10 | .665 | .673 |

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

## Ordering Information

**9LPR363yGLFT**

Example:

**XXXX** y **G** **LF** **T**

- **Designation for tape and reel packaging**
- **Lead Free, RoHS Compliant (Optional)**
- **Package Type**
  G = TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**

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(Rev.1.0 Mar 2020)


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