

General Description

The 9LPRS477D is a main clock synthesizer chip that provides all clocks required for ATI RD7xx-based systems using AMD processors. An SMBus interface allows full control of the device.

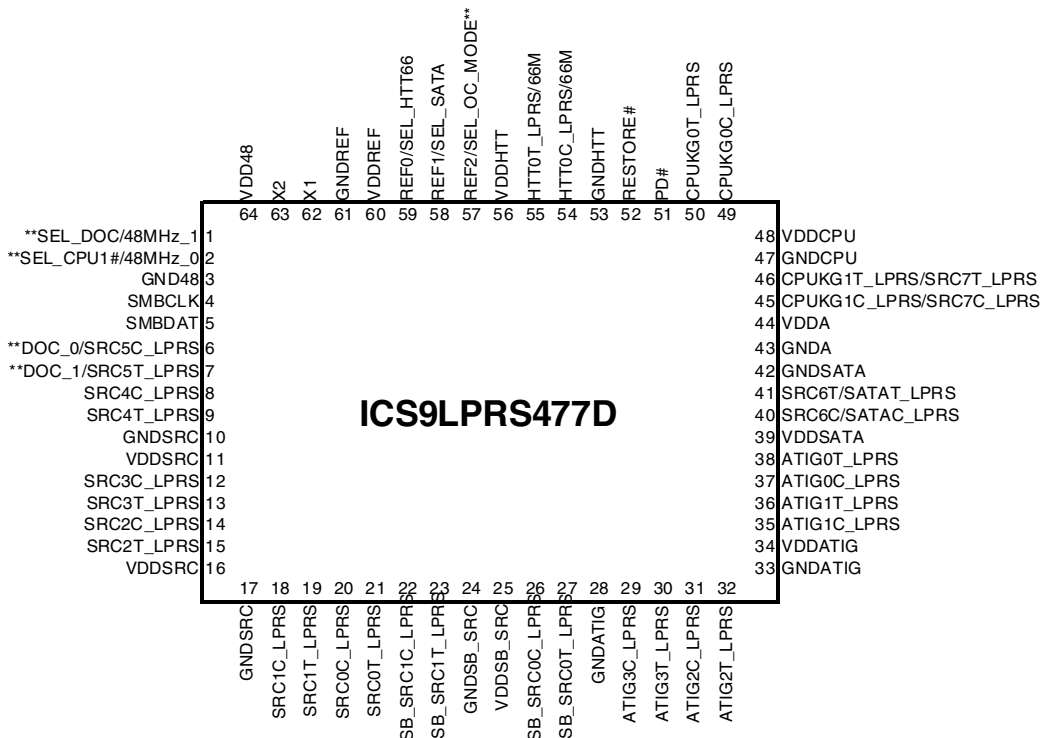
Recommended Application

ATI RS780/RS790/RD790/RS880 systems using AMD K8 processors

Output Features

- 2 - Greyhound compatible K8 CPU pairs
- 6 - low-power differential SRC pairs
- 2 - low-power differential SouthBridge SRC pairs
- 4 - low-power differential ATIG pairs
- 1 - Selectable low-power differential 100MHz non-spread SATA/ SRC output
- 1 - Selectable 100MHz low-power differential/ 66 MHz single-ended HTT clock
- 2 - 48MHz USB clocks
- 3 - 14.318MHz Reference clocks

Pin Configuration



64-Pin MLF

- * Internal Pull-Up Resistor
- ** Internal Pull-Down Resistor

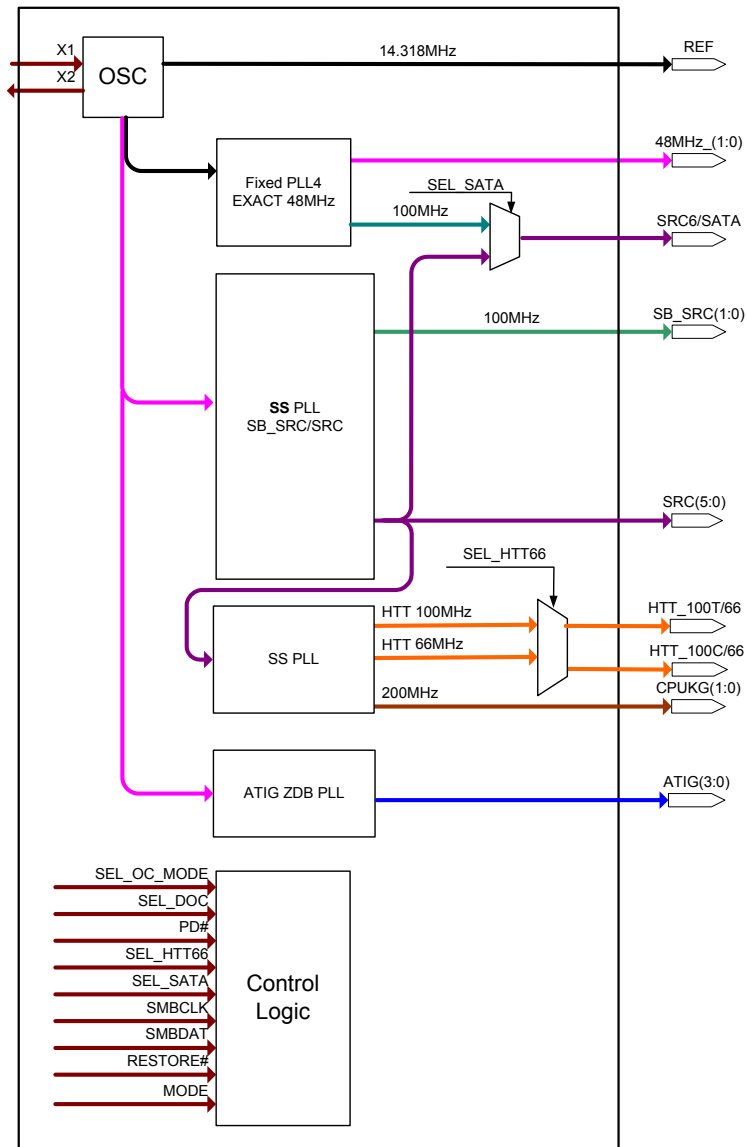
Pin Descriptions

| PIN # | PIN NAME | PIN TYPE | DESCRIPTION |
|-------|---------------------|----------|---|
| 1 | **SEL_DOC/48MHz_1 | I/O | SEL_DOC: latched input to select pin functionality 1 = DOC input. 0 = SRCCLK5 / 48MHz clock output. |
| 2 | **SEL_CPU1#/48MHz_0 | I/O | SEL_CPU1 latched input to select pin functionality 1 = SRCCLK7 0 = CPUKG1 / 48MHz clock output. |
| 3 | GND48 | GND | Ground pin for the 48MHz outputs |
| 4 | SMBCLK | IN | Clock pin of SMBus circuitry, 5V tolerant. |
| 5 | SMBDAT | I/O | Data pin for SMBus circuitry, 5V tolerant. |
| 6 | **DOC_0/SRC5C_LPRS | OUT | Dynamic Over Clocking pin: real time frequency selection 0: Normal; 1: Frequency will transition to a preprogrammed value in the I2c. / Complement clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) |
| 7 | **DOC_1/SRC5T_LPRS | OUT | Dynamic Over Clocking pin: real time frequency selection 0: Normal; 1: Frequency will transition to a preprogrammed value in the I2c. / True clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) |
| 8 | SRC4C_LPRS | OUT | Complement clock of low power differential SouthBridge SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) |
| 9 | SRC4T_LPRS | OUT | True clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) |
| 10 | GNDSRC | GND | Ground pin for the SRC outputs |
| 11 | VDDSRC | PWR | Supply for SRC core, 3.3V nominal |
| 12 | SRC3C_LPRS | OUT | Complement clock of low power differential SouthBridge SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) |
| 13 | SRC3T_LPRS | OUT | True clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) |
| 14 | SRC2C_LPRS | OUT | Complement clock of low power differential SouthBridge SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) |
| 15 | SRC2T_LPRS | OUT | True clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) |
| 16 | VDDSRC | PWR | Supply for SRC core, 3.3V nominal |
| 17 | GNDSRC | GND | Ground pin for the SRC outputs |
| 18 | SRC1C_LPRS | OUT | Complement clock of low power differential SouthBridge SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) |
| 19 | SRC1T_LPRS | OUT | True clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) |
| 20 | SRC0C_LPRS | OUT | Complement clock of low power differential SouthBridge SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) |
| 21 | SRC0T_LPRS | OUT | True clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) |
| 22 | SB_SRC1C_LPRS | OUT | Complement clock of low power differential SouthBridge SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) |
| 23 | SB_SRC1T_LPRS | OUT | True clock of low power differential SouthBridge SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) |
| 24 | GNDSB_SRC | GND | Ground pin for the SB_SRC outputs |
| 25 | VDDSB_SRC | PWR | Supply for SRC core, 3.3V nominal |
| 26 | SB_SRC0C_LPRS | OUT | Complement clock of low power differential SouthBridge SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) |
| 27 | SB_SRC0T_LPRS | OUT | True clock of low power differential SouthBridge SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) |
| 28 | GNDATIG | GND | Ground pin for the ATIG outputs |
| 29 | ATIG3C_LPRS | OUT | Complementary clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) |
| 30 | ATIG3T_LPRS | OUT | True clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) |
| 31 | ATIG2C_LPRS | OUT | Complementary clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) |
| 32 | ATIG2T_LPRS | OUT | True clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) |

Pin Descriptions (cont.)

| PIN # | PIN NAME | PIN TYPE | DESCRIPTION |
|-------|-------------------------|----------|---|
| 33 | GNDATIG | GND | Ground pin for the ATIG outputs |
| 34 | VDDATIG | PWR | Power supply for ATIG core, nominal 3.3V |
| 35 | ATIG1C_LPRS | OUT | Complementary clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) |
| 36 | ATIG1T_LPRS | OUT | True clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) |
| 37 | ATIG0C_LPRS | OUT | Complementary clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) |
| 38 | ATIG0T_LPRS | OUT | True clock of low-power differential push-pull PCI-Express pair with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) |
| 39 | VDDSATA | PWR | Power supply for SATA core logic, nominal 3.3V |
| 40 | SRC6C/SATAC_LPRS | OUT | Complement clock of low power differential SRC/SATA clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) |
| 41 | SRC6T/SATAT_LPRS | OUT | True clock of low power differential SRC/SATA clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) |
| 42 | GNDSATA | GND | Ground pin for the SRC outputs |
| 43 | GNDA | GND | Ground for the Analog Core |
| 44 | VDDA | PWR | 3.3V Power for the Analog Core |
| 45 | CPUKG1C_LPRS/SRC7C_LPRS | OUT | Complementary signal of low-power differential push-pull AMD K8 "Greyhound" clock with integrated series resistor. (no 33 ohm series resistor needed) / Complement clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) |
| 46 | CPUKG1T_LPRS/SRC7T_LPRS | OUT | True signal of low-power differential push-pull AMD K8 "Greyhound" clock with integrated series resistor. (no 33 ohm series resistor needed) / True clock of low power differential SRC clock pair. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) |
| 47 | GNDCPU | GND | Ground pin for the CPU outputs |
| 48 | VDDCPU | PWR | Supply for CPU core, 3.3V nominal |
| 49 | CPUKG0C_LPRS | OUT | Complementary signal of low-power differential push-pull AMD K8 "Greyhound" clock with integrated series resistor. (no 33 ohm series resistor needed) |
| 50 | CPUKG0T_LPRS | OUT | True signal of low-power differential push-pull AMD K8 "Greyhound" clock with integrated series resistor. (no 33 ohm series resistor needed) |
| 51 | PD# | IN | Enter /Exit Power Down. 0 = Power Down, 1 = normal operation. |
| 52 | RESTORE# | I/O | Open Drain I/O. As an input it restores the PLL's to power up default state. As an output, this signal is driven low when the internal watchdog hardware timer expires. It is cleared when the internal watchdog hardware timer is reset or disabled. The input is falling edge triggered. 0 = Restore Settings, 1 = normal operation. |
| 53 | GNDHTT | PWR | Ground pin for the HTT outputs |
| 54 | HTT0C_LPRS/66M | OUT | Complementary signal of low-power differential push-pull hypertransport clock with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) / 3.3V single ended 66MHz hyper transport clock |
| 55 | HTT0T_LPRS/66M | OUT | True signal of low-power differential push-pull hypertransport clock with integrated series resistor. (no 50ohm shunt resistor to GND and no 33 ohm series resistor needed) / 3.3V single ended 66MHz hyper transport clock |
| 56 | VDDHTT | PWR | Supply for HTT clocks, nominal 3.3V. |
| 57 | REF2/SEL_OC_MODE** | I/O | 14.318 MHz 3.3V reference clock / SEL_OC_MODE: latched input to select pin functionality 1 = ATIG/SRC PCIE Gen1 Mode with higher overclocking ability 0 = ATIG/SRC PCIE Gen2 Mode with limited overclocking ability |
| 58 | REF1/SEL_SATA | I/O | 14.318 MHz 3.3V reference clock / 3.3V tolerant latched input to select function of SRC6/SATA output 0 = 100MHz differential spreading SRC clock, 1 = 100MHz non-spreading differential SATA clock |
| 59 | REF0/SEL_HTT66 | I/O | 14.318 MHz 3.3V reference clock / 3.3V tolerant latched input to select Hyper Transport Clock Frequency. 0 = 100MHz differential HTT clock, 1 = 66MHz 3.3V single ended HTT clock |
| 60 | VDDREF | PWR | Ref, XTAL power supply, nominal 3.3V |
| 61 | GNDREF | GND | Ground pin for the REF outputs. |
| 62 | X1 | IN | Crystal input, nominally 14.318MHz |
| 63 | X2 | OUT | Crystal output, nominally 14.318MHz |
| 64 | VDD48 | PWR | Power pin for the 48MHz outputs and core. 3.3V |

Block Diagram



Power Groups

| Pin Number | | Description |
|------------|--------|------------------------------|
| VDD | GND | |
| 64 | 3 | USB_48 outputs |
| 11, 16 | 10, 17 | SRC differential outputs |
| 25 | 24 | SB_SRC differential outputs |
| 39 | 42 | SRC/SATA differential output |
| 34 | 28,33 | ATIG differential outputs |
| 44 | 43 | Analog, PLL |
| 48 | 47 | CPUKG differential outputs |
| 56 | 53 | HTTCLK output |
| 60 | 61 | REF outputs |

Differential Output Power Management Table

| PD# | CLKREQ# | SMBus Register OE | True output | Complement Output | True output | Complement Output |
|-----|---------|-------------------|-------------|-------------------|------------------|-------------------|
| | | | Free-Run | | CLKREQ# Selected | |
| 1 | 0 | Enable | Running | Running | Running | Running |
| 0 | X | X | Low/20K | Low | Low/20K | Low |
| 1 | 1 | Enable | Running | Running | Low/20K | Low |
| X | X | Disable | Low/20K | Low | Low/20K | Low |

Note: 20K means 20Kohm Pull Down

Singled-ended Power Management Table

| PD# | SMBus Register OE | USB | REF0, 1 | REF2 |
|-----|-------------------|---------|---------|---------|
| 1 | Enable | Running | Running | Running |
| 0 | Enable | Low | Hi-Z | Hi-Z |

Table1: CPU and HTT Frequency Selection Table

| Byte 3 | | | | | CPU (MHz) | HTT Single-ended | HTT Differential | Spread % (B6b6=1 and B3b5=1) | CPU OverClock % | CPU Output Divider | VCO |
|----------|----------|----------|----------|----------|---------------|------------------|------------------|------------------------------|-----------------|--------------------|---------------|
| Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | | SEL_HTT66 = 1 | SEL_HTT66 = 0 | | | | (MHz) |
| CPU FS4 | CPU FS3 | CPU FS2 | CPU FS1 | CPU FS0 | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 200.00 | 66.67 | 100.00 | | 0% | 2 | 400.00 |
| 0 | 0 | 0 | 0 | 1 | 205.00 | 68.33 | 102.50 | | 2% | 2 | 410.00 |
| 0 | 0 | 0 | 1 | 0 | 210.00 | 70.00 | 105.00 | | 5% | 2 | 420.00 |
| 0 | 0 | 0 | 1 | 1 | 215.00 | 71.67 | 107.50 | | 8% | 2 | 430.00 |
| 0 | 0 | 1 | 0 | 0 | 220.00 | 73.33 | 110.00 | | 10% | 2 | 440.00 |
| 0 | 0 | 1 | 0 | 1 | 225.00 | 75.00 | 112.50 | | 13% | 2 | 450.00 |
| 0 | 0 | 1 | 1 | 0 | 230.00 | 76.67 | 115.00 | | 15% | 2 | 460.00 |
| 0 | 0 | 1 | 1 | 1 | 235.00 | 78.33 | 117.50 | | 18% | 2 | 470.00 |
| 0 | 1 | 0 | 0 | 0 | 240.00 | 80.00 | 120.00 | | 20% | 2 | 480.00 |
| 0 | 1 | 0 | 0 | 1 | 245.00 | 81.67 | 122.50 | | 23% | 2 | 490.00 |
| 0 | 1 | 0 | 1 | 0 | 250.00 | 83.33 | 125.00 | | 25% | 2 | 500.00 |
| 0 | 1 | 0 | 1 | 1 | 255.00 | 85.00 | 127.50 | | 28% | 2 | 510.00 |
| 0 | 1 | 1 | 0 | 0 | 260.00 | 86.67 | 130.00 | | 30% | 2 | 520.00 |
| 0 | 1 | 1 | 0 | 1 | 265.00 | 88.33 | 132.50 | | 33% | 2 | 530.00 |
| 0 | 1 | 1 | 1 | 0 | 270.00 | 90.00 | 135.00 | | 35% | 2 | 540.00 |
| 0 | 1 | 1 | 1 | 1 | 200.00 | 66.67 | 100.00 | | 0% | 2 | 400.00 |
| 1 | 0 | 0 | 0 | 0 | 280.00 | 93.33 | 140.00 | | 40% | 2 | 560.00 |
| 1 | 0 | 0 | 0 | 1 | 285.00 | 95.00 | 142.50 | | 43% | 2 | 570.00 |
| 1 | 0 | 0 | 1 | 0 | 290.00 | 96.67 | 145.00 | | 45% | 2 | 580.00 |
| 1 | 0 | 0 | 1 | 1 | 295.00 | 98.33 | 147.50 | | 48% | 2 | 590.00 |
| 1 | 0 | 1 | 0 | 0 | 300.00 | 100.00 | 150.00 | | 50% | 2 | 600.00 |
| 1 | 0 | 1 | 0 | 1 | 305.00 | 101.67 | 152.50 | | 53% | 2 | 610.00 |
| 1 | 0 | 1 | 1 | 0 | 310.00 | 103.33 | 155.00 | | 55% | 2 | 620.00 |
| 1 | 0 | 1 | 1 | 1 | 315.00 | 105.00 | 157.50 | | 58% | 2 | 630.00 |
| 1 | 1 | 0 | 0 | 0 | 320.00 | 106.67 | 160.00 | | 60% | 2 | 640.00 |
| 1 | 1 | 0 | 0 | 1 | 325.00 | 108.33 | 162.50 | | 63% | 2 | 650.00 |
| 1 | 1 | 0 | 1 | 0 | 330.00 | 110.00 | 165.00 | | 65% | 2 | 660.00 |
| 1 | 1 | 0 | 1 | 1 | 335.00 | 111.67 | 167.50 | | 68% | 2 | 670.00 |
| 1 | 1 | 1 | 0 | 0 | 340.00 | 113.33 | 170.00 | | 70% | 2 | 680.00 |
| 1 | 1 | 1 | 0 | 1 | 345.00 | 115.00 | 172.50 | | 73% | 2 | 690.00 |
| 1 | 1 | 1 | 1 | 0 | 350.00 | 116.67 | 175.00 | | 75% | 2 | 700.00 |
| 1 | 1 | 1 | 1 | 1 | 355.00 | 118.33 | 177.50 | | 78% | 2 | 710.00 |

Depends on SB_SRC PLL. See Table 4.

Table 2: SRC Frequency Selection Table

| B12b3 | Byte 4 | | | | SRC (MHz) | Spread % (B6b5=1) | SRC OverClock % |
|-------------|-----------|-----------|-----------|-----------|---------------|-------------------------|-----------------------|
| | Bit3 | Bit2 | Bit1 | Bit0 | | | |
| OC Latch | SB FS3 | SB FS2 | SB FS1 | SB FS0 | | | |
| 0 | 0 | 0 | 0 | 0 | 100.00 | OFF ¹ | 0% |
| 0 | 0 | 0 | 0 | 1 | 101.00 | | 1% |
| 0 | 0 | 0 | 1 | 0 | 102.00 | | 2% |
| 0 | 0 | 0 | 1 | 1 | 103.00 | | 3% |
| 0 | 0 | 1 | 0 | 0 | 104.00 | | 4% |
| 0 | 0 | 1 | 0 | 1 | 105.00 | | 5% |
| 0 | 0 | 1 | 1 | 0 | 106.00 | | 6% |
| 0 | 0 | 1 | 1 | 1 | 107.00 | | 7% |
| 0 | 1 | 0 | 0 | 0 | 108.00 | | 8% |
| 0 | 1 | 0 | 0 | 1 | 109.00 | | 9% |
| 0 | 1 | 0 | 1 | 0 | 110.00 | | 10% |
| 0 | 1 | 0 | 1 | 1 | 111.00 | | 11% |
| 0 | 1 | 1 | 0 | 0 | 112.00 | | 12% |
| 0 | 1 | 1 | 0 | 1 | 113.00 | | 13% |
| 0 | 1 | 1 | 1 | 0 | 114.00 | 14% | |
| 0 | 1 | 1 | 1 | 1 | 100.00 | OFF | 0% |
| 1 | 0 | 0 | 0 | 0 | 100.00 | OFF ¹ | 0% |
| 1 | 0 | 0 | 0 | 1 | 101.00 | | 1% |
| 1 | 0 | 0 | 1 | 0 | 102.00 | | 2% |
| 1 | 0 | 0 | 1 | 1 | 103.00 | | 3% |
| 1 | 0 | 1 | 0 | 0 | 104.00 | | 4% |
| 1 | 0 | 1 | 0 | 1 | 105.00 | | 5% |
| 1 | 0 | 1 | 1 | 0 | 106.00 | | 6% |
| 1 | 0 | 1 | 1 | 1 | 107.00 | | 7% |
| 1 | 1 | 0 | 0 | 0 | 108.00 | | 8% |
| 1 | 1 | 0 | 0 | 1 | 109.00 | | 9% |
| 1 | 1 | 0 | 1 | 0 | 110.00 | | 10% |
| 1 | 1 | 0 | 1 | 1 | 111.00 | | 11% |
| 1 | 1 | 1 | 0 | 0 | 112.00 | | 12% |
| 1 | 1 | 1 | 0 | 1 | 113.00 | | 13% |
| 1 | 1 | 1 | 1 | 0 | 114.00 | 14% | |
| 1 | 1 | 1 | 1 | 1 | 100.00 | OFF | 0% |

Note ¹: After SRC SS_EN bit is enabled through SMBus Byte 6 bit 5, there will be no spread for SRC's by default. To obtain spread spectrum on SRC outputs, please program Byte23 & Byte24.

To pass USB3.0, please use below reference SMBus setting:

| Byte Setting | Description |
|--------------|--|
| B4=E0h | Change SRC to FS0000 Frequency Setting |
| B6=2Fh | Enable SRC Spread Spectrum |
| B12=45h | SRC MN Enable |
| B21=8Ch | Set SRC M Div |
| B22=68h | Set SRC N Div |
| B23=1Ah | Set SRC Spread % |
| B24=3Eh | Set SRC Spread % |

* Actual word used can deviate from above table pending usage

Table3: ATIG Frequency Selection Table

| B12b4 | Byte 5 | | | | ATIG(3:0) (MHz) | Spread % (B6b7=1) | ATIG OverClock % | ATIG Output Divider | VCO (MHz) |
|----------|---------------------|-------------------|-------------------|--------------------------------|--------------------|-------------------------|---------------------|---------------------------|----------------|
| | Bit3 OC Latch | Bit2 SB FS3 | Bit1 SB FS2 | Bit0 SB FS1 SB FS0 | | | | | |
| 0 | 0 | 0 | 0 | 0 | 100.00 | -0.50% | 0% | 10 | 1000.00 |
| 0 | 0 | 0 | 0 | 1 | 101.00 | | 1% | 10 | 1010.00 |
| 0 | 0 | 0 | 1 | 0 | 102.00 | | 2% | 10 | 1020.00 |
| 0 | 0 | 0 | 1 | 1 | 103.00 | | 3% | 10 | 1030.00 |
| 0 | 0 | 1 | 0 | 0 | 104.00 | | 4% | 10 | 1040.00 |
| 0 | 0 | 1 | 0 | 1 | 105.00 | | 5% | 10 | 1050.00 |
| 0 | 0 | 1 | 1 | 0 | 106.00 | | 6% | 10 | 1060.00 |
| 0 | 0 | 1 | 1 | 1 | 107.00 | | 7% | 10 | 1070.00 |
| 0 | 1 | 0 | 0 | 0 | 108.00 | | 8% | 10 | 1080.00 |
| 0 | 1 | 0 | 0 | 1 | 109.00 | | 9% | 10 | 1090.00 |
| 0 | 1 | 0 | 1 | 0 | 110.00 | | 10% | 10 | 1100.00 |
| 0 | 1 | 0 | 1 | 1 | 111.00 | | 11% | 10 | 1110.00 |
| 0 | 1 | 1 | 0 | 0 | 112.00 | | 12% | 10 | 1120.00 |
| 0 | 1 | 1 | 0 | 1 | 113.00 | | 13% | 10 | 1130.00 |
| 0 | 1 | 1 | 1 | 0 | 114.00 | 14% | 10 | 1140.00 | |
| 0 | 1 | 1 | 1 | 1 | 100.00 | OFF | 0% | 10 | 1000.00 |
| 1 | 0 | 0 | 0 | 0 | 100.00 | -0.50% | 0% | 8 | 800.00 |
| 1 | 0 | 0 | 0 | 1 | 101.00 | | 1% | 8 | 808.00 |
| 1 | 0 | 0 | 1 | 0 | 102.00 | | 2% | 8 | 816.00 |
| 1 | 0 | 0 | 1 | 1 | 103.00 | | 3% | 8 | 824.00 |
| 1 | 0 | 1 | 0 | 0 | 104.00 | | 4% | 8 | 832.00 |
| 1 | 0 | 1 | 0 | 1 | 105.00 | | 5% | 8 | 840.00 |
| 1 | 0 | 1 | 1 | 0 | 106.00 | | 6% | 8 | 848.00 |
| 1 | 0 | 1 | 1 | 1 | 107.00 | | 7% | 8 | 856.00 |
| 1 | 1 | 0 | 0 | 0 | 108.00 | | 8% | 8 | 864.00 |
| 1 | 1 | 0 | 0 | 1 | 109.00 | | 9% | 8 | 872.00 |
| 1 | 1 | 0 | 1 | 0 | 110.00 | | 10% | 8 | 880.00 |
| 1 | 1 | 0 | 1 | 1 | 111.00 | | 11% | 8 | 888.00 |
| 1 | 1 | 1 | 0 | 0 | 112.00 | | 12% | 8 | 896.00 |
| 1 | 1 | 1 | 0 | 1 | 113.00 | | 13% | 8 | 904.00 |
| 1 | 1 | 1 | 1 | 0 | 114.00 | 14% | 8 | 912.00 | |
| 1 | 1 | 1 | 1 | 1 | 100.00 | OFF | 0% | 8 | 800.00 |

Table4: SB_SRC Frequency Selection Table

| Byte 6 | | | | | SB_SRC (1:0) (MHz) | Spread % (B6b6=1) | SB_SRC OverClock % | SB_SRC Output Divider | VCO (MHz) |
|------------|------------|------------|------------|------------|--------------------------|-------------------------|--------------------------|-----------------------------|--------------|
| Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | | | | | |
| SRC FS4 | SRC FS3 | SRC FS2 | SRC FS1 | SRC FS0 | | | | | |
| 0 | 0 | 0 | 0 | 0 | 85.00 | -0.50% | -15% | 10 | 850.00 |
| 0 | 0 | 0 | 0 | 1 | 86.00 | | -14% | 10 | 860.00 |
| 0 | 0 | 0 | 1 | 0 | 87.00 | | -13% | 10 | 870.00 |
| 0 | 0 | 0 | 1 | 1 | 88.00 | | -12% | 10 | 880.00 |
| 0 | 0 | 1 | 0 | 0 | 89.00 | | -11% | 10 | 890.00 |
| 0 | 0 | 1 | 0 | 1 | 90.00 | | -10% | 10 | 900.00 |
| 0 | 0 | 1 | 1 | 0 | 91.00 | | -9% | 10 | 910.00 |
| 0 | 0 | 1 | 1 | 1 | 92.00 | | -8% | 10 | 920.00 |
| 0 | 1 | 0 | 0 | 0 | 93.00 | | -7% | 10 | 930.00 |
| 0 | 1 | 0 | 0 | 1 | 94.00 | | -6% | 10 | 940.00 |
| 0 | 1 | 0 | 1 | 0 | 95.00 | | -5% | 10 | 950.00 |
| 0 | 1 | 0 | 1 | 1 | 96.00 | | -4% | 10 | 960.00 |
| 0 | 1 | 1 | 0 | 0 | 97.00 | | -3% | 10 | 970.00 |
| 0 | 1 | 1 | 0 | 1 | 98.00 | | -2% | 10 | 980.00 |
| 0 | 1 | 1 | 1 | 0 | 99.00 | | -1% | 10 | 990.00 |
| 0 | 1 | 1 | 1 | 1 | 100.00 | | OFF | 0% | 10 |
| 1 | 0 | 0 | 0 | 0 | 100.00 | -0.50% | 0% | 10 | 1000.00 |
| 1 | 0 | 0 | 0 | 1 | 101.00 | | 1% | 10 | 1010.00 |
| 1 | 0 | 0 | 1 | 0 | 102.00 | | 2% | 10 | 1020.00 |
| 1 | 0 | 0 | 1 | 1 | 103.00 | | 3% | 10 | 1030.00 |
| 1 | 0 | 1 | 0 | 0 | 104.00 | | 4% | 10 | 1040.00 |
| 1 | 0 | 1 | 0 | 1 | 105.00 | | 5% | 10 | 1050.00 |
| 1 | 0 | 1 | 1 | 0 | 106.00 | | 6% | 10 | 1060.00 |
| 1 | 0 | 1 | 1 | 1 | 107.00 | | 7% | 10 | 1070.00 |
| 1 | 1 | 0 | 0 | 0 | 108.00 | | 8% | 10 | 1080.00 |
| 1 | 1 | 0 | 0 | 1 | 109.00 | | 9% | 10 | 1090.00 |
| 1 | 1 | 0 | 1 | 0 | 110.00 | | 10% | 10 | 1100.00 |
| 1 | 1 | 0 | 1 | 1 | 111.00 | | 11% | 10 | 1110.00 |
| 1 | 1 | 1 | 0 | 0 | 112.00 | | 12% | 10 | 1120.00 |
| 1 | 1 | 1 | 0 | 1 | 113.00 | | 13% | 10 | 1130.00 |
| 1 | 1 | 1 | 1 | 0 | 114.00 | | 14% | 10 | 1140.00 |
| 1 | 1 | 1 | 1 | 1 | 115.00 | 15% | 10 | 1150.00 | |

NOTE: All frequencies assume that the SB_SRC are at 0% Overclocking.

Table 5: IO_Vout select table

| B12b2 | B12b1 | B12b0 | IO_Vout |
|----------|----------|----------|-------------|
| 0 | 0 | 0 | 0.3V |
| 0 | 0 | 1 | 0.4V |
| 0 | 1 | 0 | 0.5V |
| 0 | 1 | 1 | 0.6V |
| 1 | 0 | 0 | 0.7V |
| 1 | 0 | 1 | 0.8V |
| 1 | 1 | 0 | 0.9V |
| 1 | 1 | 1 | 1.0V |

Bold Entry is Power up Default

General SMBus Serial Interface Information for 9LPRS477D

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte N through Byte N+X-1
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

| Index Block Write Operation | | | |
|-----------------------------|-----------|----------------------|-----|
| Controller (Host) | | IDT (Slave/Receiver) | |
| T | starT bit | | |
| Slave Address | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| Data Byte Count = X | | | |
| | | | ACK |
| Beginning Byte N | | X Byte | |
| | | | ACK |
| O | | | O |
| O | | | O |
| | | | O |
| Byte N + X - 1 | | | |
| | | | ACK |
| P | stoP bit | | |

| Read Address | Write Address |
|-------------------|-------------------|
| D3 _(H) | D2 _(H) |

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte N+X-1
- IDT clock sends **Byte 0 through Byte X (if X_(H) was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation | | | |
|----------------------------|-----------------|----------------------|-------------------|
| Controller (Host) | | IDT (Slave/Receiver) | |
| T | starT bit | | |
| Slave Address | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| RT | Repeat starT | | |
| Slave Address | | | |
| RD | ReaD | | |
| | | | ACK |
| | | | |
| ACK | | | Data Byte Count=X |
| | | | |
| ACK | | X Byte | Beginning Byte N |
| | | | O |
| O | | | O |
| O | | | O |
| | | | |
| ACK | | | Byte N + X - 1 |
| N | Not acknowledge | | |
| P | stoP bit | | |

SMBus Table: Latched Input Readback Output Enable Control Register

| Byte | 0 | Name | Description | Type | 0 | 1 | Default |
|-------|--------------------|------|-----------------------|------|---|--|---------|
| Bit 7 | SEL_HTT66 readback | | Hypertransport Select | R | 100MHz Differential HTT clock | 66 MHz 3.3V Single-ended HTT clock | Latch |
| Bit 6 | SEL_SATA readback | | SATA Select | R | SRC6/SATA pair is SRC SS capable output | SRC6/SATA pair is SATA non-spread output | Latch |
| Bit 5 | REF0_OE | | Output Enable | RW | Hi-Z | Enabled | 1 |
| Bit 4 | REF1_OE | | Output Enable | RW | Hi-Z | Enabled | 1 |
| Bit 3 | REF2_OE | | Output Enable | RW | Hi-Z | Enabled | 1 |
| Bit 2 | 48MHz_1_OE | | Output Enable | RW | Low | Enabled | 1 |
| Bit 1 | 48MHz_0_OE | | Output Enable | RW | Low | Enabled | 1 |
| Bit 0 | SEL_CPU1 readback | | CPU1/SRC7 Select | R | CPU1 Differential output | SRC7 Differential output | Latch |

SMBus Table: Output Enable Control Register

| Byte | 1 | Name | Control Function | Type | 0 | 1 | Default |
|-------|---------------------|------|------------------|------|--------------------------|---------|---------|
| Bit 7 | SEL_DOC readback | | DOC Select | R | SRC5 Differential output | DOC | Latch |
| Bit 6 | SRC6/SATA_OE Enable | | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 5 | SRC5_OE | | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 4 | SRC4_OE | | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 3 | SRC3_OE | | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 2 | SRC2_OE | | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 1 | SRC1_OE | | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 0 | SRC0_OE | | Output Enable | RW | Low/Low | Enabled | 1 |

SMBus Table: Output Enable and 48MHz Strength Control Register

| Byte | 2 | Name | Control Function | Type | 0 | 1 | Default |
|-------|------------------|-----------------------------|------------------|--------|---------|---------|---------|
| Bit 7 | SB_SRC1_OE | | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 6 | SB_SRC0_OE | | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 5 | ATIG3_OE | | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 4 | ATIG2_OE | | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 3 | ATIG1_OE | | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 2 | ATIG0_OE | | Output Enable | RW | Low/Low | Enabled | 1 |
| Bit 1 | 48MHz_1_Strength | 48MHz_1 Drive Strength Sel. | RW | 1 Load | 2 Load | 1 | |
| Bit 0 | 48MHz_0_Strength | 48MHz_0 Drive Strength Sel. | RW | 1 Load | 2 Load | 1 | |

SMBus Table: CPU/HTT Frequency Control Register

| Byte | 3 | Name | Control Function | Type | 0 | 1 | Default |
|-------|-------------------|--------------------------|------------------|--|------------|--------|---------|
| Bit 7 | CPU1_OE/SRC7_OE | | Output enable | RW | Low/Low | Enable | 1 |
| Bit 6 | CPU0_OE | | Output enable | RW | Low/Low | Enable | 1 |
| Bit 5 | CPU Spread Source | CPU Spread Source | RW | Fix PLL | SB_SRC PLL | 1 | |
| Bit 4 | CPU_FS4 | CPU Frequency Select MSB | RW | See CPU Frequency Select Table Default value corresponds to 200MHz. Note that Selected HTT frequency tracks the CPU frequency. | | 0 | |
| Bit 3 | CPU_FS3 | CPU Frequency Select | RW | | 1 | | |
| Bit 2 | CPU_FS2 | CPU Frequency Select | RW | | 1 | | |
| Bit 1 | CPU_FS1 | CPU Frequency Select | RW | | 1 | | |
| Bit 0 | CPU_FS0 | CPU Frequency Select LSB | RW | | 1 | | |

SMBus Table: SRC Frequency Control Register

| Byte | 4 | Name | Control Function | Type | 0 | 1 | Default |
|-------|---------------|--------------------------|------------------|--------------------------------|--------|---|---------|
| Bit 7 | REF0_Strength | REF0_Drive Strength Sel | RW | 1 Load | 2 Load | 1 | |
| Bit 6 | REF1_Strength | REF1_Drive Strength Sel | RW | 1 Load | 2 Load | 1 | |
| Bit 5 | REF2_Strength | REF2_Drive Strength Sel | RW | 1 Load | 2 Load | 1 | |
| Bit 4 | | Reserved | | | | 0 | |
| Bit 3 | SRC_FS3 | SRC Frequency Select | RW | See SRC Frequency Select Table | | 1 | |
| Bit 2 | SRC_FS2 | SRC Frequency Select | RW | | 1 | | |
| Bit 1 | SRC_FS1 | SRC Frequency Select | RW | | 1 | | |
| Bit 0 | SRC_FS0 | SRC Frequency Select LSB | RW | | 1 | | |

SMBus Table: ATIG Frequency Select Register

| Byte | 5 | Name | Control Function | Type | 0 | 1 | Default |
|-------|---------------|--|-----------------------|---------------------------------|-------------|--------|---------|
| Bit 7 | ATIG_PLL_TBEN | | ATIG PLL Turbo Enable | RW | Disable | Enable | 0 |
| Bit 6 | CPU_PLL_TBEN | | CPU PLL Turbo Enable | RW | Disable | Enable | 0 |
| Bit 5 | SRC_PLL_TBEN | | SRC PLL Turbo Enable | RW | Disable | Enable | 0 |
| Bit 4 | DISABLE_ORT | Disable \underline{Q} overshoot \underline{R} eduction Technology during CPU PLL M/N Programming | RW | ENABLE ORT | DISABLE ORT | 0 | |
| Bit 3 | ATIG_FS3 | ATIG Frequency Select | RW | See ATIG Frequency Select Table | | 1 | |
| Bit 2 | ATIG_FS2 | ATIG Frequency Select | RW | | 1 | | |
| Bit 1 | ATIG_FS1 | ATIG Frequency Select | RW | | 1 | | |
| Bit 0 | ATIG_FS0 | ATIG Frequency Select LSB | RW | | 1 | | |

SMBus Table: SB_SRC Frequency Select Register

| Byte | 6 | Name | Control Function | Type | 0 | 1 | Default |
|-------|---|-----------------|-----------------------------|------|---|--------|---------|
| Bit 7 | | ATIG SSEN | ATIG Spread Enable | RW | Disable | Enable | 0 |
| Bit 6 | | SB_SRC/CPU SSEN | SB_SRC/CPU Spread Enable | RW | Disable | Enable | 0 |
| Bit 5 | | SRC SSEN | SRC Spread Enable | RW | Disable | Enable | 0 |
| Bit 4 | | SB_SRC_FS4 | SB_SRC Frequency Select MSB | RW | See SB_SRC Frequency Select Table Note: SB_SRC and CPU Clocks are synchronous. Changing this frequency will alter the SB_SRC and CPU frequency by the same percentage. | | 0 |
| Bit 3 | | SB_SRC_FS3 | SB_SRC Frequency Select | RW | | | 1 |
| Bit 2 | | SB_SRC_FS2 | SB_SRC Frequency Select | RW | | | 1 |
| Bit 1 | | SB_SRC_FS1 | SB_SRC Frequency Select | RW | | | 1 |
| Bit 0 | | SB_SRC_FS0 | SB_SRC Frequency Select LSB | RW | | | 1 |

SMBus Table: Device ID register

| Byte | 7 | Name | Control Function | Type | 0 | 1 | Default |
|-------|---|------------|------------------|------|---------------------|---|---------|
| Bit 7 | | Device ID7 | Device ID | R | 75 hex for 9LPRS477 | | x |
| Bit 6 | | Device ID6 | | R | | | x |
| Bit 5 | | Device ID5 | | R | | | x |
| Bit 4 | | Device ID4 | | R | | | x |
| Bit 3 | | Device ID3 | | R | | | x |
| Bit 2 | | Device ID2 | | R | | | x |
| Bit 1 | | Device ID1 | | R | | | x |
| Bit 0 | | Device ID0 | | R | | | x |

SMBus Table: Vendor & Revision ID Register

| Byte | 8 | Name | Control Function | Type | 0 | 1 | Default |
|-------|---|------|------------------|------|---|---|---------|
| Bit 7 | | RID3 | REVISION ID | R | - | - | 0 |
| Bit 6 | | RID2 | | R | - | - | 1 |
| Bit 5 | | RID1 | | R | - | - | 0 |
| Bit 4 | | RID0 | | R | - | - | 0 |
| Bit 3 | | VID3 | VENDOR ID | R | - | - | 0 |
| Bit 2 | | VID2 | | R | - | - | 0 |
| Bit 1 | | VID1 | | R | - | - | 0 |
| Bit 0 | | VID0 | | R | - | - | 1 |

SMBus Table: WatchDog Timer Control Register

| Byte | 9 | Name | Control Function | Type | 0 | 1 | Default |
|-------|---|----------------|-----------------------------------|------|---|--------------|---------|
| Bit 7 | | HWD_EN | Watchdog Hard Alarm Enable | RW | Disable and Reload Hard Alarm Timer, Clear WD Hard status bit. | Enable Timer | 0 |
| Bit 6 | | SWD_EN | Watchdog Soft Alarm Enable | RW | Disable | Enable | 0 |
| Bit 5 | | WD Hard Status | WD Hard Alarm Status | R | Normal | Alarm | X |
| Bit 4 | | WD Soft Status | WD Soft Alarm Status | R | Normal | Alarm | X |
| Bit 3 | | WDT Ctrl | Watch Dog Alarm Time base Control | RW | 290ms Base | 1160ms Base | 0 |
| Bit 2 | | HWD2 | WD Hard Alarm Timer Bit 2 | RW | These bits represent the number of Watch Dog Time Base Units that pass before the Watch Alarm expires. Default is 7 X 290ms = 2s. | | 1 |
| Bit 1 | | HWD1 | WD Hard Alarm Timer Bit 1 | RW | | | 1 |
| Bit 0 | | HWD0 | WD Hard Alarm Timer Bit 0 | RW | | | 1 |

SMBus Table: WD Timer Safe Frequency Control Register

| Byte | 10 | Name | Control Function | Type | 0 | 1 | Default |
|-------|----|--------|--------------------------------------|------|---|---|---------|
| Bit 7 | | SWD2 | WD Soft Alarm Timer Bit 2 | RW | These bits represent the number of Watch Dog Time Base Units that pass before the Watch Alarm expires. Default is 7 X 290ms = 2s. | | 1 |
| Bit 6 | | SWD1 | WD Soft Alarm Timer Bit 1 | RW | | | 1 |
| Bit 5 | | SWD0 | WD Soft Alarm Timer Bit 0 | RW | | | 1 |
| Bit 4 | | WD SF4 | Watch Dog Safe Freq Programming bits | RW | These bits configure the safe frequency that the device returns to if the Watchdog Timer expires. The value show here corresponds to the power up default of the device. See the various Frequency Select Tables for the exact frequencies. | | 0 |
| Bit 3 | | WD SF3 | | RW | | | 1 |
| Bit 2 | | WD SF2 | | RW | | | 1 |
| Bit 1 | | WD SF1 | | RW | | | 1 |
| Bit 0 | | WD SF0 | | RW | | | 1 |

SMBus Table: Byte Count Register

| Byte | 11 | Name | Control Function | Type | 0 | 1 | Default |
|-------|----|------|------------------------|------|---|---|---------|
| Bit 7 | | | | | Reserved | | 0 |
| Bit 6 | | | | | Reserved | | 0 |
| Bit 5 | | BC5 | Byte Count bit 5 (MSB) | RW | Determines the number of bytes that are read back from the device. Default is 0F hex. | | 0 |
| Bit 4 | | BC4 | Byte Count bit 4 | RW | | | 0 |
| Bit 3 | | BC3 | Byte Count bit 3 | RW | | | 1 |
| Bit 2 | | BC2 | Byte Count bit 2 | RW | | | 1 |
| Bit 1 | | BC1 | Byte Count bit 1 | RW | | | 1 |
| Bit 0 | | BC0 | Byte Count bit 0 (LSB) | RW | | | 1 |

SMBus Table: M/N Programming Enable and I/O Vout Control Register

| Byte | 12 | Name | Control Function | Type | 0 | 1 | Default |
|-------|----|----------------------|--|------|--|-------------------|---------|
| Bit 7 | | CPU M/N En | CPU PLL M/N Prog. Enable | RW | M/N Prog. Disabled | M/N Prog. Enabled | 0 |
| Bit 6 | | SRC M/N En | SRC M/N Prog.Enable | RW | M/N Prog. Disabled | M/N Prog. Enabled | 0 |
| Bit 5 | | ATIG M/N En | ATIG M/N Prog. Enable | RW | M/N Prog. Disabled | M/N Prog. Enabled | 0 |
| Bit 4 | | SB_SRC M/N En | SB_SRC M/N Prog. Enable | RW | M/N Prog. Disabled | M/N Prog. Enabled | 0 |
| Bit 3 | | SEL_OC_MODE readback | OC MODE Select | R | PCIe Gen2 Mode | PCIe Gen1 Mode | Latch |
| Bit 2 | | IO_VOUT2 | IO Output Voltage Select (Most Significant Bit) | RW | See Table 5: V_IO Selection (Default is 0.8V) | | 1 |
| Bit 1 | | IO_VOUT1 | IO Output Voltage Select | RW | | | 0 |
| Bit 0 | | IO_VOUT0 | IO Output Voltage Select (Least Significant Bit) | RW | | | 1 |

Bytes 13/14 are reserved

SMBus Table:Test Mode Register

| Byte | 15 | Name | Control Function | Type | 0 | 1 | Default |
|-------|----|---------------|-----------------------------|------|-------------|-----------------------|---------|
| Bit 7 | | Test_Sel | Selects Test Mode | RW | Normal mode | All outputs are REF/N | 0 |
| Bit 6 | | SB_SRC Source | SB_SRC Source Selection | RW | SB_SRC PLL | SRC PLL | 1 |
| Bit 5 | | ATIG PLL | ATIG PLL DOC pin control | RW | DOC0 | DOC1 | 0 |
| Bit 4 | | CPU PLL | CPU PLL DOC pin control | RW | DOC0 | DOC1 | 0 |
| Bit 3 | | SRC PLL | SRC PLL DOC pin control | RW | DOC0 | DOC1 | 0 |
| Bit 2 | | ATIG PLL | ATIG PLL DOC0 2 pin control | RW | Disable | Enable | 0 |
| Bit 1 | | CPU PLL | CPU PLL DOC0 2 pin control | RW | Disable | Enable | 0 |
| Bit 0 | | SRC PLL | SRC PLL DOC0 2 pin control | RW | Disable | Enable | 0 |

SMBus Table: CPU PLL Frequency Control Register

| Byte | 16 | Name | Control Function | Type | 0 | 1 | Default |
|-------|----|--------|----------------------------|------|--|---|---------|
| Bit 7 | | N Div2 | N Divider Prog bit 2 | RW | The decimal representation of M and N Divider in Byte 16 and 17 will configure the VCO frequency. Default at power up = Byte 3 Rom table. See M/N Calculation Tables for VCO frequency formulas. | | X |
| Bit 6 | | N Div1 | N Divider Prog bit 1 | RW | | | X |
| Bit 5 | | M Div5 | M Divider Programming bits | RW | | | X |
| Bit 4 | | M Div4 | | RW | | | X |
| Bit 3 | | M Div3 | | RW | | | X |
| Bit 2 | | M Div2 | | RW | | | X |
| Bit 1 | | M Div1 | | RW | | | X |
| Bit 0 | | M Div0 | | RW | | | X |

SMBus Table: CPU PLL Frequency Control Register

| Byte | 17 | Name | Control Function | Type | 0 | 1 | Default |
|-------|----|---------|-------------------------------|------|--|---|---------|
| Bit 7 | | N Div10 | N Divider Programming b(10:3) | RW | The decimal representation of M and N Divider in Byte 16 and 17 will configure the VCO frequency. Default at power up = Byte 3 Rom table. See M/N Calculation Tables for VCO frequency formulas. | | X |
| Bit 6 | | N Div9 | | RW | | | X |
| Bit 5 | | N Div8 | | RW | | | X |
| Bit 4 | | N Div7 | | RW | | | X |
| Bit 3 | | N Div6 | | RW | | | X |
| Bit 2 | | N Div5 | | RW | | | X |
| Bit 1 | | N Div4 | | RW | | | X |
| Bit 0 | | N Div3 | | RW | | | X |

SMBus Table: SB_SRC PLL Spread Spectrum Control Register

| Byte | 18 | Name | Control Function | Type | 0 | 1 | Default |
|-------|----|------|------------------------------------|------|---|---|---------|
| Bit 7 | | SSP7 | Spread Spectrum Programming b(7:0) | RW | These bits set the SB_SRC spread percentage. Please contact IDT for the appropriate values. | | X |
| Bit 6 | | SSP6 | | RW | | | X |
| Bit 5 | | SSP5 | | RW | | | X |
| Bit 4 | | SSP4 | | RW | | | X |
| Bit 3 | | SSP3 | | RW | | | X |
| Bit 2 | | SSP2 | | RW | | | X |
| Bit 1 | | SSP1 | | RW | | | X |
| Bit 0 | | SSP0 | | RW | | | X |

SMBus Table: SB_SRC PLL Spread Spectrum Control Register

| Byte | 19 | Name | Control Function | Type | 0 | 1 | Default |
|-------|----|-------|-------------------------------------|------|---|---|---------|
| Bit 7 | | SSP15 | Spread Spectrum Programming b(15:8) | RW | These bits set the SB_SRC spread percentage. Please contact IDT for the appropriate values. | | X |
| Bit 6 | | SSP14 | | RW | | | X |
| Bit 5 | | SSP13 | | RW | | | X |
| Bit 4 | | SSP12 | | RW | | | X |
| Bit 3 | | SSP11 | | RW | | | X |
| Bit 2 | | SSP10 | | RW | | | X |
| Bit 1 | | SSP9 | | RW | | | X |
| Bit 0 | | SSP8 | | RW | | | X |

SMBUS Table: CPU Output Divider Register

| Byte | 20 | Name | Control Function | Type | 0 | 1 | Default |
|-------|----|-----------|------------------------------------|----------|--|---------------------|---------|
| Bit 7 | | CPU NDiv0 | LSB N Divider Programming | RW | Byte 28 has the N Divider LSB (bit 0) for CPU M/N programming. | | X |
| Bit 6 | | | | Reserved | | | X |
| Bit 5 | | | | Reserved | | | X |
| Bit 4 | | | | Reserved | | | X |
| Bit 3 | | CPUDiv3 | CPU Divider Ratio Programming Bits | RW | 0000:/2 ; 0100:/4 | 1000:/8 ; 1100:/16 | X |
| Bit 2 | | CPUDiv2 | | RW | 0001:/3 ; 0101:/6 | 1001:/12 ; 1101:/24 | X |
| Bit 1 | | CPUDiv1 | | RW | 0010:/5 ; 0110:/10 | 1010:/20 ; 1110:/40 | X |
| Bit 0 | | CPUDiv0 | | RW | 0011:/9 ; 0111:/18 | 1011:/36 ; 1111:/72 | X |

SMBUS Table: SRC Frequency Control Register

| Byte | 21 | Name | Control Function | Type | 0 | 1 | Default |
|-------|----|--------|---------------------------------|------|---|---|---------|
| Bit 7 | | N Div2 | N Divider Prog bit 2 | RW | The decimal representation of M and N Divider in Byte 21 and 22 configure the SRC VCO frequency. See M/N Calculation Tables for VCO frequency formulas. | | X |
| Bit 6 | | N Div1 | N Divider Prog bit 1 | RW | | | X |
| Bit 5 | | M Div5 | M Divider Programming bit (5:0) | RW | | | X |
| Bit 4 | | M Div4 | | RW | | | X |
| Bit 3 | | M Div3 | | RW | | | X |
| Bit 2 | | M Div2 | | RW | | | X |
| Bit 1 | | M Div1 | | RW | | | X |
| Bit 0 | | M Div0 | | RW | | | X |

SMBUS Table: SRC Frequency Control Register

| Byte | 22 | Name | Control Function | Type | 0 | 1 | Default |
|-------|----|---------|---|------|---|---|---------|
| Bit 7 | | N Div10 | N Divider Programming Byte16 bit(7:0) and Byte15 bit(7:6) | RW | The decimal representation of M and N Divider in Byte 21 and 22 configure the SRC VCO frequency. See M/N Calculation Tables for VCO frequency formulas. | | X |
| Bit 6 | | N Div9 | | RW | | | X |
| Bit 5 | | N Div8 | | RW | | | X |
| Bit 4 | | N Div7 | | RW | | | X |
| Bit 3 | | N Div6 | | RW | | | X |
| Bit 2 | | N Div5 | | RW | | | X |
| Bit 1 | | N Div4 | | RW | | | X |
| Bit 0 | | N Div3 | | RW | | | X |

SMBUS Table: SRC Spread Spectrum Control Register

| Byte | 23 | Name | Control Function | Type | 0 | 1 | Default |
|-------|----|------|--------------------------------------|------|---|---|---------|
| Bit 7 | | SSP7 | Spread Spectrum Programming bit(7:0) | RW | These bits set the SRC spread percentages. Please contact IDT for the appropriate values. | | X |
| Bit 6 | | SSP6 | | RW | | | X |
| Bit 5 | | SSP5 | | RW | | | X |
| Bit 4 | | SSP4 | | RW | | | X |
| Bit 3 | | SSP3 | | RW | | | X |
| Bit 2 | | SSP2 | | RW | | | X |
| Bit 1 | | SSP1 | | RW | | | X |
| Bit 0 | | SSP0 | | RW | | | X |

SMBUS Table: SRC Spread Spectrum Control Register

| Byte | 24 | Name | Control Function | Type | 0 | 1 | Default |
|-------|----|-------|---------------------------------------|------|---|---|---------|
| Bit 7 | | SSP15 | Spread Spectrum Programming bit(15:8) | RW | These bits set the SRC spread percentages. Please contact IDT for the appropriate values. | | X |
| Bit 6 | | SSP14 | | RW | | | X |
| Bit 5 | | SSP13 | | RW | | | X |
| Bit 4 | | SSP12 | | RW | | | X |
| Bit 3 | | SSP11 | | RW | | | X |
| Bit 2 | | SSP10 | | RW | | | X |
| Bit 1 | | SSP9 | | RW | | | X |
| Bit 0 | | SSP8 | | RW | | | X |

SMBUS Table: SRC Output Divider Control Register

| Byte | 25 | Name | Control Function | Type | 0 | 1 | Default |
|-------|----|--------------|------------------------------------|----------|--|---------------------|---------|
| Bit 7 | | SB_SRC NDiv0 | LSB N Divider Programming | RW | N Divider LSB (bit 0) for SRC M/N programming. | | X |
| Bit 6 | | | | Reserved | | | X |
| Bit 5 | | | | Reserved | | | X |
| Bit 4 | | | | Reserved | | | X |
| Bit 3 | | SRCDiv3 | SRC Divider Ratio Programming Bits | RW | 0000:/2 ; 0100:/4 | 1000:/8 ; 1100:/16 | X |
| Bit 2 | | SRCDiv2 | | RW | 0001:/3 ; 0101:/6 | 1001:/12 ; 1101:/24 | X |
| Bit 1 | | SRCDiv1 | | RW | 0010:/5 ; 0110:/10 | 1010:/20 ; 1110:/40 | X |
| Bit 0 | | SRCDiv0 | | RW | 0011:/9 ; 0111:/18 | 1011:/36 ; 1111:/72 | X |

SMBUS Table: ATIG Frequency Control Register

| Byte | 26 | Name | Control Function | Type | 0 | 1 | Default |
|-------|----|--------|---------------------------------|------|---|---|---------|
| Bit 7 | | N Div2 | N Divider Prog bit 2 | RW | The decimal representation of M and N Divider in Byte 26 and 27 will configure the VCO frequency. Default at power up = Byte 5 Rom table. See M/N Caculation Tables for VCO frequency formulas. | | X |
| Bit 6 | | N Div1 | N Divider Prog bit 1 | RW | | | X |
| Bit 5 | | M Div5 | M Divider Programming bit (5:0) | RW | | | X |
| Bit 4 | | M Div4 | | RW | | | X |
| Bit 3 | | M Div3 | | RW | | | X |
| Bit 2 | | M Div2 | | RW | | | X |
| Bit 1 | | M Div1 | | RW | | | X |
| Bit 0 | | M Div0 | | RW | | | X |

SMBUS Table: ATIG Frequency Control Register

| Byte | 27 | Name | Control Function | Type | 0 | 1 | Default |
|-------|----|---------|---|------|---|---|---------|
| Bit 7 | | N Div10 | N Divider Programming Byte20 bit(7:0) and Byte19 bit(7:6) | RW | The decimal representation of M and N Divider in Byte 26 and 27 will configure the VCO frequency. Default at power up = Byte 5 Rom table. See M/N Caculation Tables for VCO frequency formulas. | | X |
| Bit 6 | | N Div9 | | RW | | | X |
| Bit 5 | | N Div8 | | RW | | | X |
| Bit 4 | | N Div7 | | RW | | | X |
| Bit 3 | | N Div6 | | RW | | | X |
| Bit 2 | | N Div5 | | RW | | | X |
| Bit 1 | | N Div4 | | RW | | | X |
| Bit 0 | | N Div3 | | RW | | | X |

SMBUS Table: ATIG Output Divider Control Register

| Byte | 28 | Name | Control Function | Type | 0 | 1 | Default |
|-------|----|------------|-------------------------------------|----------|---|---------------------|---------|
| Bit 7 | | ATIG NDiv0 | LSB N Divider Programming | RW | N Divider LSB (bit 0) for ATIG M/N programming. | | X |
| Bit 6 | | | | Reserved | | | X |
| Bit 5 | | | | Reserved | | | X |
| Bit 4 | | | | Reserved | | | X |
| Bit 3 | | ATIGDiv3 | ATIG Divider Ratio Programming Bits | RW | 0000:/2 ; 0100:/4 | 1000:/8 ; 1100:/16 | X |
| Bit 2 | | ATIGDiv2 | | RW | 0001:/3 ; 0101:/6 | 1001:/12 ; 1101:/24 | X |
| Bit 1 | | ATIGDiv1 | | RW | 0010:/5 ; 0110:/10 | 1010:/20 ; 1110:/40 | X |
| Bit 0 | | ATIGDiv0 | | RW | 0011:/9 ; 0111:/18 | 1011:/36 ; 1111:/72 | X |

SMBUS Table: SB_SRC Frequency Control Register

| Byte | 29 | Name | Control Function | Type | 0 | 1 | Default |
|-------|----|--------|---------------------------------|------|---|---|---------|
| Bit 7 | | N Div2 | N Divider Prog bit 2 | RW | The decimal representation of M and N Divider in Byte 29 and 30 will configure the VCO frequency. Default at power up = Byte 6 Rom table. See M/N Caculation Tables for VCO frequency formulas. | | X |
| Bit 6 | | N Div1 | N Divider Prog bit 1 | RW | | | X |
| Bit 5 | | M Div5 | M Divider Programming bit (5:0) | RW | | | X |
| Bit 4 | | M Div4 | | RW | | | X |
| Bit 3 | | M Div3 | | RW | | | X |
| Bit 2 | | M Div2 | | RW | | | X |
| Bit 1 | | M Div1 | | RW | | | X |
| Bit 0 | | M Div0 | | RW | | | X |

SMBUS Table: SB_SRC Frequency Control Register

| Byte | 30 | Name | Control Function | Type | 0 | 1 | Default |
|-------|----|---------|---|------|---|---|---------|
| Bit 7 | | N Div10 | N Divider Programming Byte20 bit(7:0) and Byte19 bit(7:6) | RW | The decimal representation of M and N Divider in Byte 29 and 30 will configure the VCO frequency. Default at power up = Byte 6 Rom table. See M/N Caculation Tables for VCO frequency formulas. | | X |
| Bit 6 | | N Div9 | | RW | | | X |
| Bit 5 | | N Div8 | | RW | | | X |
| Bit 4 | | N Div7 | | RW | | | X |
| Bit 3 | | N Div6 | | RW | | | X |
| Bit 2 | | N Div5 | | RW | | | X |
| Bit 1 | | N Div4 | | RW | | | X |
| Bit 0 | | N Div3 | | RW | | | X |

SMBUS Table: SB_SRC Output Divider Control Register

| Byte | 31 | Name | Control Function | Type | 0 | 1 | Default |
|-------|----|--------------|---------------------------------------|----------|--|---------------------|---------|
| Bit 7 | | SB_SRC NDiv0 | LSB N Divider Programming | RW | N Divider LSB (bit 0) for SRC M/N programming. | | X |
| Bit 6 | | | | Reserved | | | X |
| Bit 5 | | | | Reserved | | | X |
| Bit 4 | | | | Reserved | | | X |
| Bit 3 | | SB_SRCDiv3 | SB_SRC Divider Ratio Programming Bits | RW | 0000:/2 ; 0100:/4 | 1000:/8 ; 1100:/16 | X |
| Bit 2 | | SB_SRCDiv2 | | RW | 0001:/3 ; 0101:/6 | 1001:/12 ; 1101:/24 | X |
| Bit 1 | | SB_SRCDiv1 | | RW | 0010:/5 ; 0110:/10 | 1010:/20 ; 1110:/40 | X |
| Bit 0 | | SB_SRCDiv0 | | RW | 0011:/9 ; 0111:/18 | 1011:/36 ; 1111:/72 | X |

SMBUS Table: CPU PLL DOC 1 N programming Register (1 pin control : DOC = 1; 2 pin control : DOC [0:1] = 01)

| Byte | 32 | Name | Control Function | Type | 0 | 1 | Default |
|-------|----|---------|--|------|--|---|---------|
| Bit 7 | | N Div10 | N Divider Programming Byte20 bit(7:0) and Byte19 bit(7:6) | RW | The decimal representation of M and N Divider in Byte 16 and 32 will configure the VCO frequency. Default at power up = Byte 3 Rom table. See M/N Calculation Tables for VCO frequency formulas. | | X |
| Bit 6 | | N Div9 | | RW | | | X |
| Bit 5 | | N Div8 | | RW | | | X |
| Bit 4 | | N Div7 | | RW | | | X |
| Bit 3 | | N Div6 | | RW | | | X |
| Bit 2 | | N Div5 | | RW | | | X |
| Bit 1 | | N Div4 | | RW | | | X |
| Bit 0 | | N Div3 | | RW | | | X |

SMBUS Table: CPU PLL DOC 2 N programming Register (1 pin control : DOC = 1; 2 pin control : DOC [0:1] = 10)

| Byte | 33 | Name | Control Function | Type | 0 | 1 | Default |
|-------|----|---------|--|------|--|---|---------|
| Bit 7 | | N Div10 | N Divider Programming Byte20 bit(7:0) and Byte19 bit(7:6) | RW | The decimal representation of M and N Divider in Byte 16 and 33 will configure the VCO frequency. Default at power up = Byte 3 Rom table. See M/N Calculation Tables for VCO frequency formulas. | | X |
| Bit 6 | | N Div9 | | RW | | | X |
| Bit 5 | | N Div8 | | RW | | | X |
| Bit 4 | | N Div7 | | RW | | | X |
| Bit 3 | | N Div6 | | RW | | | X |
| Bit 2 | | N Div5 | | RW | | | X |
| Bit 1 | | N Div4 | | RW | | | X |
| Bit 0 | | N Div3 | | RW | | | X |

SMBUS Table: CPU PLL DOC 3 N programming Register (1 pin control : DOC = 1; 2 pin control : DOC [0:1] = 11)

| Byte | 34 | Name | Control Function | Type | 0 | 1 | Default |
|-------|----|---------|--|------|--|---|---------|
| Bit 7 | | N Div10 | N Divider Programming Byte20 bit(7:0) and Byte19 bit(7:6) | RW | The decimal representation of M and N Divider in Byte 16 and 34 will configure the VCO frequency. Default at power up = Byte 3 Rom table. See M/N Calculation Tables for VCO frequency formulas. | | X |
| Bit 6 | | N Div9 | | RW | | | X |
| Bit 5 | | N Div8 | | RW | | | X |
| Bit 4 | | N Div7 | | RW | | | X |
| Bit 3 | | N Div6 | | RW | | | X |
| Bit 2 | | N Div5 | | RW | | | X |
| Bit 1 | | N Div4 | | RW | | | X |
| Bit 0 | | N Div3 | | RW | | | X |

SMBUS Table: ATIG PLL DOC 1 N programming Register (1 pin control : DOC = 1; 2 pin control : DOC [0:1] = 01)

| Byte | 35 | Name | Control Function | Type | 0 | 1 | Default |
|-------|----|---------|--|------|--|---|---------|
| Bit 7 | | N Div10 | N Divider Programming Byte20 bit(7:0) and Byte19 bit(7:6) | RW | The decimal representation of M and N Divider in Byte 26 and 35 will configure the VCO frequency. Default at power up = Byte 5 Rom table. See M/N Calculation Tables for VCO frequency formulas. | | X |
| Bit 6 | | N Div9 | | RW | | | X |
| Bit 5 | | N Div8 | | RW | | | X |
| Bit 4 | | N Div7 | | RW | | | X |
| Bit 3 | | N Div6 | | RW | | | X |
| Bit 2 | | N Div5 | | RW | | | X |
| Bit 1 | | N Div4 | | RW | | | X |
| Bit 0 | | N Div3 | | RW | | | X |

SMBUS Table: ATIG PLL DOC 2 N programming Register (1 pin control : DOC = 1; 2 pin control : DOC [0:1] = 10)

| Byte | 36 | Name | Control Function | Type | 0 | 1 | Default |
|-------|----|---------|--|------|--|---|---------|
| Bit 7 | | N Div10 | N Divider Programming Byte20 bit(7:0) and Byte19 bit(7:6) | RW | The decimal representation of M and N Divider in Byte 26 and 36 will configure the VCO frequency. Default at power up = Byte 5 Rom table. See M/N Calculation Tables for VCO frequency formulas. | | X |
| Bit 6 | | N Div9 | | RW | | | X |
| Bit 5 | | N Div8 | | RW | | | X |
| Bit 4 | | N Div7 | | RW | | | X |
| Bit 3 | | N Div6 | | RW | | | X |
| Bit 2 | | N Div5 | | RW | | | X |
| Bit 1 | | N Div4 | | RW | | | X |
| Bit 0 | | N Div3 | | RW | | | X |

SMBUS Table: ATIG PLL DOC 3 N programming Register (1 pin control : DOC = 1; 2 pin control : DOC [0:1] = 11)

| Byte | 37 | Name | Control Function | Type | 0 | 1 | Default |
|-------|----|---------|--|------|--|---|---------|
| Bit 7 | | N Div10 | N Divider Programming Byte20 bit(7:0) and Byte19 bit(7:6) | RW | The decimal representation of M and N Divider in Byte 26 and 37 will configure the VCO frequency. Default at power up = Byte 5 Rom table. See M/N Calculation Tables for VCO frequency formulas. | | X |
| Bit 6 | | N Div9 | | RW | | | X |
| Bit 5 | | N Div8 | | RW | | | X |
| Bit 4 | | N Div7 | | RW | | | X |
| Bit 3 | | N Div6 | | RW | | | X |
| Bit 2 | | N Div5 | | RW | | | X |
| Bit 1 | | N Div4 | | RW | | | X |
| Bit 0 | | N Div3 | | RW | | | X |

SMBUS Table: SRC PLL DOC 1 N programming Register (1 pin control : DOC = 1; 2 pin control : DOC [0:1] = 01)

| Byte | 38 | Name | Control Function | Type | 0 | 1 | Default |
|-------|----|---------|--|------|---|---|---------|
| Bit 7 | | N Div10 | N Divider Programming Byte20 bit(7:0) and Byte19 bit(7:6) | RW | The decimal representation of M and N Divider in Byte 21 and 38 will configure the VCO frequency. Default at power up = Byte 4 Rom table. See M/N Caculation Tables for VCO frequency formulas. | | X |
| Bit 6 | | N Div9 | | RW | | | X |
| Bit 5 | | N Div8 | | RW | | | X |
| Bit 4 | | N Div7 | | RW | | | X |
| Bit 3 | | N Div6 | | RW | | | X |
| Bit 2 | | N Div5 | | RW | | | X |
| Bit 1 | | N Div4 | | RW | | | X |
| Bit 0 | | N Div3 | | RW | | | X |

SMBUS Table: SRC PLL DOC 2 N programming Register (1 pin control : DOC = 1; 2 pin control : DOC [0:1] = 10)

| Byte | 39 | Name | Control Function | Type | 0 | 1 | Default |
|-------|----|---------|--|------|---|---|---------|
| Bit 7 | | N Div10 | N Divider Programming Byte20 bit(7:0) and Byte19 bit(7:6) | RW | The decimal representation of M and N Divider in Byte 21 and 39 will configure the VCO frequency. Default at power up = Byte 4 Rom table. See M/N Caculation Tables for VCO frequency formulas. | | X |
| Bit 6 | | N Div9 | | RW | | | X |
| Bit 5 | | N Div8 | | RW | | | X |
| Bit 4 | | N Div7 | | RW | | | X |
| Bit 3 | | N Div6 | | RW | | | X |
| Bit 2 | | N Div5 | | RW | | | X |
| Bit 1 | | N Div4 | | RW | | | X |
| Bit 0 | | N Div3 | | RW | | | X |

SMBUS Table: SRC PLL DOC 3 N programming Register (1 pin control : DOC = 1; 2 pin control : DOC [0:1] = 11)

| Byte | 40 | Name | Control Function | Type | 0 | 1 | Default |
|-------|----|---------|--|------|---|---|---------|
| Bit 7 | | N Div10 | N Divider Programming Byte20 bit(7:0) and Byte19 bit(7:6) | RW | The decimal representation of M and N Divider in Byte 21 and 37 will configure the VCO frequency. Default at power up = Byte 4 Rom table. See M/N Caculation Tables for VCO frequency formulas. | | X |
| Bit 6 | | N Div9 | | RW | | | X |
| Bit 5 | | N Div8 | | RW | | | X |
| Bit 4 | | N Div7 | | RW | | | X |
| Bit 3 | | N Div6 | | RW | | | X |
| Bit 2 | | N Div5 | | RW | | | X |
| Bit 1 | | N Div4 | | RW | | | X |
| Bit 0 | | N Div3 | | RW | | | X |

SMBus Table: ATIG PLL Spread Spectrum Control Register

| Byte | 41 | Name | Control Function | Type | 0 | 1 | Default |
|-------|----|------|---------------------------------------|------|--|---|---------|
| Bit 7 | | SSP7 | Spread Spectrum Programming b(7:0) | RW | These bits set the ATIG spread percentage. Please contact IDT for the appropriate values. | | X |
| Bit 6 | | SSP6 | | RW | | | X |
| Bit 5 | | SSP5 | | RW | | | X |
| Bit 4 | | SSP4 | | RW | | | X |
| Bit 3 | | SSP3 | | RW | | | X |
| Bit 2 | | SSP2 | | RW | | | X |
| Bit 1 | | SSP1 | | RW | | | X |
| Bit 0 | | SSP0 | | RW | | | X |

SMBus Table: ATIG PLL Spread Spectrum Control Register

| Byte | 42 | Name | Control Function | Type | 0 | 1 | Default |
|-------|----|-------|--|------|--|---|---------|
| Bit 7 | | SSP15 | Spread Spectrum Programming b(15:8) | RW | These bits set the ATIG spread percentage. Please contact IDT for the appropriate values. | | X |
| Bit 6 | | SSP14 | | RW | | | X |
| Bit 5 | | SSP13 | | RW | | | X |
| Bit 4 | | SSP12 | | RW | | | X |
| Bit 3 | | SSP11 | | RW | | | X |
| Bit 2 | | SSP10 | | RW | | | X |
| Bit 1 | | SSP9 | | RW | | | X |
| Bit 0 | | SSP8 | | RW | | | X |

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9LPRS477D. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | Notes |
|--------------------------|----------------------|------------|------|-----|------------|-------|-------|
| 3.3V Core Supply Voltage | VDDxxx | - | | 3.3 | GND + 3.9V | V | 1 |
| Storage Temperature | T _s | - | -65 | | 150 | °C | 1 |
| Ambient Operating Temp | T _{ambient} | - | 0 | | 70 | °C | 1 |
| Case Temperature | T _{case} | - | | | 115 | °C | 1 |
| Input ESD protection HBM | ESD prot | - | 2000 | | | V | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics—Input/Supply/Common Output Parameters

| PARAMETER | SYMBOL | CONDITIONS* | MIN | TYP | MAX | UNITS | Notes |
|--|------------------------|--|-----------------------|----------|-----------------------|-------|-------|
| 3.3V Core Supply Voltage | VDDxxx | - | 3.135 | 3.3 | 3.465 | V | 1 |
| Input High Voltage | V _{IH} | VDD = 3.3 V +/-5% | 2 | | V _{DD} + 0.3 | V | 1 |
| Input Low Voltage | V _L | VDD = 3.3 V +/-5% | V _{SS} - 0.3 | | 0.8 | V | 1 |
| Input High Current | I _{IH} | V _{IN} = V _{DD} | -5 | | 5 | uA | 1 |
| Input Low Current | I _{IL1} | V _{IN} = 0 V; Inputs with no pull-up resistors | -5 | | | uA | 1 |
| | I _{IL2} | V _{IN} = 0 V; Inputs with pull-up resistors | -200 | | | uA | 1 |
| Low Threshold Input-High Voltage | V _{IH_FS} | VDD = 3.3 V +/-5% | 0.7 | | V _{DD} + 0.3 | V | 1 |
| Low Threshold Input-Low Voltage | V _{IL_FS} | VDD = 3.3 V +/-5% | V _{SS} - 0.3 | | 0.35 | V | 1 |
| Operating Current | I _{DD3.3CP} | all outputs driven | | | 225 | mA | 1 |
| Powerdown Current | I _{DD3.3PD} | all diff pairs low/low | | | 12 | mA | 1 |
| Input Frequency | F _i | VDD = 3.3 V +/-5% | | 14.31818 | | MHz | 2 |
| Pin Inductance | L _{pin} | | | | 7 | nH | 1 |
| Input Capacitance | C _{IN} | Logic Inputs | | | 5 | pF | 1 |
| | C _{OUT} | Output pin capacitance | | | 6 | pF | 1 |
| | C _{INX} | X1 & X2 pins | | | 5 | pF | 1 |
| Clk Stabilization | T _{STAB} | From VDD Power-Up or de-assertion of PD to 1st clock | | | 1.8 | ms | 1 |
| Modulation Frequency | | Triangular Modulation | 30 | | 33 | kHz | 1 |
| Tdrive_PD | | CPU output enable after PD de-assertion | | | 300 | us | 1 |
| Tfall_PD | | PD fall time of | | | 5 | ns | 1 |
| Trise_PD | | PD rise time of | | | 5 | ns | 1 |
| SMBus Voltage | V _{DDSMB} | | 2.7 | | 5.5 | V | 1 |
| Low-level Output Voltage | V _{OLSMB} | @ I _{PULLUP} | | | 0.4 | V | 1 |
| Current sinking at V _{OL} = 0.4 V | I _{PULLUPSMB} | | 4 | 6 | | mA | 1 |
| SMBCLK/SMBDAT Clock/Data Rise Time | T _{RSMB} | (Max V _{IL} - 0.15) to (Min V _{IH} + 0.15) | | | 1000 | ns | 1 |
| SMBCLK/SMBDAT Clock/Data Fall Time | T _{FSMB} | (Min V _{IH} + 0.15) to (Max V _{IL} - 0.15) | | | 300 | ns | 1 |

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%

¹Guaranteed by design and characterization, not 100% tested in production.

²Input frequency should be measured at the REF pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.

AC Electrical Characteristics—Low-Power DIF Outputs: CPUKG and HTT

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|--------------------|-----------------------------------|-------|-----|------|-------|-------|
| Crossing Point Variation | ΔV_{CROSS} | Single-ended Measurement | | | 140 | mV | 1,2,5 |
| Frequency | f | Spread Specturm On | 198.8 | | 200 | MHz | 1,3 |
| Long Term Accuracy | ppm | Spread Specturm Off | -300 | | +300 | ppm | 1,1 1 |
| Rising Edge Slew Rate | S_{RISE} | Differential Measurement | 0.5 | | 10 | V/ns | 1,4 |
| Falling Edge Slew Rate | S_{FALL} | Differential Measurement | 0.5 | | 10 | V/ns | 1,4 |
| Slew Rate Variation | t_{SLVAR} | Single-ended Measurement | | | 20 | % | 1 |
| CPU, DIF HTT Jitter - Cycle to Cycle | $CPUJ_{C2C}$ | Differential Measurement | | | 150 | ps | 1,6 |
| Accumulated Jitter | t_{JACC} | See Notes | | | 1 | ns | 1,7 |
| Peak to Peak Differential Voltage | $V_{D(PK-PK)}$ | Differential Measurement | 400 | | 2400 | mV | 1,8 |
| Differential Voltage | V_D | Differential Measurement | 200 | | 1200 | mV | 1,9 |
| Duty Cycle | D_{CYC} | Differential Measurement | 45 | | 55 | % | 1 |
| Amplitude Variation | ΔV_D | Change in V_D DC cycle to cycle | -75 | | 75 | mV | 1,1 0 |
| CPU[1:0] Skew | CPU_{SKEW10} | Differential Measurement | | | 100 | ps | 1 |

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 2pF with Rs = 0Ω (unless otherwise specified)

¹Guaranteed by design and characterization, not 100% tested in production.

²Single-ended measurement at crossing point. Value is maximum – minimum over all time. DC value of common mode is not important due to the blocking cap.

³Minimum Frequency is a result of 0.5% down spread spectrum

⁴Differential measurement through the range of ±100 mV, differential signal must remain monotonic and within slew rate spec when crossing through this region.

⁵Defined as the total variation of all crossing voltages of CLK rising and CLK# falling. Matching applies to rising edge rate of CLK and falling edge of CLK#. It is measured using a +/-75mV window centered on the average cross point where CLK meets CLK#.

⁶Max difference of t_{CYCLE} between any two adjacent cycles.

⁷Accumulated t_{jc} over a 10μs time period, measured with JI2 TIE at 50ps interval.

⁸ $V_{D(PK-PK)}$ is the overall magnitude of the differential signal.

⁹ $V_D(\min)$ is the amplitude of the ring-back differential measurement, guaranteed by design, that ring-back will not cross 0V V_D . $V_D(\max)$ is the largest amplitude allowed.

¹⁰The difference in magnitude of two adjacent V_{D_DC} measurements. V_{D_DC} is the stable post overshoot and ring-back part of the signal.

¹¹All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

AC Electrical Characteristics—Low-Power DIF Outputs: SRC, SB_SRC, ATIG

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|-----------------|--------------------------|------|-----|------|-------|-------|
| Rising Edge Slew Rate | t_{SLR} | Differential Measurement | 0.6 | | 4 | V/ns | 1,2 |
| Falling Edge Slew Rate | t_{FLR} | Differential Measurement | 0.6 | | 4 | V/ns | 1,2 |
| Slew Rate Variation | t_{SLVAR} | Single-ended Measurement | | | 20 | % | 1 |
| Maximum Output Voltage | V_{HIGH} | Includes overshoot | | | 1150 | mV | 1 |
| Minimum Output Voltage | V_{LOW} | Includes undershoot | -300 | | | mV | 1 |
| Differential Voltage Swing | V_{SWING} | Differential Measurement | 300 | | | mV | 1 |
| Crossing Point Voltage | V_{XABS} | Single-ended Measurement | 300 | | 550 | mV | 1,3,4 |
| Crossing Point Variation | $V_{XABSVAR}$ | Single-ended Measurement | | | 140 | mV | 1,3,5 |
| Duty Cycle | D_{CYC} | Differential Measurement | 45 | | 55 | % | 1 |
| SRC, SB_SRC, ATIG, Jitter - Cycle to Cycle | $SRC_{J_{C2C}}$ | Differential Measurement | | | 125 | ps | 1 |
| SRC[5:0] Skew | SRC_{SKEW} | Differential Measurement | | | 250 | ps | 1 |
| SB_SRC[1:0] Skew | SRC_{SKEW} | Differential Measurement | | | 100 | ps | 1 |
| ATIG[3:0] Skew | SRC_{SKEW} | Differential Measurement | | | 100 | ps | 1 |

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 2pF with Rs = 0Ω (unless otherwise specified)

¹Guaranteed by design and characterization, not 100% tested in production.

²Slew rate measured through Vswing centered around differential zero

³Vxabs is defined as the voltage where CLK = CLK#

⁴Only applies to the differential rising edge (CLK rising and CLK# falling)

⁵Defined as the total variation of all crossing voltages of CLK rising and CLK# falling. Matching applies to rising edge rate of CLK and falling edge of CLK#. It is measured using a +/-75mV window centered on the average cross point where CLK meets CLK#.

⁶All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

Electrical Characteristics—Single-Ended HTT 66MHz Clock

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | Notes |
|------------------------|---------------------|------------------------------------|---------|-----|---------|-------|-------|
| Long Accuracy | ppm | see Tperiod min-max values | -300 | | 300 | ppm | 1,2 |
| PCI33 Clock period | T_{period} | 33.33MHz output nominal | 29.9910 | | 30.0090 | ns | 2 |
| | | 33.33MHz output spread | 29.9910 | | 30.1598 | ns | 2 |
| HTT66 Clock period | T_{period} | 66.67MHz output nominal | 14.9955 | | 15.0045 | ns | 2 |
| | | 66.67MHz output spread | 14.9955 | | 15.0799 | ns | 2 |
| Output High Voltage | V_{OH} | $I_{OH} = -1$ mA | 2.4 | | | V | 1 |
| Output Low Voltage | V_{OL} | $I_{OL} = 1$ mA | | | 0.55 | V | 1 |
| Output High Current | I_{OH} | $V_{OH} @ MIN = 1.0$ V | -33 | | | mA | 1 |
| | | $V_{OH} @ MAX = 3.135$ V | | | -33 | mA | 1 |
| Output Low Current | I_{OL} | $V_{OL} @ MIN = 1.95$ V | 30 | | | mA | 1 |
| | | $V_{OL} @ MAX = 0.4$ V | | | 38 | mA | 1 |
| Edge Rate | $\Delta V/\Delta t$ | Rising edge rate | 1 | | 4 | V/ns | 1 |
| Edge Rate | $\Delta V/\Delta t$ | Falling edge rate | 1 | | 4 | V/ns | 1 |
| Rise Time | t_{r1} | $V_{OL} = 0.4$ V, $V_{OH} = 2.4$ V | 0.5 | | 2 | ns | 1 |
| Fall Time | t_{f1} | $V_{OH} = 2.4$ V, $V_{OL} = 0.4$ V | 0.5 | | 2 | ns | 1 |
| Duty Cycle | d_{t1} | $V_T = 1.5$ V | 45 | | 55 | % | 1 |
| Jitter, Cycle to cycle | $t_{cyc-cyc}$ | $V_T = 1.5$ V | | | 180 | ps | 1 |

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5pF with Rs = 33Ω (unless otherwise specified)

¹Guaranteed by design and characterization, not 100% tested in production.

²All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that REF is at 14.31818MHz

Electrical Characteristics–USB - 48MHz

| PARAMETER | SYMBOL | CONDITIONS* | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|----------------------|--|---------|-----|---------|-------|-------|
| Long Accuracy | ppm | see Tperiod min-max values | -100 | | 100 | ppm | 1,2 |
| Clock period | T _{period} | 48.00MHz output nominal | 20.8229 | | 20.8344 | ns | 2 |
| Clock Low Time | T _{low} | Measure from < 0.6V | 9.3750 | | 11.4580 | ns | 2 |
| Clock High Time | T _{high} | Measure from > 2.0V | 9.3750 | | 11.4580 | ns | 2 |
| Output High Voltage | V _{OH} | I _{OH} = -1 mA | 2.4 | | | V | 1 |
| Output Low Voltage | V _{OL} | I _{OL} = 1 mA | | | 0.55 | V | 1 |
| Output High Current | I _{OH} | V _{OH} @ MIN = 1.0 V | -33 | | | mA | 1 |
| | | V _{OH} @ MAX = 3.135 V | | | -33 | mA | 1 |
| Output Low Current | I _{OL} | V _{OL} @ MIN = 1.95 V | 30 | | | mA | 1 |
| | | V _{OL} @ MAX = 0.4 V | | | 38 | mA | 1 |
| Rise Time | t _{r,USB} | V _{OL} = 0.4 V, V _{OH} = 2.4 V | 0.5 | | 1.5 | ns | 1 |
| Fall Time | t _{f,USB} | V _{OH} = 2.4 V, V _{OL} = 0.4 V | 0.5 | | 1.5 | ns | 1 |
| Duty Cycle | d _{tt} | V _T = 1.5 V | 45 | | 55 | % | 1 |
| Group Skew | t _{skew} | V _T = 1.5 V | | | 250 | ps | 1 |
| Jitter, Cycle to cycle | t _{cyc-cyc} | V _T = 1.5 V | | | 130 | ps | 1,2 |

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5pF with Rs = 33Ω (unless otherwise specified)

¹Guaranteed by design and characterization, not 100% tested in production.

²IDT recommended and/or chipset vendor layout guidelines must be followed to meet this specification

Electrical Characteristics–REF-14.318MHz

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | Notes |
|---------------------|----------------------|--|---------|-----|---------|-------|-------|
| Long Accuracy | ppm | see Tperiod min-max values | -300 | | 300 | ppm | 1,2 |
| Clock period | T _{period} | 14.318MHz output nominal | 69.8270 | | 69.8550 | ns | 2 |
| Clock Low Time | T _{low} | Measure from < 0.6V | 30.9290 | | 37.9130 | ns | 2 |
| Clock High Time | T _{high} | Measure from > 2.0V | 30.9290 | | 37.9130 | ns | 2 |
| Output High Voltage | V _{OH} | I _{OH} = -1 mA | 2.4 | | | V | 1 |
| Output Low Voltage | V _{OL} | I _{OL} = 1 mA | | | 0.4 | V | 1 |
| Output High Current | I _{OH} | V _{OH} @ MIN = 1.0 V, | -29 | | | mA | 1 |
| | | V _{OH} @ MAX = 3.135 V | | | -23 | mA | 1 |
| Output Low Current | I _{OL} | V _{OL} @ MIN = 1.95 V, | 29 | | | mA | 1 |
| | | V _{OL} @ MAX = 0.4 V | | | 27 | mA | 1 |
| Rise Time | t _{r1} | V _{OL} = 0.4 V, V _{OH} = 2.4 V | 1 | | 1.5 | ns | 1 |
| Fall Time | t _{f1} | V _{OH} = 2.4 V, V _{OL} = 0.4 V | 1 | | 1.5 | ns | 1 |
| Skew | t _{sk1} | V _T = 1.5 V | | | 250 | ps | 1 |
| Duty Cycle | d _{tt} | V _T = 1.5 V | 45 | | 55 | % | 1 |
| Jitter | t _{cyc-cyc} | V _T = 1.5 V | | | 200 | ps | 1 |

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5pF with Rs = 33Ω (unless otherwise specified)

¹Guaranteed by design and characterization, not 100% tested in production.

²All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

Clock Jitter Specifications—Low Power Differential Outputs

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---------------------------------|------------------|--|-----|-----|-----|-------------|-------|
| SRC/SB_SRC/ATIG Phase Jitter | $t_{jphasePLL}$ | PCIe Gen 1 | | | 86 | ps (p-p) | 1,2 |
| | $t_{jphaseLo}$ | PCIe Gen 2 $10kHz < f < 1.5MHz$ | | | 3 | ps (RMS) | 1,4 |
| | $t_{jphaseHigh}$ | PCIe Gen 2 $1.5MHz < f < Nyquist (50MHz)$ | | | 3.1 | ps (RMS) | 1,4 |

*TA = 0 - 70°C; Supply Voltage VDD = 3.3V +/-5%, Rs = 0ohms, CL = 2pF

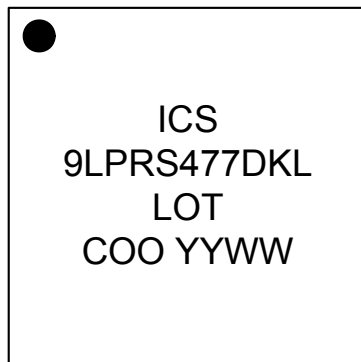
¹ Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

² Jitter specs are specified as measured on a clock characterization board. System designers need to take special care not to use these numbers, as the in-system performance will be somewhat degraded. The receiver EMTS (chispet or CPU) will have the rece

³ Phase jitter requirement: The designated Gen2 outputs will meet the reference clock jitter requirements from the PCI Express Gen2 Base Spec. The test is performed on a component test board under quiet conditions with all outputs on.

⁴ See <http://www.pcisig.com> for complete specs

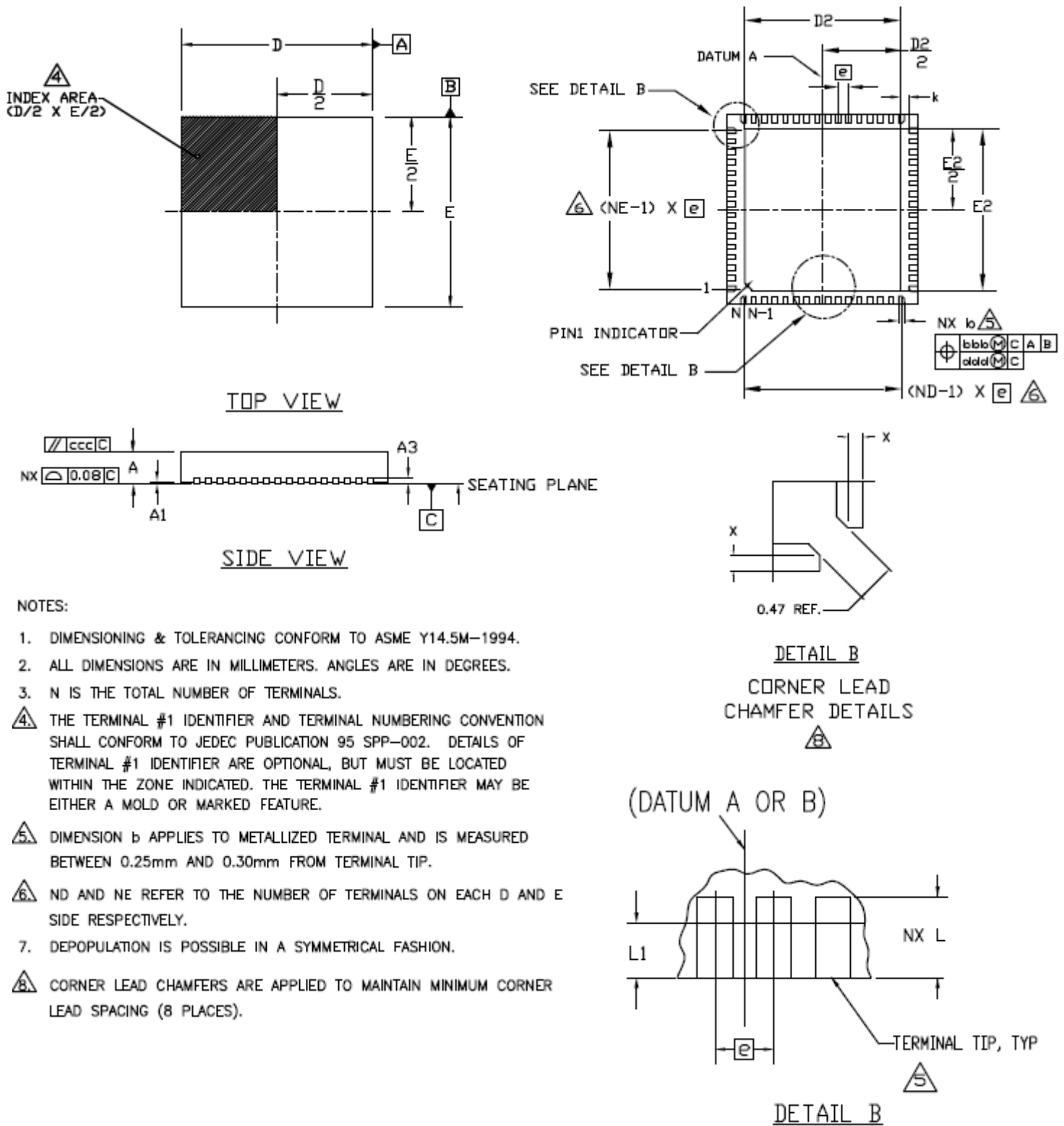
Marking Diagram



Notes:

1. "LOT" is the lot number.
2. "COO" is the country of origin.
3. "YYWW" is the last two digits of the year and week that the part was assembled.
4. "L" denotes RoHS compliant package.

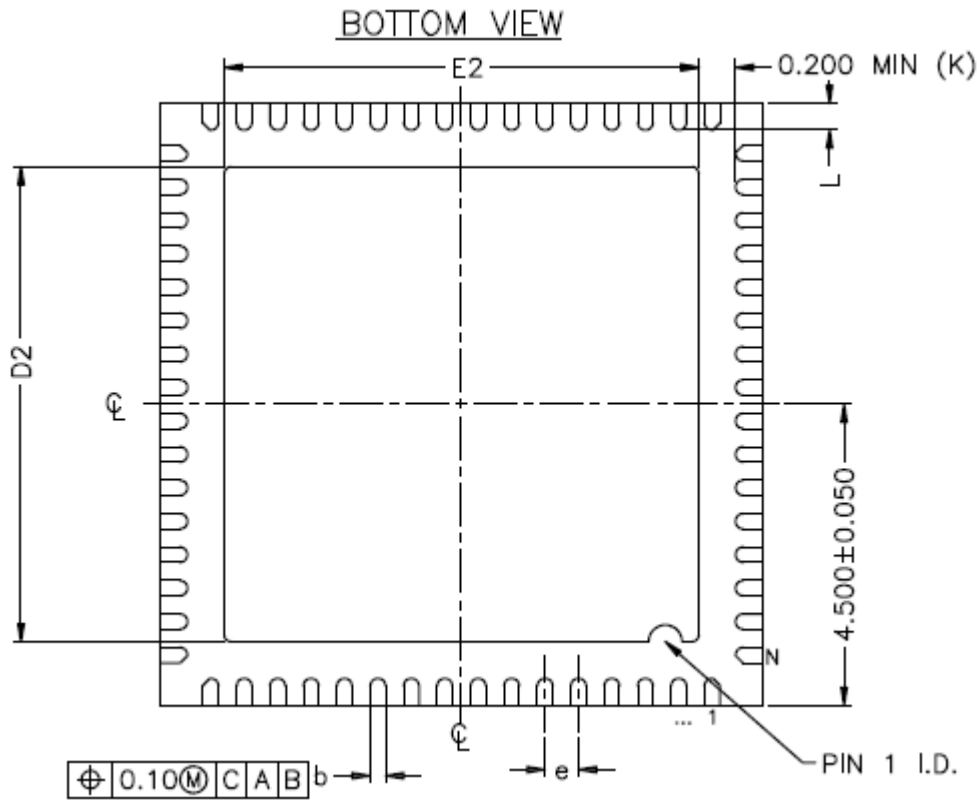
Package Outline and Package Dimensions (64-pin MLF)



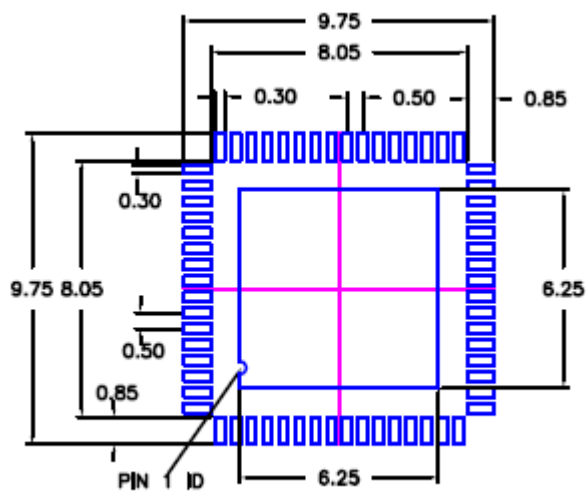
NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC PUBLICATION 95 SPP-002. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. CORNER LEAD CHAMFERS ARE APPLIED TO MAINTAIN MINIMUM CORNER LEAD SPACING (8 PLACES).

Package Outline and Package Dimensions, cont. (64-pin MLF)



| DIMENSIONS | | | |
|------------|--------------------|------|------|
| PACKAGE | 64L 9.0x9.0 - 0.50 | | |
| REF. | MIN. | NOM. | MAX. |
| A | 0.80 | 0.90 | 1.00 |
| b | 0.18 | 0.25 | 0.30 |
| D | 9.00 BSC | | |
| D2 | 6.0 | 6.15 | 6.25 |
| E | 9.00 BSC | | |
| E2 | 6.0 | 6.15 | 6.25 |
| e | 0.50 BSC. | | |
| L | 0.30 | 0.40 | 0.50 |
| N | 64 | | |
| ND | 16 | | |
| NE | 16 | | |
| k | 0.20 | | |



EPAD 6.15

NOTES:

1. ALL DIMENSION ARE IN mm, ANGLES IN DEGREES,
2. TOP DOWN VIEW, AS VIEWED ON PCB,
3. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
4. LAND PATTERN RECOMMENDATION PER IPC-7351B LP CALCULATOR.

| SYMBOL | COMMON DIMENSIONS | | | NOTE |
|---------------------------------|-------------------|-----------|------|------|
| | MIN. | NOM. | MAX. | |
| A1 | 0 | 0.02 | 0.05 | |
| A3 | - | 0.20 REF. | - | |
| X | b/2 | - | - | |
| TOLERANCES OF FORM AND POSITION | | | | |
| bbb | 0.10 | | | |
| ccc | 0.10 | | | |
| ddd | 0.05 | | | |

Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---------------------|-------------|--------------------|------------|-------------|
| 9LPRS477DKLF | see page 22 | Tubes | 64-pin MLF | 0 to +70° C |
| 9LPRS477DKLFT | | Tape and Reel | 64-pin MLF | 0 to +70° C |

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

"D" is the device revision designator (will not correlate with the datasheet revision).

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Revision History

| Rev. | Date | Originator | Description of Change |
|------|----------|------------|--|
| A | 01/28/14 | RDW | Move to final per char data. |
| B | 12/09/14 | D. C. | 1. Replaced "Anvil Singulation" with "Punch Singulation" in package outline and dimensions drawing. 2. Updated top-side device marking. |
| C | 01/07/15 | D. C. | Updated package drawing and dimensions from PUNCH to SAWN version. |

9LPRS477D

PROGRAMMABLE SYSTEM CLOCK CHIP FOR ATI RD790-K8™ BASED SYSTEMS

SYNTHESIZERS

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