19-Output DB1900Z for PCIe Gen1-4 and QPI/UPI

9ZX21901D

DATASHEET

Description

The 9ZX21901D is a second generation DB1900Z differential buffer for Intel Purley and newer platforms. The part is backwards compatible to the 9ZX21901C while offering much improved phase jitter performance. A fixed external feedback maintains low drift for critical QPI/UPI applications. In bypass mode, the 9ZX21901D can provide outputs up to 400MHz.

PCIe Clocking Architectures Supported

- Common Clocked (CC)
- Separate Reference No Spread (SRNS)
- Separate Reference Independent Spread (SRIS)

Typical Applications

- Servers, Storage, Networking

Output Features

- 19 HCSL output pairs

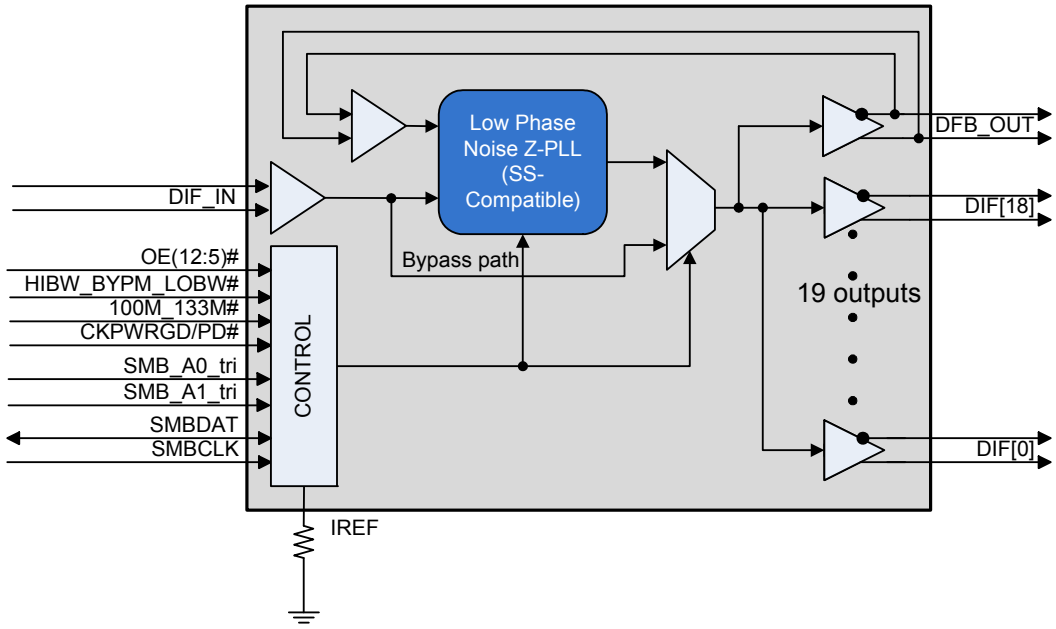
Key Specifications

- Cycle-to-cycle jitter: < 50ps
- Output-to-output skew: < 50ps
- Input-to-output delay: Fixed at 0 ps
- Input-to-output delay variation: < 50ps
- Phase jitter: PCIe Gen4 < 0.5ps rms
- Phase jitter: UPI 9.6GB/s < 0.1ps rms

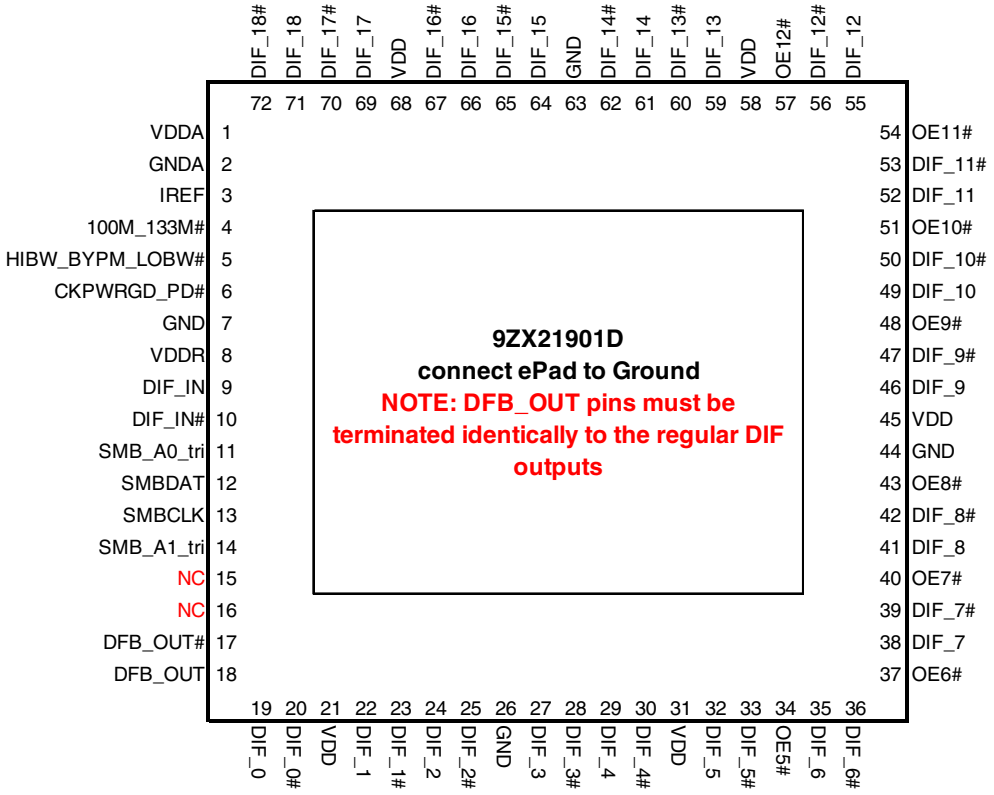
Features

- Fixed feedback path; 0ps input-to-output delay
- 9 Selectable SMBus addresses; multiple devices can share same SMBus segment
- 8 dedicated OE# pins; hardware control of outputs
- PLL or bypass mode; PLL can dejitter incoming clock
- Selectable PLL BW; minimizes jitter peaking in downstream PLL's
- Hardware or software control of PLL operating mode; change mode with software mode does not need power cycle
- Spread spectrum compatible; tracks spreading input clock for EMI reduction
- SMBus Interface; unused outputs can be disabled
- 100MHz and 133.33MHz PLL mode; legacy QPI support
- 72-QFN 10 x 10 mm package; small board footprint

Functional Block Diagram



Pin Configuration



72-pin VFQFPN (10mm x10 mm, 0.5mm pad pitch)

Functionality at Power Up (PLL Mode)

100M_133M#	DIF_IN (MHz)	DIF_x (MHz)
1	100.00	DIF_IN
0	133.33	DIF_IN

PLL Operating Mode Readback Table

HiBW_BypM_LoBW#	Byte0, bit 7	Byte 0, bit 6
Low (Low BW)	0	0
Mid (Bypass)	0	1
High (High BW)	1	1

PLL Operating Mode

HiBW_BypM_LoBW#	MODE
Low	PLL Lo BW
Mid	Bypass
High	PLL Hi BW

NOTE: PLL is OFF in Bypass Mode

Tri-level Input Thresholds

Level	Voltage
Low	<0.8V
Mid	1.2<Vin<1.8V
High	Vin > 2.2V

Power Connections

Pin Number		Description
VDD	GND	
1	2	Analog PLL
8	7	Analog Input
21, 31, 45, 58, 68	26, 44, 63	DIF clocks

9ZX21901 SMBus Addressing

Pin		SMBus Address
SMB_A1_tri	SMB_A0_tri	(Rd/Wrt bit = 0)
0	0	D8
0	M	DA
0	1	DE
M	0	C2
M	M	C4
M	1	C6
1	0	CA
1	M	CC
1	1	CE

Pin Descriptions

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	VDDA	PWR	Power supply for PLL core.
2	GNDA	GND	Ground pin for the PLL core.
3	IREF	OUT	This pin establishes the reference for the differential current-mode output pairs. It requires a fixed precision resistor to ground. 475ohm is the standard value for 100ohm differential impedance. Other impedances require different values. See data sheet.
4	100M_133M#	IN	Input to select operating frequency 1 = 100MHz, 0 = 133.33MHz
5	HIBW_BYPM_LOBW#	IN	Tri-level input to select High BW, Bypass or Low BW mode. See PLL Operating Mode Table for Details.
6	CKPWRGD_PD#	IN	3.3V input notifies device to sample latched inputs and start up on first high assertion, or exit Power Down Mode on subsequent assertions. Low enters Power Down Mode.
7	GND	GND	Ground pin.
8	VDDR	PWR	Power supply for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately. Nominally 3.3V.
9	DIF_IN	IN	HCSL true input.
10	DIF_IN#	IN	HCSL complementary input.
11	SMB_A0_tri	IN	SMBus address pin. This is a tri-level input that works in conjunction with other SMBus address pins to decode 3^n SMBus addresses, where n is the number
12	SMBDAT	I/O	Data pin of SMBUS circuitry
13	SMBCLK	IN	Clock pin of SMBUS circuitry
14	SMB_A1_tri	IN	SMBus address pin. This is a tri-level input that works in conjunction with other SMBus address pins to decode 3^n SMBus addresses, where n is the number
15	NC	N/A	No connection.
16	NC	N/A	No connection.
17	DFB_OUT#	OUT	Complementary half of differential feedback output, provides feedback signal to the PLL for synchronization with input clock to eliminate phase error.
18	DFB_OUT	OUT	True half of differential feedback output, provides feedback signal to the PLL for synchronization with the input clock to eliminate phase error.
19	DIF_0	OUT	HCSL true clock output.
20	DIF_0#	OUT	HCSL complementary clock output.
21	VDD	PWR	Power supply, nominally 3.3V.
22	DIF_1	OUT	HCSL true clock output.
23	DIF_1#	OUT	HCSL complementary clock output.
24	DIF_2	OUT	HCSL true clock output.
25	DIF_2#	OUT	HCSL complementary clock output.
26	GND	GND	Ground pin.
27	DIF_3	OUT	HCSL true clock output.
28	DIF_3#	OUT	HCSL complementary clock output.
29	DIF_4	OUT	HCSL true clock output.
30	DIF_4#	OUT	HCSL complementary clock output.
31	VDD	PWR	Power supply, nominally 3.3V.
32	DIF_5	OUT	HCSL true clock output.
33	DIF_5#	OUT	HCSL complementary clock output.
34	OE5#	IN	Active low input for enabling output 5. 1 = disable outputs, 0 = enable outputs.
35	DIF_6	OUT	HCSL true clock output.
36	DIF_6#	OUT	HCSL complementary clock output.

Pin Descriptions (cont.)

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
37	OE6#	IN	Active low input for enabling DIF pair 6. 1 =disable outputs, 0 = enable outputs
38	DIF_7	OUT	HCSL true clock output
39	DIF_7#	OUT	HCSL Complementary clock output
40	OE7#	IN	Active low input for enabling DIF pair 7. 1 =disable outputs, 0 = enable outputs
41	DIF_8	OUT	HCSL true clock output
42	DIF_8#	OUT	HCSL Complementary clock output
43	OE8#	IN	Active low input for enabling DIF pair 8. 1 =disable outputs, 0 = enable outputs
44	GND	GND	Ground pin.
45	VDD	PWR	Power supply, nominal 3.3V
46	DIF_9	OUT	HCSL true clock output
47	DIF_9#	OUT	HCSL Complementary clock output
48	OE9#	IN	Active low input for enabling DIF pair 9. 1 =disable outputs, 0 = enable outputs
49	DIF_10	OUT	HCSL true clock output
50	DIF_10#	OUT	HCSL Complementary clock output
51	OE10#	IN	Active low input for enabling DIF pair 10. 1 =disable outputs, 0 = enable outputs
52	DIF_11	OUT	HCSL true clock output
53	DIF_11#	OUT	HCSL Complementary clock output
54	OE11#	IN	Active low input for enabling DIF pair 11. 1 =disable outputs, 0 = enable outputs
55	DIF_12	OUT	HCSL true clock output
56	DIF_12#	OUT	HCSL Complementary clock output
57	OE12#	IN	Active low input for enabling DIF pair 12. 1 =disable outputs, 0 = enable outputs
58	VDD	PWR	Power supply, nominal 3.3V
59	DIF_13	OUT	HCSL true clock output
60	DIF_13#	OUT	HCSL Complementary clock output
61	DIF_14	OUT	HCSL true clock output
62	DIF_14#	OUT	HCSL Complementary clock output
63	GND	GND	Ground pin.
64	DIF_15	OUT	HCSL true clock output
65	DIF_15#	OUT	HCSL Complementary clock output
66	DIF_16	OUT	HCSL true clock output
67	DIF_16#	OUT	HCSL Complementary clock output
68	VDD	PWR	Power supply, nominal 3.3V
69	DIF_17	OUT	HCSL true clock output
70	DIF_17#	OUT	HCSL Complementary clock output
71	DIF_18	OUT	HCSL true clock output
72	DIF_18#	OUT	HCSL Complementary clock output

Electrical Characteristics – Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	VDDx				3.9	V	1,2
Input Low Voltage	V_{IL}		GND-0.5			V	1
Input High Voltage	V_{IH}	Except for SMBus interface			V_{DD}+0.5	V	1,3
Input High Voltage	V_{IHSMB}	SMBus clock and data pins			3.9	V	1
Storage Temperature	Ts		-65		150	°C	1
Junction Temperature	Tj				125	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

[3] Not to exceed 3.9V.

Electrical Characteristics – DIF_IN Clock Input Parameters

Over specified temperature and voltage ranges unless otherwise indicated. See Test Loads for loading conditions.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input Crossover Voltage	V_{CROSS}	Crossover voltage	150		900	mV	1
Input Swing - DIF_IN	V_{SWING}	Differential value	300			mV	1
Input Slew Rate - DIF_IN	dv/dt	Measured differentially	0.35		8	V/ns	1,2
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND	-5		5	uA	
Input Duty Cycle	d_{tin}	Measurement from differential waveform	45		55	%	1
Input Jitter - Cycle to Cycle	J_{DIFIn}	Differential measurement	0		125	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2]Slew rate measured through +/-75mV window centered around differential zero.

Electrical Characteristics – SMBus

Over specified temperature and voltage ranges unless otherwise indicated. See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SMBus Input Low Voltage	V_{ILSMB}				0.8	V	
SMBus Input High Voltage	V_{IHSMB}		2.1		V_{DDSMB}	V	
SMBus Output Low Voltage	V_{OLSMB}	@ I_{PULLUP}			0.4	V	
SMBus Sink Current	I_{PULLUP}	@ V_{OL}	4			mA	
Nominal Bus Voltage	V_{DDSMB}		2.7		3.6	V	1
SCLK/SDATA Rise Time	t_{RSMB}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Fall Time	t_{FSMB}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1
SMBus Operating Frequency	f_{MAXSMB}	Maximum SMBus operating frequency			400	kHz	5

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]Control input must be monotonic from 20% to 80% of input swing.

[3]Time from deassertion until outputs are >200 mV

[4]DIF_IN input

[5]The differential input clock must be running for the SMBus to be active

Electrical Characteristics – Current Consumption

Over specified temperature and voltage ranges unless otherwise indicated. See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Current	I_{DDA}	VDDA, PLL Mode@100MHz		42	45	mA	1
Operating Supply Current	I_{DD}	All other VDD pins		466	490	mA	
Powerdown Current	I_{DDPD}	All DIF pairs Hi-Z		4	5	mA	

[1.] Includes VDDR if applicable

Electrical Characteristics – Input/Supply/Common Parameters

Over specified temperature and voltage ranges unless otherwise indicated. See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	VDDx	Supply voltage for core and analog	3.135	3.3	3.465	V	
Ambient Operating Temperature	T_{AMB}	Commercial range (T_{COM})	0		70	°C	
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus, tri-level inputs	2		V_{DD} + 0.3	V	
Input Low Voltage	V_{IL}	Single-ended inputs, except SMBus, tri-level inputs	GND - 0.3		0.8	V	
Input High Voltage	V_{IH}	Tri-Level Inputs	2.2		V_{DD} + 0.3	V	
Input Mid Voltage	V_{IL}	Tri-Level Inputs	1.2	VDD/2	1.8	V	
Input Low Voltage	V_{IL}	Tri-Level Inputs	GND - 0.3		0.8	V	
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = VDD	-5		5	µA	
	I_{INP}	Single-ended inputs V_{IN} = 0 V; Inputs with internal pull-up resistors V_{IN} = VDD; Inputs with internal pull-down resistors	-200		200	µA	
Input Frequency	F_{ibyp}	V_{DD} = 3.3 V, Bypass mode	33		400	MHz	
	F_{ipll}	V_{DD} = 3.3 V, 100MHz PLL mode	98.5	100.00	102	MHz	
	F_{ipll}	V_{DD} = 3.3 V, 133.33MHz PLL mode	125	130.50	135	MHz	
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic Inputs, except DIF_IN	1.5		5	pF	1
	C_{INDIF_IN}	DIF_IN differential clock inputs	1.5		2.7	pF	1,4
	C_{OUT}	Output pin capacitance			6	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock		1.4	1.8	ms	1,2
Input SS Modulation Frequency PCIe	$f_{MODINPCIe}$	Allowable Frequency for PCIe Applications (Triangular Modulation)	30		33	kHz	
OE# Latency	$t_{LATOE\#}$	DIF start after OE# assertion DIF stop after OE# deassertion	4	6	10	clocks	1,2,3
Tdrive_PD#	t_{DRVPD}	DIF output enable after PD# de-assertion		85	300	µs	1,3
Tfall	t_F	Fall time of control inputs			5	ns	2
Trise	t_R	Rise time of control inputs			5	ns	2

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are > 200 mV.

[4] DIF_IN input.

Electrical Characteristics – DIF HCSL/LP-HCSL Outputs

Over specified temperature and voltage ranges unless otherwise indicated. See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	INDUSTRY LIMIT	UNITS	NOTES
Slew rate	dV/dt	Scope averaging on	1.5	2.2	3.0	0.6 - 4	V/ns	1,2,3
Slew rate matching	ΔdV/dt	Slew rate matching, Scope averaging on		7.3	18	20	%	1,2,4,7
Max Voltage	Vmax	Measurement on single ended signal using absolute value. (Scope averaging off)	719	772	842	1150	mV	7,8
Min Voltage	Vmin			11	50	-300		7,8
Crossing Voltage (abs)	Vcross_abs	Scope averaging off	310	367	400	250 - 550	mV	1,5,7
Crossing Voltage (var)	Δ-Vcross	Scope averaging off		14	30	140	mV	1,6,7

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform

[3] Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting ↑-Vcross to be smaller than Vcross absolute.

[7] At default SMBus settings.

[8] If driving a receiver with input terminations, the Vmax and Vmin values will be halved.

Electrical Characteristics – Skew and Differential Jitter Parameters

Over specified temperature and voltage ranges unless otherwise indicated. See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
CLK_IN, DIF[x:0]	t_{SPO_PLL}	Input-to-Output Skew in PLL mode at 100MHz, nominal temperature and voltage	-100	54	100	ps	1,2,4,5,8
CLK_IN, DIF[x:0]	t_{PD_BYP}	Input-to-Output Skew in Bypass mode at 100MHz, nominal temperature and voltage	1.9	2.6	3	ns	1,2,3,5,8
CLK_IN, DIF[x:0]	t_{DSPO_PLL}	Input-to-Output Skew Variation in PLL mode at 100MHz, across voltage and temperature	-50	0.0	50	ps	1,2,3,5,8
CLK_IN, DIF[x:0]	t_{DSPO_BYP}	Input-to-Output Skew Variation in Bypass mode at 100MHz, across voltage and temperature, $T_{AMB} = T_{COM}$	-250	0.0	250	ps	1,2,3,5,8
DIF[x:0]	t_{SKEW_ALL}	Output-to-Output Skew across all outputs, common to PLL and Bypass mode, at 100MHz		32	50	ps	1,2,3,8
PLL Jitter Peaking	$j_{peak\text{-}hibw}$	LOBW#_BYPASS_HIBW = 1	0	1.4	2.5	dB	7,8
PLL Jitter Peaking	$j_{peak\text{-}lobw}$	LOBW#_BYPASS_HIBW = 0	0	1.2	2	dB	7,8
PLL Bandwidth	pll_{HIBW}	LOBW#_BYPASS_HIBW = 1	2	2.8	4	MHz	8,9
PLL Bandwidth	pll_{LOBW}	LOBW#_BYPASS_HIBW = 0	0.7	1.1	1.4	MHz	8,9
Duty Cycle	t_{DC}	Measured differentially, PLL Mode	45	50	55	%	1
Duty Cycle Distortion	t_{DCD}	Measured differentially, Bypass Mode at 100MHz	-1	-0.5	0	%	1,10
Jitter, Cycle to Cycle	$t_{jcyc\text{-}cyc}$	PLL mode		17	50	ps	1,11
		Additive Jitter in Bypass Mode		0.1	5	ps	1,11

[1] Measured into fixed 2 pF load cap. Input to output skew is measured at the first output edge following the corresponding input.

[2] Measured from differential cross-point to differential cross-point. This parameter can be tuned with external feedback path, if present.

[3] All Bypass Mode Input-to-Output specs refer to the timing between an input edge and the specific output edge created by it.

[4] This parameter is deterministic for a given device.

[5] Measured with scope averaging on to find mean value.

[6] t is the period of the input clock.

[7] Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.

[8.] Guaranteed by design and characterization, not 100% tested in production.

[9] Measured at 3 db down or half power point.

[10] Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

[11] Measured from differential waveform.

Electrical Characteristics – Filtered Phase Jitter Parameters - PCIe Common Clocked (CC) Architectures

Over specified temperature and voltage ranges unless otherwise indicated. See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	INDUSTRY LIMIT	UNITS	Notes
Phase Jitter, PLL Mode	$t_{jphPCIeG1-CC}$	PCIe Gen 1		18	30	86	ps (p-p)	1,2,3
	$t_{jphPCIeG2-CC}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz (PLL BW of 5-16MHz or 8-5MHz, CDR = 5MHz)		0.4	0.8	3	ps (rms)	1,2
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5-16MHz or 8-5MHz, CDR = 5MHz)		1.1	1.6	3.1	ps (rms)	1,2
	$t_{jphPCIeG3-CC}$	PCIe Gen 3 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)		0.28	0.40	1	ps (rms)	1,2
	$t_{jphPCIeG4-CC}$	PCIe Gen 4 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)		0.28	0.40	0.5	ps (rms)	1,2
Additive Phase Jitter, Bypass mode	$t_{jphPCIeG1-CC}$	PCIe Gen 1		0.1	0.1	n/a	ps (p-p)	1,2
	$t_{jphPCIeG2-CC}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz (PLL BW of 5-16MHz or 8-5MHz, CDR = 5MHz)		0.1	0.1		ps (rms)	1,2,4
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5-16MHz or 8-5MHz, CDR = 5MHz)		0.105	0.13		ps (rms)	1,2,4
	$t_{jphPCIeG3-CC}$	PCIe Gen 3 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)		0.1	0.1		ps (rms)	1,2,4
	$t_{jphPCIeG4-CC}$	PCIe Gen 4 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)		0.1	0.1		ps (rms)	1,2,4

[1] Applies to all outputs,, when driven by 9SQL4958 or equivalent

[2] Based on PCIe Base Specification Rev4.0 version 0.7 draft. See http://www.pcisig.com for latest specifications.

[3] Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

[4] For RMS values additive jitter is calculated by solving the following equation for b [*a^2+b^2=c^2*] where a is rms input jitter and c is rms total jitter.

Electrical Characteristics – Filtered Phase Jitter Parameters - PCIe Separate Reference Independent Spread (SRIS) Architectures

Over specified temperature and voltage ranges unless otherwise indicated. See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	INDUSTRY LIMIT	UNITS	Notes
Phase Jitter, PLL Mode	$t_{jphPCIeG1-SRIS}$	PCIe Gen 1		n/a		n/a	ps (p-p)	1,2,3
	$t_{jphPCIeG2-SRIS}$	PCIe Gen 2 (PLL BW of 16MHz , CDR = 5MHz)		0.8	1.1	2	ps (rms)	1,2
	$t_{jphPCIeG3-SRIS}$	PCIe Gen 3 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)		0.6	0.7	TBD	ps (rms)	1,2
	$t_{jphPCIeG4-SRIS}$	PCIe Gen 4 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)		n/a		n/a	ps (rms)	1,2
AdditivePhase Jitter, Bypass mode	$t_{jphPCIeG1-SRIS}$	PCIe Gen 1		n/a		n/a	ps (p-p)	1,2
	$t_{jphPCIeG2-SRIS}$	PCIe Gen 2 (PLL BW of 16MHz , CDR = 5MHz)		0.0	0.01		ps (rms)	1,2,4
	$t_{jphPCIeG3-SRIS}$	PCIe Gen 3 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)		0.0	0.01		ps (rms)	1,2,4
	$t_{jphPCIeG4-SRIS}$	PCIe Gen 4 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)		n/a			ps (rms)	1,2,4

[1] Applies to all outputs, when driven by 9SQL4958 or equivalent

[2] Preliminary based on PCIe Base Specification Rev3.1a. PCIe Gen4 is expected to remove the SRIS specifications. These filters are different than Common Clock filters. See http://www.pcisig.com for latest specifications.

[3] Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

[4] For RMS values, additive jitter is calculated by solving the following equation for b [*a^2+b^2=c^2*] where a is rms input jitter and c is rms total

Electrical Characteristics – Filtered Phase Jitter Parameters - QPI/UPI

Over specified temperature and voltage ranges unless otherwise indicated. See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	IND.LIMIT	UNITS	Notes
Phase Jitter, PLL Mode	t_{jphQPI_UPI}	QPI & SMI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI)		0.15	0.3	0.5	ps (rms)	1,2
		QPI & SMI (100MHz, 8.0Gb/s, 12UI)		0.08	0.12	0.3	ps (rms)	1,2
		QPI & SMI (100MHz, 9.6Gb/s, 12UI)		0.07	0.1	0.2	ps (rms)	1,2
Additive Phase Jitter, Bypass mode	t_{jphQPI_UPI}	QPI & SMI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI)		0.009	0.12	n/a	ps (rms)	1,2,3
		QPI & SMI (100MHz, 8.0Gb/s, 12UI)		0.020	0.07		ps (rms)	1,2,3
		QPI & SMI (100MHz, 9.6Gb/s, 12UI)		0.016	0.06		ps (rms)	1,2,3

[1] Applies to all outputs, when driven by 9SQL4958 or equivalent

[2] Calculated from Intel-supplied Clock Jitter Tool v 1.6.6

[3] For RMS values additive jitter is calculated by solving the following equation for b [*a^2+b^2=c^2*] where a is rms input jitter and c is rms total jitter.

Electrical Characteristics – Unfiltered Phase Jitter Parameters - 12kHz to 20MHz

Over specified temperature and voltage ranges unless otherwise indicated. See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	IND.LIMIT	UNITS	Notes
Phase Jitter, PLL Mode	$t_{jph12k-20MHi}$	PLL High BW, SSC OFF, 100MHz	161	178	198	n/a	fs (rms)	1,2
Phase Jitter, PLL Mode	$t_{jph12k-20MLo}$	PLL Low BW, SSC OFF, 100MHz	175	193	207	n/a	fs (rms)	1,2
Additive Phase Jitter, Bypass mode	$t_{jph12k-20MByp}$	Bypass Mode, SSC OFF, 100MHz	104	104	110	n/a	fs (rms)	1,2,3

[1] Applies to all outputs.

[2] 12kHz to 20MHz brick wall filter.

[3] For RMS values additive jitter is calculated by solving the following equation for b [*a^2+b^2=c^2*] where a is rms input jitter and c is rms total jitter.

Power Management Table

Inputs		Control Bits/Pins		Outputs			PLL State
CKPWRGD_PD#	DIF_IN/ DIF_IN#	SMBus EN bit	OE# Pin	DIF(5:12)	Other DIF	DFB_OUT	
0	X	X	X	Hi-Z[1]	Hi-Z[1]	Hi-Z[1]	OFF
1	Running	0	X	Hi-Z[1]	Hi-Z[1]	Running	ON
		1	0	Running	Running	Running	ON
		1	1	Hi-Z[1]	Running	Running	ON

NOTE: 1. Due to external pull down resistors, HI-Z results in Low/Low on the True/Complement outputs

Clock Periods – Differential Outputs with Spread Spectrum Disabled

SSC OFF	Center Freq. MHz	Measurement Window							Units	Notes
		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
		-c2c jitter AbsPer Min	-SSC Short-Term Average Min	- ppm Long-Term Average Min	0 ppm Period Nominal	+ ppm Long-Term Average Max	+SSC Short-Term Average Max	+c2c jitter AbsPer Max		
DIF	100.00	9.94900		9.99900	10.00000	10.00100		10.05100	ns	1,2,3
	133.33	7.44925		7.49925	7.50000	7.50075		7.55075	ns	1,2,4

Clock Periods – Differential Outputs with Spread Spectrum Enabled

SSC ON	Center Freq. MHz	Measurement Window							Units	Notes
		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
		-c2c jitter AbsPer Min	-SSC Short-Term Average Min	- ppm Long-Term Average Min	0 ppm Period Nominal	+ ppm Long-Term Average Max	+SSC Short-Term Average Max	+c2c jitter AbsPer Max		
DIF	99.75	9.94906	9.99906	10.02406	10.02506	10.02607	10.05107	10.10107	ns	1,2,3
	133.00	7.44930	7.49930	7.51805	7.51880	7.51955	7.53830	7.58830	ns	1,2,4

Notes:

[1]Guaranteed by design and characterization, not 100% tested in production.

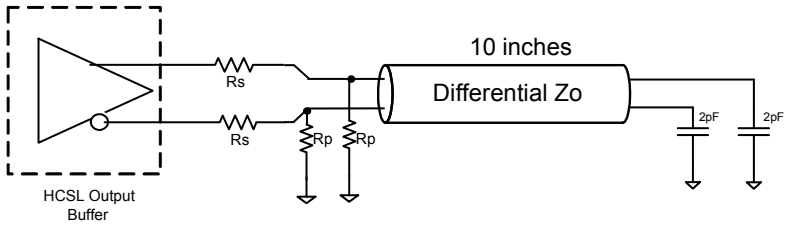
[2] All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK420BQ accuracy requirements (+/-100ppm). The device itself does not contribute to ppm error.

[3] Driven by SRC output of main clock, 100 MHz PLL Mode or Bypass mode

[4] Driven by CPU output of main clock, 133 MHz PLL Mode or Bypass mode

Test Loads

9ZX21901D Characterization Test Loads



Differential Output Termination Table

DIF Zo (Ω)	Iref (Ω)	Rs (Ω)	Rp (Ω)
100	475	33	50
85	412	27	42.2 or 43.2

Alternate Terminations

The 9ZX21901D can easily drive LVPECL, LVDS, CML, and SSTL logic. See "AN-891 Driving LVPECL, LVDS, CML, and SSTL Logic with IDT's "Universal" Low-Power HCSL Outputs" for details.

General SMBus Serial Interface Information

(see also 9ZX21901 SMBus Addressing on page 2)

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address $XX_{(H)}$
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending **Byte N through Byte N+X-1**
- IDT clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a Stop bit

Index Block Write Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Note: $XX_{(H)}$ is defined by SMBus Address select pins.

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address $XX_{(H)}$
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address $YY_{(H)}$
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

SMBusTable: PLL Mode, and Frequency Select Register

Byte 0	Pin	Name	Control Function	Type	0	1	Default
Bit 7	5	PLL Mode 1	PLL Operating Mode Rd back 1	R	See PLL Operating Mode		Latch
Bit 6	5	PLL Mode 0	PLL Operating Mode Rd back 0	R	Readback Table		Latch
Bit 5	72/71	DIF_18_En	Output Enable	RW	Hi-Z	Enable	1
Bit 4	70/69	DIF_17_En	Output Enable	RW	Hi-Z	Enable	1
Bit 3	67/66	DIF_16_En	Output Enable	RW	Hi-Z	Enable	1
Bit 2		Reserved					0
Bit 1		Reserved					0
Bit 0	4	100M_133M#	Frequency Select Readback	R	133MHz	100MHz	Latch

SMBusTable: Output Control Register

Byte 1	Pin	Name	Control Function	Type	0	1	Default
Bit 7	39/38	DIF_7_En	Output Enable	RW	Hi-Z	OE# pin controlled	1
Bit 6	35/36	DIF_6_En	Output Enable	RW			1
Bit 5	32/33	DIF_5_En	Output Enable	RW			1
Bit 4	29/30	DIF_4_En	Output Enable	RW		Enable	1
Bit 3	27/28	DIF_3_En	Output Enable	RW			1
Bit 2	24/25	DIF_2_En	Output Enable	RW			1
Bit 1	22/23	DIF_1_En	Output Enable	RW			1
Bit 0	19/20	DIF_0_En	Output Enable	RW			1

SMBusTable: Output Control Register

Byte 2	Pin	Name	Control Function	Type	0	1	Default
Bit 7	65/64	DIF_15_En	Output Enable	RW	Hi-Z	Enable	1
Bit 6	62/61	DIF_14_En	Output Enable	RW			1
Bit 5	60/59	DIF_13_En	Output Enable	RW			1
Bit 4	56/55	DIF_12_En	Output Enable	RW		OE# pin controlled	1
Bit 3	53/52	DIF_11_En	Output Enable	RW			1
Bit 2	50/49	DIF_10_En	Output Enable	RW			1
Bit 1	47/46	DIF_9_En	Output Enable	RW			1
Bit 0	42/41	DIF_8_En	Output Enable	RW			1

SMBusTable: Output Enable Pin Status Readback Register

Byte 3	Pin	Name	Control Function	Type	0	1	Default
Bit 7	57	OE_RB12	Real Time readback of OE#12	R	OE# pin Low	OE# Pin High	Real time
Bit 6	54	OE_RB11	Real Time readback of OE#11	R			Real time
Bit 5	51	OE_RB10	Real Time readback of OE#10	R			Real time
Bit 4	48	OE_RB9	Real Time readback of OE#9	R			Real time
Bit 3	43	OE_RB8	Real Time readback of OE#8	R			Real time
Bit 2	40	OE_RB7	Real Time readback of OE#7	R			Real time
Bit 1	37	OE_RB6	Real Time readback of OE#6	R			Real time
Bit 0	34	OE_RB5	Real Time readback of OE#5	R			Real time

SMBusTable: PLL SW Override Control Register

Byte 4	Pin	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		PLL_SW_EN	Enable S/W control of PLL BW	RW	HW Latch	SMBus Control	0
Bit 2		PLL Mode 1	PLL Operating Mode 1	RW	See PLL Operating Mode		0
Bit 1		PLL Mode 0	PLL Operating Mode 1	RW	Readback Table		0
Bit 0		Reserved					0

Note: Setting bit 3 to '1' allows the user to override the Latch value from pin 4 via use of bits 2 and 1. Use the values from the PLL Operating Mode Readback Table. Note that Byte 0, Bits 7:6 will keep the value originally latched on pin 4. A warm reset of the system will have to be completed if the user changes these bits.

SMBusTable: Vendor & Revision ID Register

Byte 5	Pin	Name	Control Function	Type	0	1	Default
Bit 7	-	RID3	REVISION ID	R	D rev = 0011		0
Bit 6	-	RID2		R			0
Bit 5	-	RID1		R			1
Bit 4	-	RID0		R			1
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

SMBusTable: DEVICE ID

Byte 6	Pin	Name	Control Function	Type	0	1	Default
Bit 7	-	Device ID 7 (MSB)		R	Device ID is 219 decimal or DB hex.		1
Bit 6	-	Device ID 6		R			1
Bit 5	-	Device ID 5		R			0
Bit 4	-	Device ID 4		R			1
Bit 3	-	Device ID 3		R			1
Bit 2	-	Device ID 2		R			0
Bit 1	-	Device ID 1		R			1
Bit 0	-	Device ID 0		R			1

SMBusTable: Byte Count Register

Byte 7	Pin	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4	-	BC4	Writing to this register configures how many bytes will be read back.	RW	Default value is 8 hex, so 9 bytes (0 to 8) will be read back by default.		0
Bit 3	-	BC3		RW			1
Bit 2	-	BC2		RW			0
Bit 1	-	BC1		RW			0
Bit 0	-	BC0		RW			0

SMBusTable: Reserved Register

Byte 8	Pin	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		Reserved					0
Bit 2		Reserved					0
Bit 1		Reserved					0
Bit 0		Reserved					0

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/nlnlg72-package-outline-100-x-100-mm-body-epad-59-mm-sq-050-mm-pitch-vfqfpn-sawn

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θJA	Still air		28.2		°C/W
	θJA	1 m/s air flow		21.6		°C/W
	θJA	3 m/s air flow		17.9		°C/W
Thermal Resistance Junction to Case	θJC			14.4		°C/W
Thermal Resistance Junction to Board	θJB			0.61		°C/W

Marking Diagram

Notes:

1. “LOT” is the lot sequence number.
2. “COO” denotes country of origin.
3. “YYWW” is the last two digits of the year and week that the part was assembled.
4. “LF” denotes RoHS compliant package.

Ordering Information

Part / Order Number	Shipping Package	Package	Temperature
9ZX21901DKLF	Trays	72-pin VFQFPN	0 to +70°C
9ZX21901DKLFT	Tape and Reel	72-pin VFQFPN	0 to +70°C

"LF" designates PB-free configuration, RoHS compliant.

"D" designates die revision and does not correlate to data sheet revision.

Revision History

Issue Date	Description
9/16/2016	1. Updated electrical tables 2. Move to Final
10/5/2016	Changed IDD maximum value from 450 to 490mA
2/15/2017	1. Features change: "Hardware or software control of PLL operating mode; change mode with software mode does not need power cycle." 2. Change Max of Powerdown Current IDDPD to 5mA. 3. Input frequency of PLL mode: (1). Change Min of 100MHz to 98.5HMz and Max of 100MHz to 102MHz. (2). Change Max of 133.33MHz to 130.5MHz and Max of 133.33MHz to 135MHz. 4. DIF HCSL/LP-HCSL Outputs: (1). Change Min of Max Voltage to 719mV and Max of Max Voltage to 842mV. (2). Change Min of (Crossing Voltage (abs)) to 310mV and Max of (Crossing Voltage (abs)) to 400mV. 5. Change Typ of Cycle to cycle jitter of PLL mode to 17ps. 6.Filtered Phase Jitter Parameters - PCIe Common Clocked (CC) Architectures" (1).Change Typ of additive phase jitter of bypass mode of PCIe Gen1 to 0.1. (2). Change Typ and max of additive phase jitter of bypass mode of PCIe Gen2 Lo Band to 0.1. (3). Change Typ and max of additive phase jitter of bypass mode of PCIe Gen3 to 0.1. (4). Change Typ and max of additive phase jitter of bypass mode of PCIe Gen4 to 0.1. 7.Unfiltered Phase Jitter Parameters - 12kHz to 20MHz (1). Change Min,TYP and Max of PLLmode High BW to 161, 178, 198ps. (2). Change Min,TYP and Max of PLLmode Low BW to 175, 193, 207ps. (3). Change Min,TYP and Max of Bpmode to 104, 104, 110ps.
12/1/2017	Removed “5V tolerant” reference in pins 12 and 13 descriptions.
4/17/2018	Updated absolute maximum supply voltage rating and VIHSMB to 3.9V.

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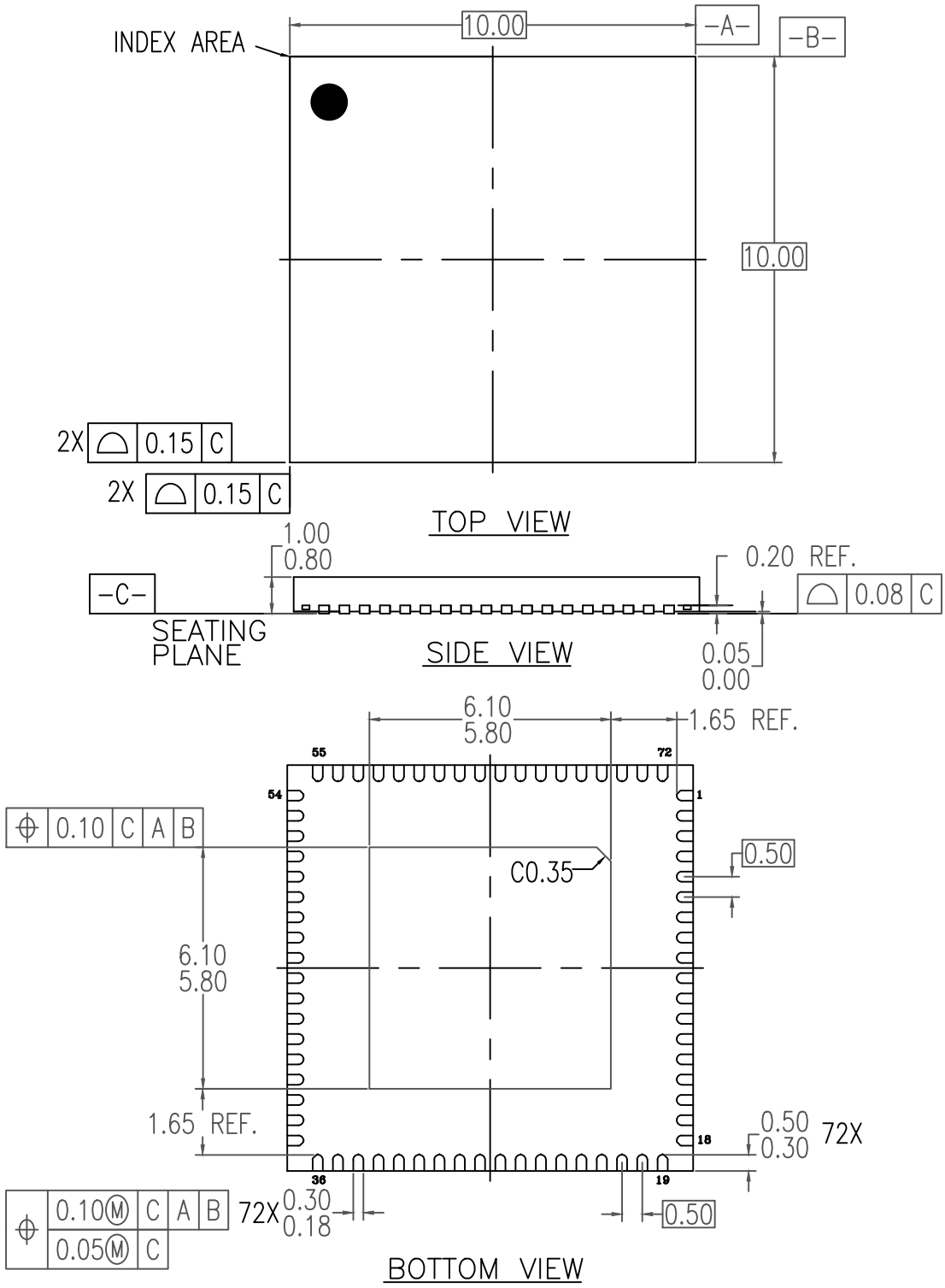
72-VFQFPN, Package Outline Drawing

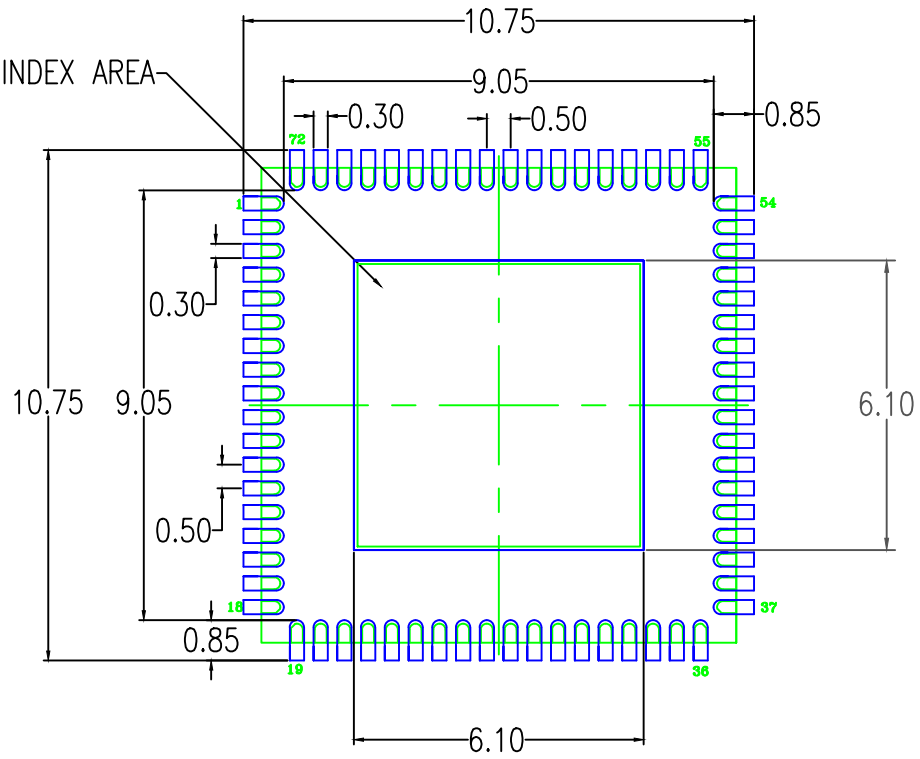
10.0 x 10.0 x 0.90 mm Body, Epad 5.95 x 5.95 mm 0.50mm Pitch

NLG72P1, PSC-4208-01, Rev 03, Page 1



NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1994
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. INDEX AREA (PIN1 IDENTIFIER)



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
Sept 3, 2019	Rev 03	Update P1 Dimension from 5. 8 to 5.95 mm SQ
May 8, 2017	Rev 02	Change Package Code QFN to VFQFPN