GENERAL DESCRIPTION

The IDTF2255 is a low insertion loss Voltage Variable RF Attenuator (VVA) designed for a multitude of wireless and other RF applications. This device covers a broad frequency range from 1MHz to 3000MHz. In addition to providing low insertion loss, the IDTF2255 provides excellent linearity performance over its entire voltage control and attenuation range.

The F2255 uses a single positive supply voltage of 3.15V to 5.25V. Other features include the VMODE pin allowing either positive or negative voltage control slope vs attenuation and multi-directional operation meaning the RF input can be applied to either RF1 or RF2 pins. Control voltage ranges from 0V to 3.6V using either positive or negative control voltage slope.

COMPETITIVE ADVANTAGE

IDTF2255 provides extremely low insertion loss and superb IP3, IP2, Return Loss and Slope Linearity across the control range. Comparing to competitive VVAs this device is better as follows:

- Operation down to 1MHz
- Insertion Loss @ 500MHz: 1.1dB
- Maximum Attenuation Slope: 33dB/Volt
- Minimum Output IP3: 98dBm
- Minimum Input IP2: 74dBm
- High Operating Temperature: +105°C

APPLICATIONS

- Base Station 2G, 3G, 4G
- Portable Wireless
- Repeaters and E911 systems
- Digital Pre-Distortion
- Point to Point Infrastructure
- Public Safety Infrastructure
- Satellite Receivers and Modems
- WIMAX Receivers and Transmitters
- Military Radios covering HF, VHF, UHF
- RFID handheld and portable readers
- Cable Infrastructure
- Wireless LAN
- Test / ATE Equipment

FEATURES

- Low Insertion Loss: 1.1dB @ 500MHz
- Typical / Min IIP3: 60dBm / 46dBm
- Typical / Min IIP2: 98dBm / 74dBm
- 33dB Attenuation Range
- Bi-directional RF ports
- +36dBm Input P1dB compression
- VMODE pin allows either positive or negative control response
- Linear-in-dB attenuation characteristic
- Supply voltage: 3.15V to 5.25V
- VCTRL range: 0V to 3.6V using 5V supply
- +105°C max operating temperature
- 3mm x 3mm, 16-pin QFN package

DEVICE BLOCK DIAGRAM

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Part#</th>
<th>RF Freq Range (MHz)</th>
<th>Insertion Loss (dB)</th>
<th>IIP3 (dBm)</th>
<th>Pinout Compatibility</th>
</tr>
</thead>
<tbody>
<tr>
<td>F2250</td>
<td>50 - 6000</td>
<td>1.5 (at 2GHz)</td>
<td>+65</td>
<td>RFMD</td>
</tr>
<tr>
<td>F2255</td>
<td>1 - 3000</td>
<td>1.1 (at 500MHz)</td>
<td>+60</td>
<td></td>
</tr>
<tr>
<td>F2258</td>
<td>50 - 6000</td>
<td>1.4 (at 2GHz)</td>
<td>+65</td>
<td>Hittite</td>
</tr>
</tbody>
</table>

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Rev 2, February 9, 2018

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**ABSOLUTE MAXIMUM RATINGS**

<table>
<thead>
<tr>
<th>Parameter / Condition</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$ to GND</td>
<td>$V_{DD}$</td>
<td>-0.3</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>$V_{MODE}$ to GND</td>
<td>$V_{MODE}$</td>
<td>-0.3</td>
<td>Minimum ( $V_{DD}$, 3.9 )</td>
<td>V</td>
</tr>
<tr>
<td>$V_{CTRL}$ to GND</td>
<td>$V_{CTRL}$</td>
<td>-0.3</td>
<td>Minimum ( $V_{DD}$, 4.0 )</td>
<td>V</td>
</tr>
<tr>
<td>RF1, RF2 to GND</td>
<td>$V_{RF}$</td>
<td>-0.3</td>
<td>0.3</td>
<td>V</td>
</tr>
<tr>
<td>RF1 or RF2 Input Power applied for 24 hours maximum</td>
<td>$P_{MAX24}$</td>
<td>30</td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>RF1 or RF2 Continuous Operating Power</td>
<td>$P_{MAX, OP}$</td>
<td>See Figure 1</td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>Maximum Junction Temperature</td>
<td>$T_{JMAX}$</td>
<td>+150</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>$T_{ST}$</td>
<td>-65</td>
<td>+150</td>
<td>°C</td>
</tr>
<tr>
<td>Lead Temperature (soldering, 10s)</td>
<td>$T_{LEAD}$</td>
<td>+260</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>ESD Voltage – HBM (Per ESD STM5.1-2007)</td>
<td>$V_{ESD,HBM}$</td>
<td>Class 2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ESD Voltage – CDM (Per ESD STM5.3.1-2009)</td>
<td>$V_{ESD, CDM}$</td>
<td>Class 3</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**PACKAGE THERMAL AND MOISTURE CHARACTERISTICS**

- $\Theta_{JA}$ (Junction – Ambient) 80.6°C/W
- $\Theta_{JC}$ (Junction – Case) The Case is defined as the exposed paddle 5.1°C/W
- Moisture Sensitivity Rating (Per J-STD-020) MSL 1
# IDTF2255 Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Frequency Range</td>
<td>$F_{RF}$</td>
<td></td>
<td>1</td>
<td></td>
<td>3000 MHz</td>
<td></td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>$V_{DD}$</td>
<td></td>
<td>3.15</td>
<td>5.25</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{MODE}$ Logic</td>
<td>$V_{IH}$</td>
<td>$V_{DD} &gt; 3.9V$</td>
<td>1.17</td>
<td></td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$V_{IL}$</td>
<td>$V_{DD} = 3.15$ to $3.9V$</td>
<td>1.17</td>
<td></td>
<td>$V_{DD} - 0.3V$</td>
<td>V</td>
</tr>
<tr>
<td>Supply Current</td>
<td>$I_{DD}$</td>
<td>$V_{DD} = 3.9V$ to $5.25V$</td>
<td>0</td>
<td></td>
<td>3.6</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 3.15V$ to $3.9V$</td>
<td>0</td>
<td></td>
<td>$V_{DD} - 0.3$</td>
<td>V</td>
</tr>
<tr>
<td>Logic Current</td>
<td>$I_{MODE}$</td>
<td></td>
<td>-1.0</td>
<td></td>
<td>38</td>
<td>μA</td>
</tr>
<tr>
<td>ICTRL Current</td>
<td>$I_{CTRL}$</td>
<td></td>
<td>-1.0</td>
<td></td>
<td>14</td>
<td>μA</td>
</tr>
<tr>
<td>RF Operating Power</td>
<td>$P_{MAXCW}$</td>
<td></td>
<td></td>
<td>See Figure 1</td>
<td>dBm</td>
<td></td>
</tr>
<tr>
<td>RF1 Port Impedance</td>
<td>$Z_{RF1}$</td>
<td></td>
<td>50</td>
<td></td>
<td>50</td>
<td>Ω</td>
</tr>
<tr>
<td>RF2 Port Impedance</td>
<td>$Z_{RF2}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>$T_{CASE}$</td>
<td>Exposed Paddle Temperature</td>
<td>-40</td>
<td></td>
<td>+105</td>
<td>°C</td>
</tr>
</tbody>
</table>

**Operating Conditions Notes:**

1 – Items in min/max columns in **bold italics** are Guaranteed by Test.

2 – Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.

3 – Refer to the Maximum Operating RF Input Power vs. RF Frequency curves in Figure 1.
**IDTF2255 Specifications**

Refer to EVKit / Applications Circuit, \( V_{DD} = +3.3\text{V}, T_c = +25^\circ\text{C} \), signals applied to RF1 input, \( F_{RF} = 500\text{MHz} \), minimum attenuation, \( P_{IN} = 0\text{dBm} \) for small signal parameters, \( +20\text{dBm} \) for single tone linearity tests, \( +20\text{dBm} \) per tone for two tone tests, two tone delta frequency = 80MHz, PCB board traces and connector losses are de-embedded unless otherwise noted. Refer to Typical Operating Curves for performance over entire frequency band.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Insertion Loss, IL</td>
<td>( A_{MIN} )</td>
<td>Minimum Attenuation</td>
<td>1.1</td>
<td>1.7(^1)</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Maximum attenuation</td>
<td>( A_{MAX} )</td>
<td></td>
<td>33</td>
<td>34.6</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Insertion Phase ( \Delta )</td>
<td>( \Phi_{\text{MAX}} )</td>
<td>At 36dB attenuation relative to Insertion Loss</td>
<td>27</td>
<td>deg</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( \Phi_{\text{MID}} )</td>
<td>At 18dB attenuation relative to Insertion Loss</td>
<td>8</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input 1dB Compression (^3)</td>
<td>( P_{1dB} )</td>
<td></td>
<td>36</td>
<td>dBm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Minimum RF1 Return Loss over control voltage range</td>
<td>( S_{11} )</td>
<td>20MHz</td>
<td>23</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>500MHz</td>
<td>22</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>2000MHz</td>
<td>23</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3000MHz</td>
<td>30</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Minimum RF2 Return Loss over control voltage range</td>
<td>( S_{22} )</td>
<td>20MHz</td>
<td>23</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>500MHz</td>
<td>22</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>2000MHz</td>
<td>23</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3000MHz</td>
<td>24</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input IP3</td>
<td>( I_{IP3} )</td>
<td></td>
<td>60</td>
<td>dBm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input IP3 over Attenuation</td>
<td>( I_{IP3\text{ATTEN}} )</td>
<td>All attenuation settings</td>
<td>44(^2)</td>
<td>46</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Minimum Output IP3</td>
<td>( O_{IP3\text{MIN}} )</td>
<td>Maximum attenuation</td>
<td>35</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input IP2</td>
<td>( I_{IP2} )</td>
<td>( \text{PIN} + \text{IM2}_{\text{DBC}}, \text{IM2 term is F1+F2} )</td>
<td>98</td>
<td>dBm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Minimum Input IP2</td>
<td>( I_{IP2\text{MIN}} )</td>
<td>All attenuation settings</td>
<td>74</td>
<td>dBm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input IH2</td>
<td>( H_{D2} )</td>
<td>( \text{PIN} + H_{2\text{DBC}} )</td>
<td>82</td>
<td>dBm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input IH3</td>
<td>( H_{D3} )</td>
<td>( \text{PIN} + (H_{3\text{DBC}}/2) )</td>
<td>49</td>
<td>dBm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Settling Time</td>
<td>( T_{\text{SETTL0.1dB}} )</td>
<td>Any 1dB step in the 0dB to 33dB control range 50% ( V_{CTRL} ) to RF settled to within ( \pm 0.1\text{dB} )</td>
<td>15</td>
<td>( \mu\text{Sec} )</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Specification Notes:**
1 – Items in min/max columns in **bold italics** are Guaranteed by Test.
2 – Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
3 – The input 1dB compression point is a linearity figure of merit. Refer to Absolute Maximum Ratings section along with Figure 1 for the maximum RF input power vs. RF frequency.
TYPICAL OPERATING CURVES

UNLESS OTHERWISE NOTED, THE FOLLOWING CONDITIONS APPLY:

- \( V_{DD} = +3.3\text{V} \) or \(+5.0\text{V}\)
- \( T_C = +25^\circ \text{C}\)
- \( V_{MODE} = 0\text{V}\)
- RF trace and connector losses are de-embedded for S-parameters
- Pin = 0dBm for all small signal tests
- Pin = +20dBm for single tone linearity tests (RF1 port driven)
- Pin = +20dBm/tone for two tone linearity tests (RF1 port driven)
- Two tone frequency spacing = 80MHz
TYPICAL OPERATING CONDITIONS [S2P BROADBAND PERFORMANCE] (-1-)

Attenuation vs. VCTRL

Attenuation vs. Frequency

Attenuation Delta to 25C vs. VCTRL
**TYPICAL OPERATING CURVES [S2P vs. V_CTRL] (-2-)**

**Attenuation vs. V_CTRL**

25C

**Attenuation Slope vs. V_CTRL**

25C

**RF1 Return Loss vs. V_CTRL**

25C

**RF2 Return Loss vs. V_CTRL**

25C

**Insertion Phase ∆ vs. V_CTRL**

(positive phase = electrically shorter)

25C

**Insertion Phase Slope vs. V_CTRL**

25C
Typical Operating Conditions [S2P vs. $V_{\text{CTRL}}$ & Temperature] (-3-)

Attenuation Response vs. $V_{\text{CTRL}}$

RF1 Return Loss vs. $V_{\text{CTRL}}$

Insertion Phase $\Delta$ vs. $V_{\text{CTRL}}$

Attenuation Slope vs. $V_{\text{CTRL}}$

RF2 Return Loss vs. $V_{\text{CTRL}}$

Insertion Phase Slope vs. $V_{\text{CTRL}}$
TYPICAL OPERATING CONDITIONS [S2P vs. ATTENUATION & TEMPERATURE] (-4-)

RF1 Return Loss vs. Attenuation

RF2 Return Loss vs. Attenuation

Insertion Phase $\Delta$ vs. Attenuation

RF1 Return Loss vs. Attenuation

RF2 Return Loss vs. Attenuation

Insertion Phase $\Delta$ vs. Attenuation

(positive phase = electrically shorter)
Typical Operating Conditions [S2P vs. Frequency] (-5-)

Min. & Max. Attenuation vs. Frequency

Min. & Max. Attenuation Slope vs. Frequency

Worst-Case RF1 Return Loss vs. Frequency

Worst-Case RF2 Return Loss vs. Frequency

Max. Insertion Phase $\Delta$ vs. Frequency

Gain Compression vs. Frequency

VCTRL varied from 0.8V to 1.7V

VCTRL varied from 0.8V to 1.7V

Min/Max ATTN slope (dB/V)

Gain Compression (dB)

RF Input Power (dBm)
Typical Operating Conditions [S2P @ Low Frequency, Group Delay] (-6-)

Min. & Max. Attenuation vs. Low Frequency

Low-Frequency Attenuation vs. VCTRL

Low-Frequency RF1 Return Loss vs. VCTRL

Low-Frequency RF2 Return Loss vs. VCTRL

Group Delay vs. Frequency
**Typical Operating Conditions** 500MHz, \( V_{DD} = 3.3V \) [IP3, IP2, IH2, IH3 vs. \( V_{CTRL}, V_{MODE} \)] (-7-)

**Input IP3 vs. \( V_{CTRL} \)**

**Output IP3 vs. \( V_{CTRL} \)**

**Input IP2 vs. \( V_{CTRL} \)**

**Output IP2 vs. \( V_{CTRL} \)**

**2\(^{nd}\) Harm Input Intercept Point vs. \( V_{CTRL} \)**

**3\(^{rd}\) Harm Input Intercept Point vs. \( V_{CTRL} \)**
TYPICAL OPERATING CONDITIONS 500MHz, $V_{DD}=3.3V$ [IPX, IHX vs. $V_{CTRL}$, RF1/RF2 Driven] (-8-)
Typical Operating Conditions 500MHz, VDD=3.3V [IP3, IP2, IH2, IH3 vs. Attenuation] (-9-)

Input IP3 vs. Attenuation

Output IP3 vs. Attenuation

Input IP2 vs. Attenuation

Output IP2 vs. Attenuation

2nd Harm Input Intercept Point vs. Attenuation

3rd Harm Input Intercept Point vs. Attenuation
**Typical Operating Conditions** 500MHz, \( V_{\text{DD}} = 3.3\text{V} \) [IPx, IHx vs. ATTEN, RF1/RF2 Driven] (-10-)

**Input IP3 vs. Attenuation**

**Output IP3 vs. Attenuation**

**Input IP2 vs. Attenuation**

**Output IP2 vs. Attenuation**

**2nd Harm Input Intercept Point vs. Attenuation**

**3rd Harm Input Intercept Point vs. Attenuation**
PACKAGE DRAWING (3MM x 3MM 16 PIN)

16-VFQFPN Package Outline Drawing
3.0 x 3.0 x 0.9 mm, 0.5mm Pitch, 1.70 x 1.70 mm Epack
NL/NLG16P2, PSC-4169-02, Rev 05, Page 1

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES

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LAND PATTERN DRAWING

16-VFQFPN Package Outline Drawing
3.0 x 3.0 x 0.9 mm, 0.5mm Pitch, 1.70 x 1.70 mm Epad
NL/NLG16F2, PSC-4169-02, Rev 05, Page 2

RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES
2. TOP DOWN VIEW—AS VIEWED ON PCB
3. LAND PATTERN RECOMMENDATION IS PER IPC-7351B GENERIC
   REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN

Package Revision History

<table>
<thead>
<tr>
<th>Date Created</th>
<th>Rev No</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oct 25, 2017</td>
<td>Rev 04</td>
<td>Remove Bookmark at Pdf Format &amp; Update Thickness Tolerance</td>
</tr>
<tr>
<td>Jan 18, 2018</td>
<td>Rev 05</td>
<td>Change QFN to VFQFPN</td>
</tr>
</tbody>
</table>
PINOUT & BLOCK DIAGRAM

- **V_mode**: 16
- **V_d0**: 15
- **V_CTRL**: 14
- **NC**: 13
- **GND**: Connections 1, 2, 4
- **RF1**: Connections 3, 5, 9
- **RF2**: Connections 10, 11, 12, 14
- **Control**
- **E.P.**
## Pin Description

<table>
<thead>
<tr>
<th>Pin</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1, 7, 12</td>
<td>GND</td>
<td>Ground these pins as close to the device as possible.</td>
</tr>
<tr>
<td>2, 4, 9, 11, 13</td>
<td>NC</td>
<td>No internal connection. IDT recommends connecting these pins to GND.</td>
</tr>
<tr>
<td>3</td>
<td>RF1</td>
<td>RF Port 1. Matched to 50 ohms. Must use an external AC coupling capacitor as close to the device as possible. For low frequency operation increase the capacitor value to result in a low reactance at the frequency of interest.</td>
</tr>
<tr>
<td>5, 6, 8</td>
<td>RTN</td>
<td>Attenuator Ground Return. Each of these pins require a capacitor to GND to provide an RF return path. Place the capacitor as close to the device as possible.</td>
</tr>
<tr>
<td>10</td>
<td>RF2</td>
<td>RF Port 2. Matched to 50 ohms. Must use an external AC coupling capacitor as close to the device as possible. For low frequency operation increase the capacitor value to result in a low reactance at the frequency of interest.</td>
</tr>
<tr>
<td>14</td>
<td>$V_{\text{CTRL}}$</td>
<td>Attenuator control voltage. Apply a voltage in the range as specified in the Operating Conditions Table. See application section for details about $V_{\text{CTRL}}$.</td>
</tr>
<tr>
<td>15</td>
<td>$V_{\text{DD}}$</td>
<td>Power supply input. Bypass to GND with capacitors close as possible to pin.</td>
</tr>
<tr>
<td>16</td>
<td>$V_{\text{MODE}}$</td>
<td>Attenuator slope control. Set to logic LOW to enable negative attenuation slope. Set to logic HIGH to enable positive attenuation slope.</td>
</tr>
<tr>
<td></td>
<td>— EP</td>
<td>Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to achieve the specified RF performance.</td>
</tr>
</tbody>
</table>
**APPLICATIONS INFORMATION**

**Default Start-up**

$V_{MODE}$ must be tied to either GND or Logic High. If the $V_{CTRL}$ pin is left floating, the part will power up in the minimum attenuation state when $V_{MODE} = \text{GND}$, or the maximum attenuation state when $V_{MODE} = \text{High}$.

$V_{CTRL}$

The voltage level on the $V_{CTRL}$ pin is used to control the attenuation of the F2255. At $V_{CTRL} = 0\text{V}$, the attenuation is a minimum (maximum) in the negative (positive) slope mode. An increasing (decreasing) voltage on $V_{CTRL}$ produces an increasing (decreasing) attenuation respectively. The $V_{CTRL}$ pin has an on-chip pull-up ESD diode so $V_{DD}$ should be applied before $V_{CTRL}$ is applied (see Recommended Operating Conditions for details). If this sequencing is not possible, then resistor R2 in the application circuit should be set to 1kΩ to limit the current into the $V_{CTRL}$ pin.

$V_{MODE}$

The $V_{MODE}$ pin is used to set the slope of the attenuation. The attenuation is varied by $V_{CTRL}$ as described in the next section. Setting $V_{MODE}$ to a logic LOW (HIGH) will set the attenuation slope to negative (positive). A negative (positive) slope is defined as an increased (decreased) attenuation with increasing $V_{CTRL}$ voltage. The Evaluation Kit provides an on-board jumper to manually set the $V_{MODE}$. Install a jumper on header J2 from $V_{MODE}$ to the pin marked Lo (Hi) to set the device for a negative (positive) slope (see application circuit).

**RF1 and RF2 Ports**

The F2255 is a bi-directional device, allowing RF1 or RF2 to be used as the RF input. RF1 has some enhanced linearity performance, and therefore should be used as the RF input, when possible, for best results. The F2255 has been designed to accept high RF input power levels; therefore, $V_{DD}$ must be applied prior to the application of RF power to ensure reliability. DC blocking capacitors are required on the RF pins and should be set to a value that results in a low reactance over the frequency range of interest.

**Power Supplies**

The supply pin should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V/20uS. In addition, all control pins should remain at 0V (+/-0.3V) while the supply voltage ramps or while it returns to zero.
Control Pin Interface

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of control pins 14 and 16 is recommended as shown below.
Short GND pin to VMODE pin to set for negative attenuation slope. For positive attenuation slope move shorting shunt from VMODE to VHI
EVKIT PICTURE / LAYOUT (BOTTOM VIEW)
## EVkit BOM

<table>
<thead>
<tr>
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<tbody>
<tr>
<td>C1, C4, C5</td>
<td>3</td>
<td>10nF ±5%, 50V, X7R Ceramic Capacitors (0805)</td>
<td>RM188R71H103J</td>
<td>Murata</td>
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<td>C7, C8, C9, C10, C11</td>
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<td>100nF ±10%, 16V, X7R Ceramic Capacitors (0402)</td>
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<td>R1, R2, R5</td>
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<td>Panasonic</td>
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<td>Panasonic</td>
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<tr>
<td>J1, J3, J4, J5</td>
<td>4</td>
<td>Edge Launch SMA (0.375 inch pitch ground tabs)</td>
<td>142-0701-051</td>
<td>Emerson Johnson</td>
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<tr>
<td>J2</td>
<td>1</td>
<td>CONN HEADER VERT SGL 3 X 1 POS GOLD</td>
<td>961103-6404-AR</td>
<td>3M</td>
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<tr>
<td>U1</td>
<td>1</td>
<td>Voltage Variable Attenuator</td>
<td>F2255NLGK</td>
<td>IDT</td>
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<tr>
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<td>Printed Circuit Board</td>
<td>F2255 REV 1</td>
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### Top Markings

- **Date Code [YWW]** (Week 46 of 2014)
- **Lot Code**
- **Assembler Code**
- **Part Number**
### Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>Revision Date</th>
<th>Description of Change</th>
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<tbody>
<tr>
<td>2</td>
<td>February 9, 2018</td>
<td>Corrected POD drawing, added revision page</td>
</tr>
<tr>
<td>1</td>
<td>January 30, 2017</td>
<td>Updated GBT limits for $I_{DD}$, $V_{MODE}$ and $V_{CTRL}$</td>
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<tr>
<td>0</td>
<td>November 5, 2015</td>
<td>Initial Release</td>
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