

### General Description

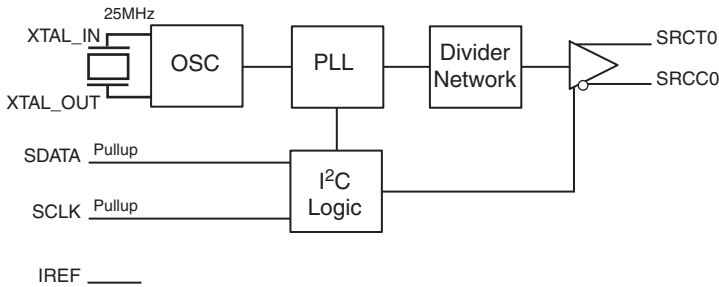
The 841S01 is a PLL-based clock generator specifically designed for PCI\_Express™ Clock Generation applications. This device generates a 100MHz HCSL clock. The device offers a HCSL (Host Clock Signal Level) clock output from a clock input reference of 25MHz. The input reference may be derived from an external source or by the addition of a 25MHz crystal to the on-chip crystal oscillator. An external reference may be applied to the XTAL\_IN pin with the XTAL\_OUT pin left floating.

The device offers spread spectrum clock output for reduced EMI applications. An I<sup>2</sup>C bus interface is used to enable or disable spread spectrum operation as well as select either a down spread value of -0.35% or -0.5%.

### Features

- One 0.7V current mode differential HCSL output pair
- Crystal oscillator interface: 25MHz
- Output frequency: 100MHz
- RMS period jitter: 3ps (maximum)
- Cycle-to-cycle jitter: 35ps (maximum)
- I<sup>2</sup>C support with readback capabilities up to 400kHz
- Spread Spectrum for electromagnetic interference (EMI) reduction
- 3.3V operating supply mode
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package

### Block Diagram



### Pin Assignment

V <sub>SS</sub>	1	16	V <sub>DD</sub>
V <sub>DD</sub>	2	15	SDATA
SRCT0	3	14	SCLK
SRCC0	4	13	XTAL_OUT
V <sub>DD</sub>	5	12	XTAL_IN
V <sub>SS</sub>	6	11	V <sub>DD</sub>
IREF	7	10	V <sub>SS</sub>
V <sub>SS</sub>	8	9	V <sub>DDA</sub>

**841S01**  
**16-Lead TSSOP**  
**5mm x 4.4mm x 0.925mm package body**  
**G Package**  
**Top View**

**Table 1. Pin Descriptions**

Number	Name	Type		Description
1, 6, 8, 10	V <sub>SS</sub>	Power		Ground for core and SRC outputs.
2, 5, 11, 16	V <sub>DD</sub>	Power		Power supply for core and SRC outputs.
3, 4	SRCT0, SRCC0	Output		Differential output pair. HCSL interface levels.
7	IREF	Input		An external fixed precision resistor (475Ω) from this pin to ground provides a reference current used for differential current-mode SRCCx, SRCTx clock outputs.
9	V <sub>DDA</sub>	Power		Analog supply pin.
12, 13	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
14	SCLK	Input	Pullup	I <sup>2</sup> C SMBus compatible SCLK. This pin has an internal pullup resistor, but is in high-impedance in power-down mode. LVCMOS/LVTTL interface levels.
15	SDATA	I/O	Pullup	I <sup>2</sup> C SMBus compatible SDATA. This pin has an internal pullup resistor, but is in high-impedance in power-down mode. LVCMOS/LVTTL interface levels.

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ

## Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default

setting upon power-up, and therefore, use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface cannot be used during system operation for power management functions.

## Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually

indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 3A*.

The block write and block read protocol is outlined in *Table 3B*, while *Table 3C* outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

**Table 3A. Command Code Definition**

Bit	Description
7	0 = Block read or block write operation, 1 = Byte read or byte write operation.
6:5	Chip select address, set to "00" to access device.
4:0	Byte offset for byte read or byte write operation. For block read or block write operations, these bits must be "0000".

**Table 3B. Block Read and Block Write Protocol**

Bit	Description = Block Write	Bit	Description = Block Read
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 bits	11:18	Command Code - 8 bits
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29:36	Data byte 1 - 8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 2 - 8 bits	30:37	Byte Count from slave - 8 bits
46	Acknowledge from slave	38	Acknowledge
	Data Byte/Slave Acknowledges	39:46	Data Byte 1 from slave - 8 bits
	Data Byte N - 8 bits	47	Acknowledge
	Acknowledge from slave	48:55	Data Byte 2 from slave - 8 bits
	Stop	56	Acknowledge
			Data Bytes from Slave/Acknowledge
			Data Byte N from slave - 8 bits
			Not Acknowledge

**Table 3C. Byte Read and Byte Write Protocol**

Bit	Description = Byte Write	Bit	Description = Byte Read
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 bits	11:18	Command Code - 8 bits
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data Byte- 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		30:37	Data from slave - 8 bits
		38	Not Acknowledge
		39	Stop

## Control Registers

**Table 4A. Byte 0: Control Register 0**

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	1	Reserved	Reserved
5	1	Reserved	Reserved
4	1	Reserved	Reserved
3	1	Reserved	Reserved
2	1	SRC[T/C]0	SRC[T/C]0 Output Enable 0 = Disable (Hi-Z) 1 = Enable
1	0	Reserved	Reserved
0	0	Reserved	Reserved

NOTE: Pup denotes Power-up.

**Table 4B. Byte 1: Control Register 1**

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	0	Reserved	Reserved
0	0	Reserved	Reserved

**Table 4C. Byte 2: Control Register 2**

Bit	@Pup	Name	Description
7	1	SRCT/C	Spread Spectrum Selection 0 = -0.35%, 1 = - 0.5%
6	1	Reserved	Reserved
5	1	Reserved	Reserved
4	0	Reserved	Reserved
3	1	Reserved	Reserved
2	0	SRC	SRC Spread Spectrum Enable 0 = Spread Off, 1 = Spread On
1	1	Reserved	Reserved
0	0	Reserved	Reserved

**Table 4D. Byte 3: Control Register 3**

Bit	@Pup	Name	Description
7	1	Reserved	Reserved
6	0	Reserved	Reserved
5	1	Reserved	Reserved
4	0	Reserved	Reserved
3	1	Reserved	Reserved
2	1	Reserved	Reserved
1	1	Reserved	Reserved
0	1	Reserved	Reserved

NOTE: Pup denotes Power-up.

**Table 4E. Byte 4: Control Register 4**

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	0	Reserved	Reserved
0	1	Reserved	Reserved

**Table 4F. Byte 5: Control Register 5**

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	0	Reserved	Reserved
0	0	Reserved	Reserved

**Table 4G. Byte 6: Control Register 6**

Bit	@Pup	Name	Description
7	0	TEST_SEL	REF/N or Hi-Z Select 0 = Hi-Z, 1 = REF/N
6	0	TEST_MODE	TEST Clock Mode Entry Control 0 = Normal Operation, 1 = REF/N or Hi-Z Mode
5	0	Reserved	Reserved
4	1	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	1	Reserved	Reserved
0	1	Reserved	Reserved

**Table 4H. Byte 7: Control Register 7**

Bit	@Pup	Name	Description
7	0		Revision Code Bit 3
6	0		Revision Code Bit 2
5	0		Revision Code Bit 1
4	0		Revision Code Bit 0
3	0		Vendor ID Bit 3
2	0		Vendor ID Bit 2
1	0		Vendor ID Bit 1
0	1		Vendor ID Bit 0

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$ XTAL_IN Other Inputs	0V to $V_{DD}$ -0.5V to $V_{DD} + 0.5V$
Outputs, $V_O$	-0.5V to $V_{DD} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$	86.9°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

Table 5A. Power Supply DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDA}$	Analog Supply Voltage		$V_{DD} - 0.22$	3.3	$V_{DD}$	V
$I_{DD}$	Power Supply Current				80	mA
$I_{DDA}$	Analog Supply Current				22	mA

Table 5B. LVCMOS/LVTTL DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		2.2			V
$V_{IL}$	Input Low Voltage				1.0	V
$I_{IH}$	Input High Current	SDATA, SCLK $V_{DD} = V_{IN} = 3.465V$			10	$\mu A$
$I_{IL}$	Input Low Current	SDATA, SCLK $V_{DD} = 3.465V, V_{IN} = 0V$	-150			$\mu A$

## AC Electrical Characteristics

Table 6. AC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{ref}$	Frequency			25		MHz
SCLK	SCLK Frequency				400	kHz
	Frequency Tolerance; NOTE 1	XTAL			50	ppm
		External Reference			0	ppm
odc	SRCT/SRCC Output Duty Cycle; NOTE 2, 3		47		53	%
$t_{PERIOD}$	Average Period; NOTE 4		9.9970		10.0533	ns
$f_{jit(cc)}$	SRCT/C Cycle-to-Cycle Jitter; NOTE 2, 3				35	ps
$f_{jit(per)}$	Period Jitter, RMS; NOTE 2, 3, 5			2.42	3	ps
$t_R / t_F$	SRCT/SRCC Rise/Fall Time; NOTE 6		150		700	ps
$t_{RFM}$	Rise/Fall Time Matching; NOTE 7				20	%
$t_{DC}$	XTAL_IN Duty Cycle; NOTE 8		47.5		52.5	%
$\Delta t_R / t_F$	Rise/Fall Time Variation				145	ps
$V_{HIGH}$	Voltage High		520		875	mV
$V_{LOW}$	Voltage Low		-150			mV
$V_{OX}$	Output Crossover Voltage	@ 0.7V Swing	250		550	mV
$V_{OVS}$	Maximum Overshoot Voltage				$V_{HIGH} + 0.3$	V
$V_{UDS}$	Minimum Undershoot Voltage		-0.3			V
$V_{RB}$	Ring Back Voltage				0.2	V

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: With recommended crystal.

NOTE 2: Measured at crossing point  $V_{OX}$ .

NOTE 3: Measured using a 50 $\Omega$  to GND termination.

NOTE 4: Measured at crossing point  $V_{OX}$  at 100MHz.

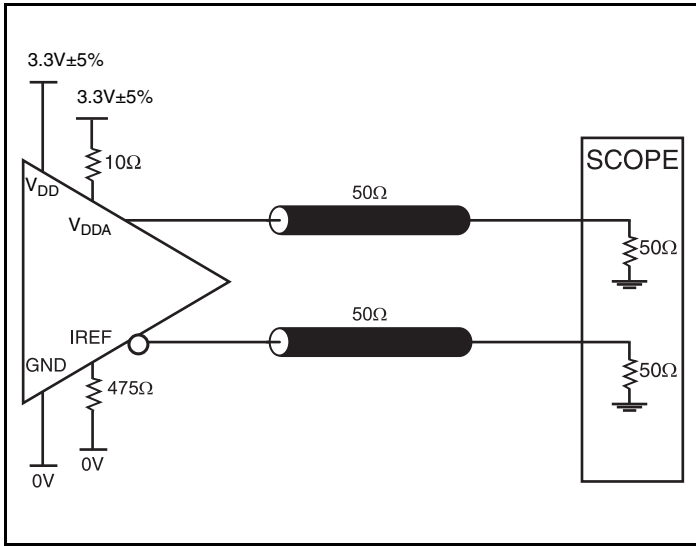
NOTE 5: If using the RMS period jitter to calculate peak-to-peak jitter, then use the typical RMS period jitter specification times the RMS multiplier. For example, for a bit error rate of 10E-12, the peak-to-peak jitter would be 2.42ps x 14 = 33.88ps.

NOTE 6: Measured from  $V_{OL} = 0.175V$  to  $V_{OH} = 0.525V$ .

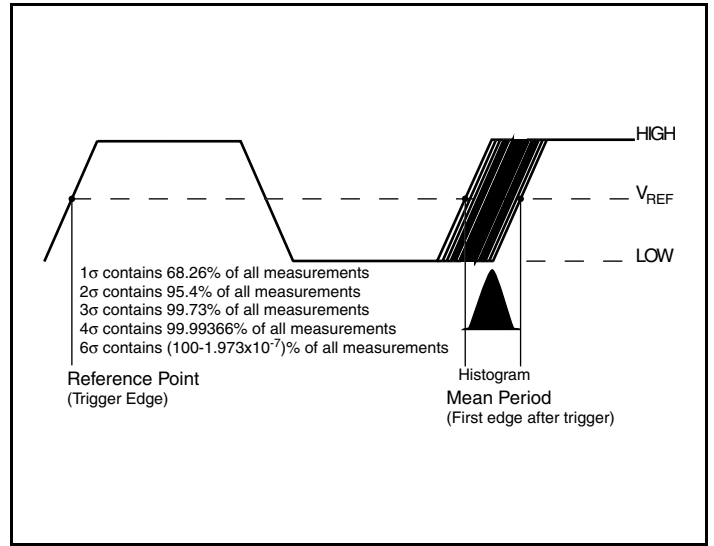
NOTE 7: Determined as a fraction of  $2 \cdot (t_R - t_F) / (t_R + t_F)$ .

NOTE 8: The device will operate reliably with input duty cycles up to 30/70% but the REF clock duty cycle will not be within specification.

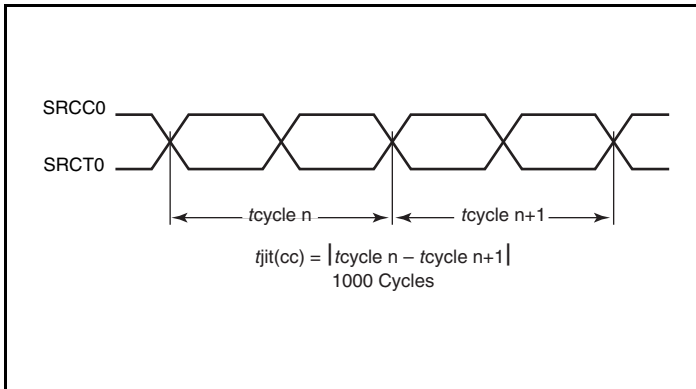
### Parameter Measurement Information



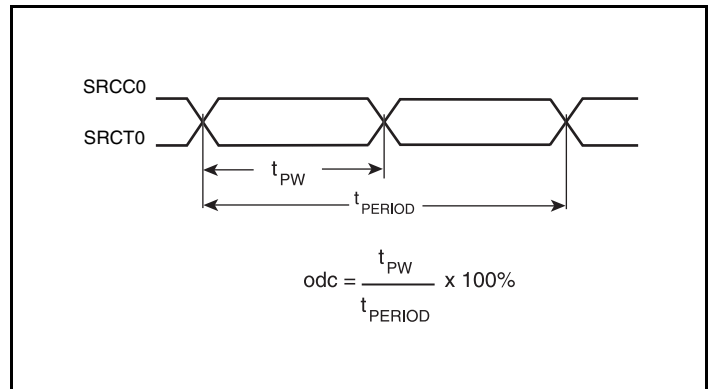
3.3V HCSL Output Load AC Test Circuit



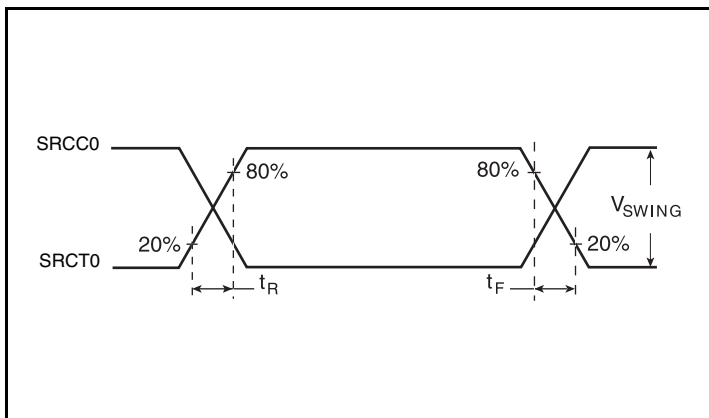
RMS Period Jitter



Cycle-to-Cycle Jitter



Output Duty Cycle/Pulse Width/Period



HCSL Output Rise/Fall Time



## Applications Information

### Recommendations for Unused Input Pins

#### Inputs:

##### LVC MOS Control Pins

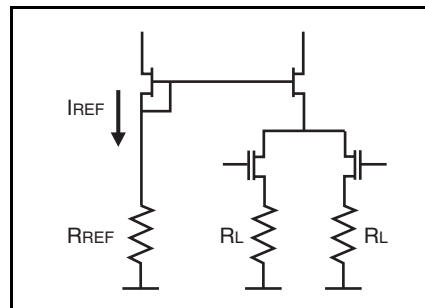
All control pins have internal pullups; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

**Table 7. Recommended Crystal Specifications**

Symbol	Parameter	Value
	Crystal Cut	Fundamental at Cut
	Resonance	Parallel Resonance
$C_L$	Load Capacitance	18pF
$C_O$	Shunt Capacitance	5pF - 7pF
ESR	Equivalent Series Resistance	20 $\Omega$ - 50 $\Omega$

### Output Driver Current

The 841S01 outputs are HCSL current drive with the current being set with a resistor from  $I_{REF}$  to ground. For a 50 $\Omega$  pc board trace, the drive current would typically be set with a  $R_{REF}$  of 475 $\Omega$  which produces an  $I_{REF}$  of 2.32mA. The  $I_{REF}$  is multiplied by a current mirror to an output drive of 6\*2.32mA or 13.92mA. See *Figure 1* for current mirror and output drive details.



**Figure 1. HCSL Current Mirror and Output Drive**

### Recommended Termination

Figure 2A is the recommended source termination for applications where the driver and receiver will be on a separate PCBs. This termination is the standard for PCI Express™ and HCSL output types.

All traces should be 50Ω impedance single-ended or 100Ω differential.

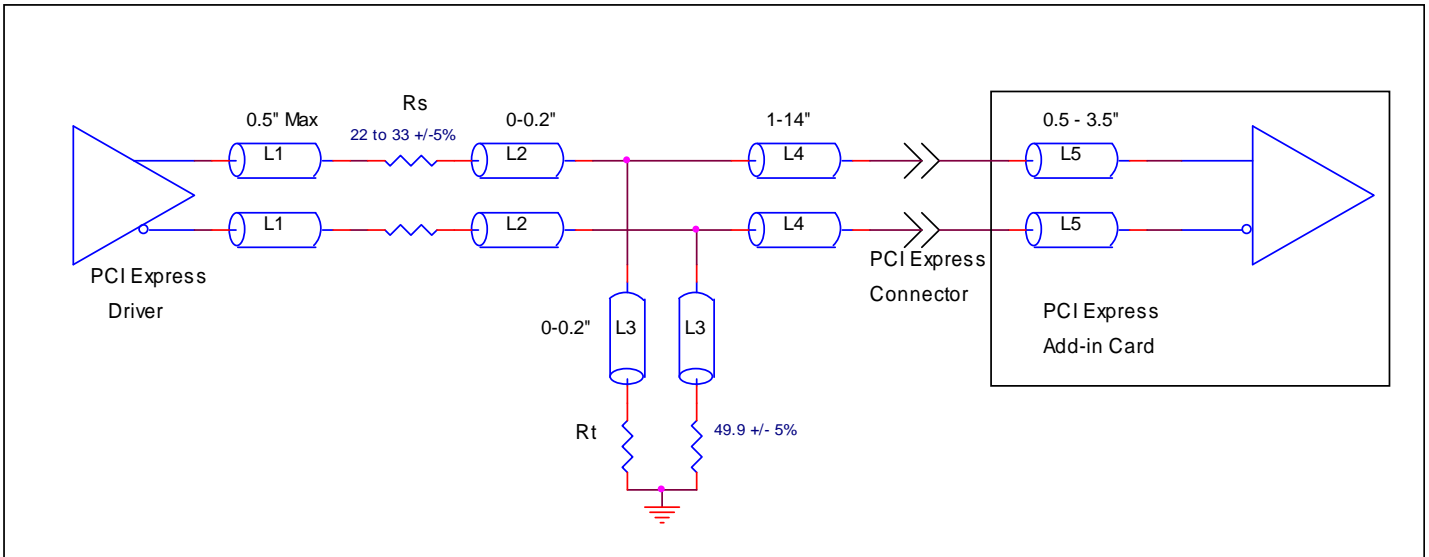


Figure 2A. Recommended Source Termination (where the driver and receiver will be on separate PCBs)

Figure 2B is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will

be minimized. In addition, a series resistor (Rs) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single-ended or 100Ω differential.

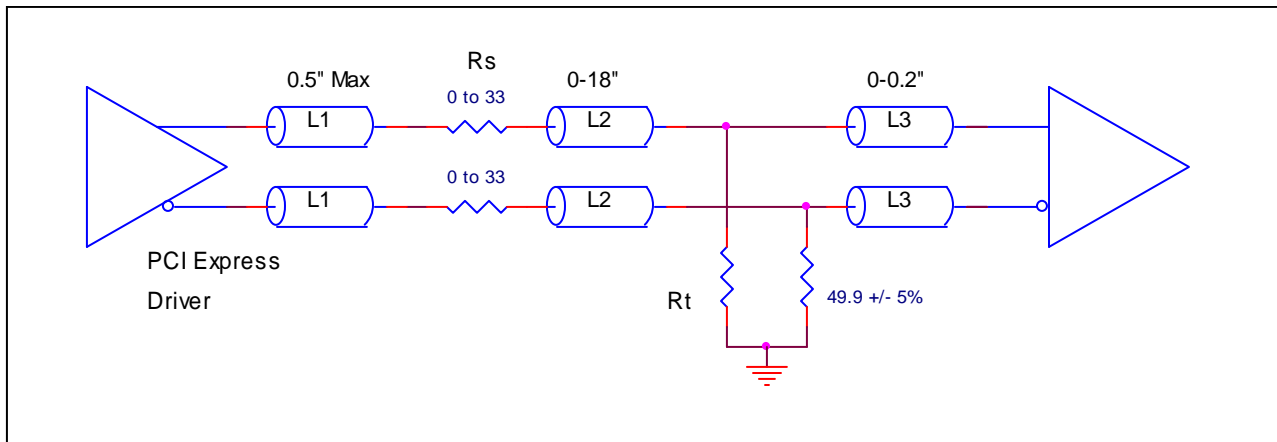


Figure 2B. Recommended Termination (where a point-to-point connection can be used)

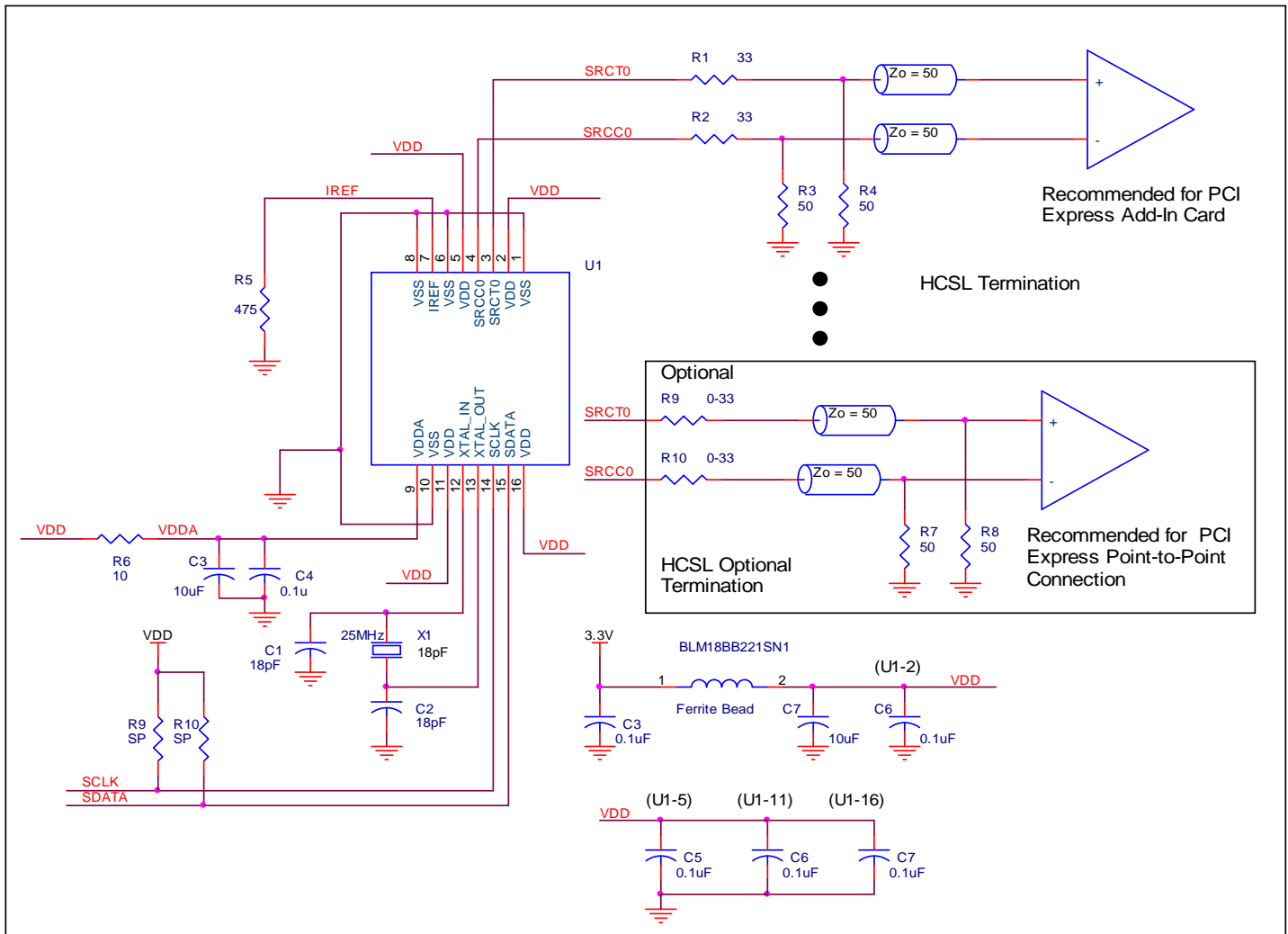
## Schematic Layout

Figure 3 shows an example of 841S01 application schematic. In this example, the device is operated at  $V_{DD} = 3.3V$ . The 18pF parallel resonant 25MHz crystal is used. The load capacitance  $C1 = 18pF$  and  $C2 = 18pF$  is recommended for frequency accuracy. Depending on the parasitic of the printed circuit board layout, these values might require a slight adjustment for optimize the frequency accuracy. For this device, the crystal load capacitors are required for proper operation.

As with any high speed analog circuitry, the power supply pins are vulnerable to noise. To achieve optimum jitter performance, power

supply isolation is required. The 841S01 provides separate power supplies to isolate noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uF capacitor in each power pin filter should be placed on the device side of the PCB and the other components can be placed on the opposite side.



**Figure 3. 841S01 Application Schematic**

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supply frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally,

good general design practices for power plane voltage stability suggests adding bulk capacitances in the local area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set.

## Power Considerations

This section provides information on power dissipation and junction temperature for the 841S01. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 841S01 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

The maximum current at 70°C is as follows:

$$I_{DD\_MAX} = 75mA$$

$$I_{DDA\_MAX} = 20mA$$

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX}) = 3.465V * (75mA + 20mA) = 329.175mW$
- Power (outputs)<sub>MAX</sub> = **44.5mW/Loaded Output pair**

$$\text{Total Power}_{MAX} = 329.175mW + 44.5mW = 373.675mW$$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 86.9°C/W per Table 8 below.

Therefore,  $T_j$  for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ C + 0.374W * 86.9^\circ C/W = 102.5^\circ C. \text{ This is below the limit of } 125^\circ C.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

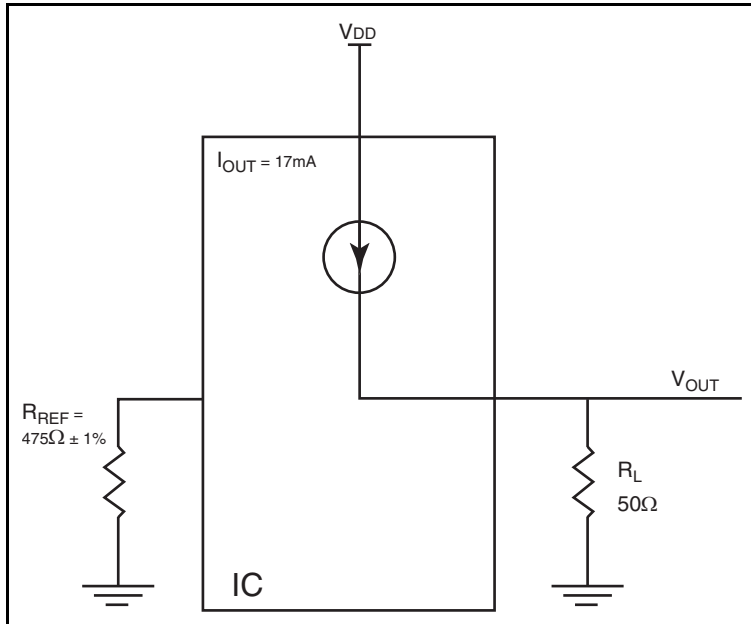
**Table 8. Thermal Resistance  $\theta_{JA}$  for 16 Lead TSSOP, Forced Convection**

$\theta_{JA}$ vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	86.9°C/W	82.5°C/W	80.4°C/W

### 3. Calculations and Equations.

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in *Figure 4*.



**Figure 4. HCSL Driver Circuit and Termination**

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs when  $V_{DD\_MAX}$ .

$$\text{Power} = (V_{DD\_MAX} - V_{OUT}) * I_{OUT}$$

$$\text{since } V_{OUT} = I_{OUT} * R_L$$

$$= (V_{DD\_MAX} - I_{OUT} * R_L) * I_{OUT}$$

$$= (3.465V - 17mA * 50\Omega) * 17mA$$

Total Power Dissipation per output pair = **44.5mW**

## Reliability Information

Table 9.  $\theta_{JA}$  vs. Air Flow Table for a 16 Lead TSSOP

$\theta_{JA}$ vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	86.9°C/W	82.5°C/W	80.4°C/W

## Transistor Count

The transistor count for 841S01 is: 1874

## Package Outline and Package Dimensions

Package Outline - G Suffix for 16 Lead TSSOP

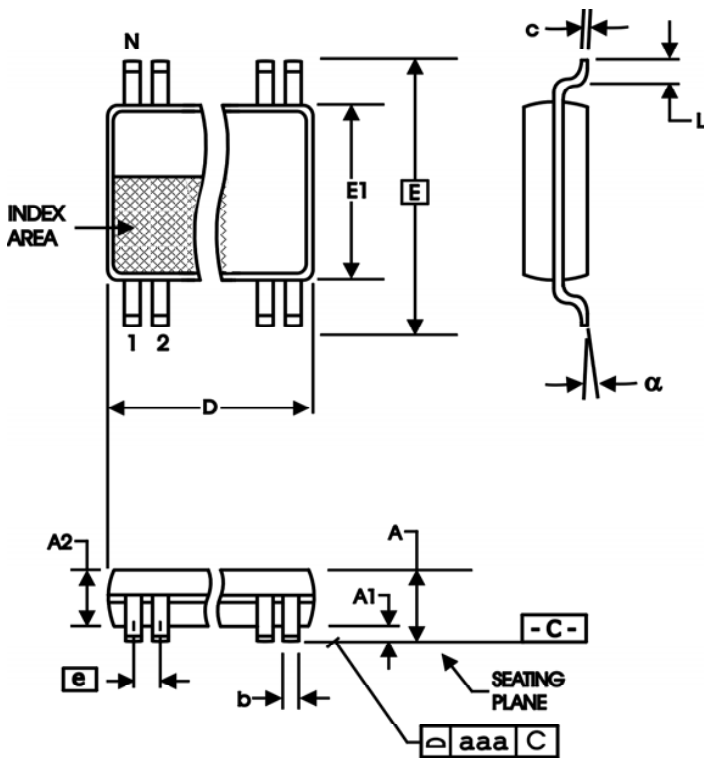


Table 10. Package Dimensions

All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	16	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
$\alpha$	0°	8°
aaa	0.10	

Reference Document: JEDEC Publication 95, MO-153

## Ordering Information

Table 11. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
841S01CGLF	841S01CL	"Lead-Free" 16 Lead TSSOP	Tube	0°C to 70°C
841S01CGLFT	841S01CL	"Lead-Free" 16 Lead TSSOP	2500 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

## Revision History Sheet

Rev	Table	Page	Description of Change	Date
B	T4A	4	Corrected Control Register Table.	8/31/12
B	T11	15	Ordering Information - removed leaded devices. Updated data sheet format.	11/16/15





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