General Description

The 849S625 is a high frequency clock generator. The 849S625 uses an external 25MHz crystal to synthesize 625MHz, 312.5MHz, 156.25MHz and 125MHz clocks. The 849S625 has excellent cycle-to-cycle and RMS phase jitter performance.

The 849S625 operates at full 3.3V supply mode and is available in a fully RoHS compliant 48-lead TQFP, E-Pad package.

Features

- Ten selectable differential LVPECL or LVDS outputs
- Output frequencies of 625MHz, 312.5MHz, 156.25MHz or 125MHz using a 25MHz crystal.
- Crystal interface designed for a 25MHz, parallel resonant crystal
- Cycle-to-cycle jitter: 25ps (maximum)
- RMS phase jitter at 156.25MHz (1MHz - 20MHz): 0.375ps (typical), LVDS outputs
- Output duty cycle: 53% (maximum)
- Full 3.3V supply mode
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) packaging

Frequency Table for Bank A, B and C Outputs

<table>
<thead>
<tr>
<th>Crystal Frequency (MHz)</th>
<th>M Feedback Divider</th>
<th>VCO Frequency (MHz)</th>
<th>Nx Output Divider</th>
<th>Output Frequency (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>25</td>
<td>625</td>
<td>1</td>
<td>625</td>
</tr>
<tr>
<td>25</td>
<td>25</td>
<td>625</td>
<td>2</td>
<td>312.5</td>
</tr>
<tr>
<td>25</td>
<td>25</td>
<td>625</td>
<td>4</td>
<td>156.25</td>
</tr>
<tr>
<td>25</td>
<td>25</td>
<td>625</td>
<td>5</td>
<td>125</td>
</tr>
</tbody>
</table>

Pin Assignment

ICS849S625I

48 Lead TQFP, E-Pad
7mm x 7mm x 1.0mm package body
Y Package
Top View
Block Diagram

- SEL_OUT
- OEA
- SELA[1:0]
- BYPASS
- REF_CLK
- XTAL_IN 25MHz
- XTAL_OUT
- MR
- OEB
- SELB[0:1]
- SELC[0:1]
- OEC
- Pulldown
- Pullup
- Pulldown
- Pulldown
- Pulldown
- Pulldown
- Pulldown
- Pulldown
- Pulldown
- Pulldown
- Pulldown
- Pulldown
- Pulldown
- Pulldown
- Pulldown
- Pulldown
- Pulldown

- Phase Detector
- VCO 575MHz - 630MHz
- M = ÷25
- NA = ÷1, ÷2, ÷4, ÷5
- NB = ÷1, ÷2, ÷4, ÷5
- NC = ÷1, ÷2, ÷4, ÷5
- 2
- 2
- 2
- 2
- 2
- 6
- 6

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Table 1. Pin Descriptions

<table>
<thead>
<tr>
<th>Number</th>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1, 2</td>
<td>XTAL_IN, XTAL_OUT</td>
<td>Input</td>
<td>Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.</td>
</tr>
<tr>
<td>3, 12, 31, 46</td>
<td>V_{EE}</td>
<td>Power</td>
<td>Negative supply pins.</td>
</tr>
<tr>
<td>4, 5</td>
<td>SELC0, SELC1</td>
<td>Input</td>
<td>Pulldown Selects the output divider value. See Table 2D.</td>
</tr>
<tr>
<td>6</td>
<td>OEA</td>
<td>Input</td>
<td>Pullup Active high output enable. When logic HIGH, Bank A outputs are enabled and active. When logic LOW, the outputs are disabled and forced to HIGH/LOW. LVCMOS/LVTTL interface levels.</td>
</tr>
<tr>
<td>7, 48</td>
<td>V_{CC}</td>
<td>Power</td>
<td>Active high output enable. When logic HIGH, Bank B outputs are enabled and active. When logic LOW, the outputs are disabled and forced to HIGH/LOW. LVCMOS/LVTTL interface levels.</td>
</tr>
<tr>
<td>8</td>
<td>OEB</td>
<td>Input</td>
<td>Pullup Active high output enable. When logic HIGH, Bank C outputs are enabled and active. When logic LOW, the outputs are disabled and forced to HIGH/LOW. LVCMOS/LVTTL interface levels.</td>
</tr>
<tr>
<td>9</td>
<td>OEC</td>
<td>Input</td>
<td>Pulldown Active high output enable. When logic HIGH, Bank C outputs are enabled and active. When logic LOW, the outputs are disabled and forced to HIGH/LOW. LVCMOS/LVTTL interface levels.</td>
</tr>
<tr>
<td>10, 11</td>
<td>SELB0, SELB1</td>
<td>Input</td>
<td>Pulldown Selects the output divider value. See Table 3C.</td>
</tr>
<tr>
<td>13, 19, 24, 32, 37</td>
<td>V_{CCO}</td>
<td>Power</td>
<td>Output supply pins.</td>
</tr>
<tr>
<td>14, 15</td>
<td>nQC1, QC1</td>
<td>Output</td>
<td>Differential output pair. LVPECL or LVDS interface levels.</td>
</tr>
<tr>
<td>16, 17</td>
<td>nQC0, QC0</td>
<td>Output</td>
<td>Differential output pair. LVPECL or LVDS interface levels.</td>
</tr>
<tr>
<td>18</td>
<td>nc</td>
<td>Unused</td>
<td>No connect.</td>
</tr>
<tr>
<td>20, 21</td>
<td>nQB1, QB1</td>
<td>Output</td>
<td>Differential output pair. LVPECL or LVDS interface levels.</td>
</tr>
<tr>
<td>22, 23</td>
<td>nQB0, QB0</td>
<td>Output</td>
<td>Differential output pair. LVPECL or LVDS interface levels.</td>
</tr>
<tr>
<td>25, 26</td>
<td>nQA5, QA5</td>
<td>Output</td>
<td>Differential output pair. LVPECL or LVDS interface levels.</td>
</tr>
<tr>
<td>27, 28</td>
<td>nQA4, QA4</td>
<td>Output</td>
<td>Differential output pair. LVPECL or LVDS interface levels.</td>
</tr>
<tr>
<td>29, 30</td>
<td>nQA3, QA3</td>
<td>Output</td>
<td>Differential output pair. LVPECL or LVDS interface levels.</td>
</tr>
<tr>
<td>33, 34</td>
<td>nQA2, QA2</td>
<td>Output</td>
<td>Differential output pair. LVPECL or LVDS interface levels.</td>
</tr>
<tr>
<td>35, 36</td>
<td>nQA1, QA1</td>
<td>Output</td>
<td>Differential output pair. LVPECL or LVDS interface levels.</td>
</tr>
<tr>
<td>38, 39</td>
<td>nQA0, QA0</td>
<td>Output</td>
<td>Differential output pair. LVPECL or LVDS interface levels.</td>
</tr>
<tr>
<td>40</td>
<td>V_{CCA}</td>
<td>Power</td>
<td>Analog supply pin.</td>
</tr>
<tr>
<td>41, 42</td>
<td>SELA1, SELA0</td>
<td>Input</td>
<td>Pulldown Selects the output divider value. See Table 3B.</td>
</tr>
<tr>
<td>43</td>
<td>SEL_OUT</td>
<td>Input</td>
<td>Pulldown Selects between either LVDS or LVPECL output levels. See Table 3A.</td>
</tr>
<tr>
<td>44</td>
<td>MR</td>
<td>Input</td>
<td>Pulldown Master Reset. LVCMOS/LVTTL interface levels.</td>
</tr>
<tr>
<td>45</td>
<td>BYPASS</td>
<td>Input</td>
<td>Pulldown PLL BYPASS mode select pin. See Table 3F. LVCMOS/LVTTL interface levels.</td>
</tr>
<tr>
<td>47</td>
<td>REF_CLK</td>
<td>Input</td>
<td>Pulldown Single-ended reference clock input. LVCMOS/LVTTL interface levels.</td>
</tr>
</tbody>
</table>

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.
### Table 2. Pin Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_IN</td>
<td>Input Capacitance</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>R_PULLUP</td>
<td>Input Pullup Resistor</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td>R_PULLDOWN</td>
<td>Input Pulldown Resistor</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>kΩ</td>
</tr>
</tbody>
</table>

### Function Tables

#### Table 3A. SEL_OUT Function Table

<table>
<thead>
<tr>
<th>Input SEL_OUT</th>
<th>Output Levels</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 (default)</td>
<td>LVDS</td>
</tr>
<tr>
<td>1</td>
<td>LVPECL</td>
</tr>
</tbody>
</table>

#### Table 3B. SELA Function Table

<table>
<thead>
<tr>
<th>Inputs SELA0 SELA1</th>
<th>NA Bank A Output Divider</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 (default) 0 (default)</td>
<td>÷1</td>
</tr>
<tr>
<td>0 1</td>
<td>÷2</td>
</tr>
<tr>
<td>1 0</td>
<td>÷4</td>
</tr>
<tr>
<td>1 1</td>
<td>÷5</td>
</tr>
</tbody>
</table>

#### Table 3C. SELB Function Table

<table>
<thead>
<tr>
<th>Inputs SELB0 SELB1</th>
<th>NB Bank B Output Divider</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 (default) 0 (default)</td>
<td>÷1</td>
</tr>
<tr>
<td>0 1</td>
<td>÷2</td>
</tr>
<tr>
<td>1 0</td>
<td>÷4</td>
</tr>
<tr>
<td>1 1</td>
<td>÷5</td>
</tr>
</tbody>
</table>

#### Table 3D. SELC Function Table

<table>
<thead>
<tr>
<th>Inputs SELC0 SELC1</th>
<th>NC Bank C Output Divider</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 (default) 0 (default)</td>
<td>÷1</td>
</tr>
<tr>
<td>0 1</td>
<td>÷2</td>
</tr>
<tr>
<td>1 0</td>
<td>÷4</td>
</tr>
<tr>
<td>1 1</td>
<td>÷5</td>
</tr>
</tbody>
</table>

#### Table 3E. MR Function Table

<table>
<thead>
<tr>
<th>Input MR</th>
<th>Device Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 (default)</td>
<td>Normal</td>
</tr>
<tr>
<td>1</td>
<td>Master Reset</td>
</tr>
</tbody>
</table>

#### Table 3F. BYPASS Function Table

<table>
<thead>
<tr>
<th>Input BYPASS</th>
<th>Device Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 (default)</td>
<td>PLL mode. The output frequency is the VCO frequency divided by the selected output divider.</td>
</tr>
<tr>
<td>1</td>
<td>Bypass mode. The output frequency is the REF_CLK frequency divided by two and then divided by the selected output divider.</td>
</tr>
</tbody>
</table>
Absolute Maximum Ratings

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the DC Characteristics or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

<table>
<thead>
<tr>
<th>Item</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage, $V_{CC}$</td>
<td>4.6V</td>
</tr>
<tr>
<td>Inputs, $V_I$</td>
<td>0V to $V_{CC}$</td>
</tr>
<tr>
<td>XTAL_IN</td>
<td>-0.5V to $V_{CC} + 0.5V$</td>
</tr>
<tr>
<td>Other Inputs</td>
<td></td>
</tr>
<tr>
<td>Outputs, LVPECL $I_O$</td>
<td>50mA</td>
</tr>
<tr>
<td>Continuos Current</td>
<td>10mA</td>
</tr>
<tr>
<td>Surge Current</td>
<td></td>
</tr>
<tr>
<td>Outputs, LVDS $I_O$</td>
<td>10mA</td>
</tr>
<tr>
<td>Continuos Current</td>
<td>15mA</td>
</tr>
<tr>
<td>Surge Current</td>
<td></td>
</tr>
<tr>
<td>Package Thermal Impedance, $\theta_{JA}$</td>
<td>33.1°C/W (0 mps)</td>
</tr>
<tr>
<td>Storage Temperature, $T_{STG}$</td>
<td>-65°C to 150°C</td>
</tr>
</tbody>
</table>

DC Electrical Characteristics

Table 4A. LVDS Power Supply DC Characteristics, $V_{CC} = V_{CCO} = 3.3\text{V} \pm 5\%$, $T_A = -40°C$ to 85°C

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>Core Supply Voltage</td>
<td></td>
<td>3.135</td>
<td>3.3</td>
<td>3.465</td>
<td>V</td>
</tr>
<tr>
<td>$V_{CCA}$</td>
<td>Analog Supply Voltage</td>
<td>$V_{CC} - 0.16$</td>
<td>3.3</td>
<td></td>
<td>$V_{CC}$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{CCO}$</td>
<td>Output Supply Voltage</td>
<td></td>
<td>3.135</td>
<td>3.3</td>
<td>3.465</td>
<td>V</td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>Power Supply Current</td>
<td></td>
<td></td>
<td></td>
<td>107</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{CCA}$</td>
<td>Analog Supply Current</td>
<td></td>
<td></td>
<td></td>
<td>16</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{CCO}$</td>
<td>Output Supply Current</td>
<td></td>
<td></td>
<td></td>
<td>228</td>
<td>mA</td>
</tr>
</tbody>
</table>

NOTE: Outputs configured as LVDS (SEL_OUT = 0).

NOTE: For the Power Supply Voltage Sequence Information, see Applications Information section.

Table 4B. LVPECL Power Supply DC Characteristics, $V_{CC} = V_{CCO} = 3.3\text{V} \pm 5\%$, $V_{EE} = 0\text{V}$, $T_A = -40°C$ to 85°C

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>Core Supply Voltage</td>
<td></td>
<td>3.135</td>
<td>3.3</td>
<td>3.465</td>
<td>V</td>
</tr>
<tr>
<td>$V_{CCA}$</td>
<td>Analog Supply Voltage</td>
<td>$V_{CC} - 0.16$</td>
<td>3.3</td>
<td></td>
<td>$V_{CC}$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{CCO}$</td>
<td>Output Supply Voltage</td>
<td></td>
<td>3.135</td>
<td>3.3</td>
<td>3.465</td>
<td>V</td>
</tr>
<tr>
<td>$I_{EE}$</td>
<td>Power Supply Current</td>
<td></td>
<td></td>
<td></td>
<td>181</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{CCA}$</td>
<td>Analog Supply Current</td>
<td></td>
<td></td>
<td></td>
<td>16</td>
<td>mA</td>
</tr>
</tbody>
</table>

NOTE: Outputs configured as LVPECL (SEL_OUT = 1).

NOTE: For the Power Supply Voltage Sequence Information, see Applications Information section.
**Table 4C. LVCMOS/LVTTL DC Characteristics**, $V_{CC} = V_{CCO} = 3.3\,\text{V} \pm 5\%, \, V_{EE} = 0\,\text{V}, \, T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>Input High Voltage</td>
<td>$V_{CC} = 3.3,\text{V}$</td>
<td>2.2</td>
<td>$V_{CC} + 0.3$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input Low Voltage</td>
<td>$V_{CC} = 3.3,\text{V}$</td>
<td>-0.3</td>
<td>0.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>Input High Current</td>
<td>$V_{CC} = V_{IN} = 3.465,\text{V}$</td>
<td>150</td>
<td>$\mu\text{A}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>REF_CLK, BYPASS, MR, SELA[1:0], SELB[1:0], SELC[1:0], SEL_OUT, OEA, OEB, OEC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Input Low Current</td>
<td>$V_{CC} = V_{IN} = 3.465,\text{V}$</td>
<td>10</td>
<td>$\mu\text{A}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>REF_CLK, BYPASS, MR, SELA[1:0], SELB[1:0], SELC[1:0], SEL_OUT, OEA, OEB, OEC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Table 4D. LVPECL DC Characteristics**, $V_{CC} = V_{CCO} = 3.3\,\text{V} \pm 5\%, \, V_{EE} = 0\,\text{V}, \, T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OH}$</td>
<td>Output High Voltage</td>
<td>$V_{CCO} - 1.2$</td>
<td>$V_{CCO} - 0.7$</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output Low Voltage</td>
<td>$V_{CCO} - 2.0$</td>
<td>$V_{CCO} - 1.5$</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{SWING}$</td>
<td>Peak-to-Peak Output Voltage Swing</td>
<td></td>
<td>0.6</td>
<td>1.0</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

**Table 4E. LVDS DC Characteristics**, $V_{CC} = V_{CCO} = 3.3\,\text{V} \pm 5\%, \, T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OD}$</td>
<td>Differential Output Voltage</td>
<td></td>
<td>268</td>
<td>475</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>$\Delta V_{OD}$</td>
<td>$V_{OD}$ Magnitude Change</td>
<td></td>
<td></td>
<td>50</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>$V_{OS}$</td>
<td>Offset Voltage</td>
<td></td>
<td>1.125</td>
<td>1.375</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$\Delta V_{OS}$</td>
<td>$V_{OS}$ Magnitude Change</td>
<td></td>
<td></td>
<td>50</td>
<td>mV</td>
<td></td>
</tr>
</tbody>
</table>
AC Electrical Characteristics

Table 5A. LVPECL AC Characteristics, $V_{CC} = V_{CCO} = 3.3\,\text{V} \pm 5\%$, $V_{EE} = 0\,\text{V}$, $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>$Q_x = \div 1$</td>
<td>575</td>
<td>625</td>
<td>630</td>
<td>MHz</td>
</tr>
<tr>
<td>$f_{OUT}$</td>
<td>Output Frequency</td>
<td>$Q_x = \div 2$</td>
<td>287.5</td>
<td>312.5</td>
<td>315</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$Q_x = \div 4$</td>
<td>143.75</td>
<td>156.25</td>
<td>157.5</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$Q_x = \div 5$</td>
<td>115</td>
<td>125</td>
<td>126</td>
<td>MHz</td>
</tr>
<tr>
<td>$\bar{j}_{it(\phi)}$</td>
<td>RMS Phase Jitter (Random); NOTE 1</td>
<td>156.25MHz, Integration Range: (1MHz – 20MHz)</td>
<td>0.373</td>
<td>0.422</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>156.25MHz, Integration Range: (12kHz – 20MHz)</td>
<td>0.694</td>
<td>1.04</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>$\bar{j}_{it(cc)}$</td>
<td>Cycle-to-Cycle Jitter; NOTE 2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>$t_{R} / t_{F}$</td>
<td>Output Rise/Fall Time</td>
<td>10% to 90%</td>
<td>65</td>
<td>180</td>
<td>350</td>
<td>ps</td>
</tr>
<tr>
<td>odc</td>
<td>Output Duty Cycle</td>
<td></td>
<td>47</td>
<td>53</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>$t_{LOCK}$</td>
<td>PLL Lock Time</td>
<td></td>
<td></td>
<td>130</td>
<td>ms</td>
<td></td>
</tr>
</tbody>
</table>

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: Outputs configured as LVPECL (SEL_OUT = 1).

NOTE 1: Refer to the Phase Noise Plot.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

Table 5B. LVDS AC Characteristics, $V_{CC} = V_{CCO} = 3.3\,\text{V} \pm 5\%$, $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>$Q_x = \div 1$</td>
<td>575</td>
<td>625</td>
<td>630</td>
<td>MHz</td>
</tr>
<tr>
<td>$f_{OUT}$</td>
<td>Output Frequency</td>
<td>$Q_x = \div 2$</td>
<td>287.5</td>
<td>312.5</td>
<td>315</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$Q_x = \div 4$</td>
<td>143.75</td>
<td>156.25</td>
<td>157.5</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$Q_x = \div 5$</td>
<td>115</td>
<td>125</td>
<td>126</td>
<td>MHz</td>
</tr>
<tr>
<td>$\bar{j}_{it(\phi)}$</td>
<td>RMS Phase Jitter (Random); NOTE 1</td>
<td>156.25MHz, Integration Range: (1MHz – 20MHz)</td>
<td>0.375</td>
<td>0.413</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>156.25MHz, Integration Range: (12kHz – 20MHz)</td>
<td>0.712</td>
<td>1.26</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>$\bar{j}_{it(cc)}$</td>
<td>Cycle-to-Cycle Jitter; NOTE 2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>$t_{R} / t_{F}$</td>
<td>Output Rise/Fall Time</td>
<td>10% to 90%</td>
<td>65</td>
<td>190</td>
<td>350</td>
<td>ps</td>
</tr>
<tr>
<td>odc</td>
<td>Output Duty Cycle</td>
<td></td>
<td>47</td>
<td>53</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>$t_{LOCK}$</td>
<td>PLL Lock Time</td>
<td></td>
<td></td>
<td>130</td>
<td>ms</td>
<td></td>
</tr>
</tbody>
</table>

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: Outputs configured as LVDS (SEL_OUT = 0).

NOTE 1: Refer to the Phase Noise Plot.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
Typical Phase Noise at 156.25MHz (LVPECL)

156.25MHz
RMS Phase Jitter (Random)
1MHz to 20MHz = 0.373ps (typical)

Offset Frequency (Hz)
Noise Power (dBc/Hz)

10 Hz 100 Hz 1 kHz 10 kHz 100 kHz 1 MHz 10 MHz 100 MHz
-70 -80 -90 -100 -110 -120 -130 -140 -150

RMS Phase Jitter (Random)
12kHz to 20MHz = 0.694ps (typical)

Offset Frequency (Hz)
Noise Power (dBc/Hz)

10 Hz 100 Hz 1 kHz 10 kHz 100 kHz 1 MHz 10 MHz 100 MHz
-70 -80 -90 -100 -110 -120 -130 -140 -150
Typical Phase Noise at 156.25MHz (LVDS)

156.25MHz
RMS Phase Jitter (Random)
1MHz to 20MHz = 0.375ps (typical)

Typical Phase Noise at 156.25MHz (LVDS)

156.25MHz
RMS Phase Jitter (Random)
12kHz to 20MHz = 0.712ps (typical)
Parameter Measurement Information

LVPECL Output Load AC Test Circuit

LVDS Output Load AC Test Circuit

RMS Phase Jitter

Cycle-to-Cycle Jitter

LVPECL Output Rise/Fall Time

LVDS Output Rise/Fall Time
Parameter Measurement Information, continued

Output Duty Cycle/Pulse Width/Period

\[ \text{odc} = \frac{t_{PW}}{t_{PERIOD}} \times 100\% \]

Offset Voltage Setup

Differential Output Voltage Setup
Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

REF_CLK Input
For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

Crystal Inputs
For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

LVCMOS Control Pins
All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs
All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVDS Outputs
All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

Table 6. Recommended Crystal Specifications

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>cCut</td>
<td>Fundamental at Cut</td>
<td></td>
</tr>
<tr>
<td>cRes</td>
<td>Parallel Resonance</td>
<td></td>
</tr>
<tr>
<td>fT</td>
<td>Frequency Tolerance</td>
<td>±25ppm at 25°C</td>
</tr>
<tr>
<td>fS</td>
<td>Frequency Stability</td>
<td>±25ppm over -40°C to +85°C</td>
</tr>
<tr>
<td>CL</td>
<td>Load Capacitance</td>
<td>18pF</td>
</tr>
<tr>
<td>CO</td>
<td>Shunt Capacitance</td>
<td>5pF - 7pF</td>
</tr>
<tr>
<td>ESR</td>
<td>Equivalent Series Resistance</td>
<td>20Ω - 50Ω</td>
</tr>
<tr>
<td></td>
<td>Aging @ 25°C</td>
<td>±15ppm/10 Years Maximum</td>
</tr>
</tbody>
</table>

NOTE: External tuning capacitors must be used for proper operation.

Power Supply Voltage Sequence Information

No power sequence restrictions apply if V_CC and V_CCA are supplied by the same power plane and the recommended V_CCA filter is used (see Figure 6). V_CCO may be applied at any time before or after V_CC and V_CCA are applied. If V_CC and V_CCA are not supplied by the same power plane, V_CCA must be powered on before or at the same time V_CC is applied. The V_CCO supply voltage may be applied at any time.
Overdriving the XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in Figure 1A. The XTAL_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

Figure 1A. General Diagram for LVCMOS Driver to XTAL Input Interface

Figure 1B. General Diagram for LVPECL Driver to XTAL Input Interface
LVDS Driver Termination

A general LVDS interface is shown in Figure 2. Standard termination for LVDS type output structure requires both a 100Ω parallel resistor at the receiver and a 100Ω differential transmission line environment. In order to avoid any transmission line reflection issues, the 100Ω resistor must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in Figure 2 can be used with either type of output structure. If using a non-standard termination, it is recommended to contact IDT and confirm if the output is a current source or a voltage source type structure. In addition, since these outputs are LVDS compatible, the input receivers amplitude and common mode input range should be verified for compatibility with the output.

![Figure 2. Typical LVDS Driver Termination](image)

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. Figures 3A and 3B show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

![Figure 3A. 3.3V LVPECL Output Termination](image)

![Figure 3B. 3.3V LVPECL Output Termination](image)
EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in Figure 4. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.
Application Schematic Example

Figure 5 shows an example of 849S625 application schematic. In this example, the device is operated at \( V_{\text{CC}} = V_{\text{CCA}} = V_{\text{CCO}} = 3.3V \). An 18pF parallel resonant 25MHz crystal is used. The load capacitance \( C_1 = 27pF \) and \( C_2 = 27pF \) are recommended for frequency accuracy. Depending on the parasitics of the printed circuit board layout, these values might required slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used. This will require adjusting \( C_1 \) and \( C_2 \). For this device, the crystal load capacitors are required for proper operation.

As with any high speed analog circuitry, the power supply pins are vulnerable to noise. To achieve optimum jitter performance, power supply isolation is required. The 849S625 provides separate power supplies to isolate from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uF capacitor in each power pin filter should be placed on the device side of the PCB and the other components can be placed on the opposite side.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supply frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitances in the local area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set.

![Application Schematic Example](image)

Figure 5. 849S625 Application Schematic

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December 2, 2015
LVPECL Power Considerations

This section provides information on power dissipation and junction temperature for the 849S625. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 849S625 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for \(V_{CC} = 3.3V + 5\% = 3.465V\), which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

The maximum current at 85°C is as follows:

\[ I_{EE\_MAX} = 170mA \]

- Power (core)\(_{MAX} = V_{CC\_MAX} \times I_{EE\_MAX} = 3.465V \times 170mA = 589.05mW \]
- Power (outputs)\(_{MAX} = 33.2mW/Loaded\ Output\ pair\]
  
  If all outputs are loaded, the total power is 10 \(\times 33.2mW = 332mW\)

**Total Power\(_{MAX}\) (3.465V, with all outputs switching) = 589.05mW + 332mW = 921.05mW**

2. Junction Temperature.

Junction temperature, \(T_j\), is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, \(T_j\), to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for \(T_j\) is as follows: \(T_j = \theta_{JA} \times P_{d\_total} + T_A\)

\(T_j =\) Junction Temperature

\(\theta_{JA} =\) Junction-to-Ambient Thermal Resistance

\(P_{d\_total} =\) Total Device Power Dissipation (example calculation is in section 1 above)

\(T_A =\) Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance \(\theta_{JA}\) must be used. Assuming no air flow and a multi-layer board, the appropriate value is 33.1°C/W per Table 7 below.

Therefore, \(T_j\) for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.921W \(\times 33.1°C/W = 115.5°C\). This is below the limit of 125°C.

This calculation is only an example. \(T_j\) will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

---

**Table 7. Thermal Resistance \(\theta_{JA}\) for 48 Lead TQFP, E-Pad, Forced Convection**

<table>
<thead>
<tr>
<th>(\theta_{JA}) by Velocity</th>
<th>0</th>
<th>1</th>
<th>2.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Meters per Second</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Multi-Layer PCB, JEDEC Standard Test Boards</td>
<td>33.1°C/W</td>
<td>27.2°C/W</td>
<td>25.7°C/W</td>
</tr>
</tbody>
</table>
3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair. LVPECL output driver circuit and termination are shown in Figure 6.

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CCO} - 2V$.

- For logic high, $V_{OUT} = V_{OH_{MAX}} = V_{CCO_{MAX}} - 0.7V$
  
  $(V_{CCO_{MAX}} - V_{OH_{MAX}}) = 0.7V$

- For logic low, $V_{OUT} = V_{OL_{MAX}} = V_{CCO_{MAX}} - 1.5V$
  
  $(V_{CCO_{MAX}} - V_{OL_{MAX}}) = 1.5V$

$P_d_H$ is power dissipation when the output drives high. $P_d_L$ is the power dissipation when the output drives low.

$P_d_H = \frac{(V_{OH_{MAX}} - (V_{CCO_{MAX}} - 2V))/R_L} * (V_{CCO_{MAX}} - V_{OH_{MAX}}) = \frac{(2V - (V_{CCO_{MAX}} - V_{OH_{MAX}}))/50\Omega} * 0.7V = 18.2mW$

$P_d_L = \frac{(V_{OL_{MAX}} - (V_{CCO_{MAX}} - 2V))/R_L} * (V_{CCO_{MAX}} - V_{OL_{MAX}}) = \frac{(2V - (V_{CCO_{MAX}} - V_{OL_{MAX}}))/50\Omega} * 1.5V = 15mW$

Total Power Dissipation per output pair = $P_d_H + P_d_L = 33.2mW$
LVDS Power Considerations

This section provides information on power dissipation and junction temperature for the 849S625. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 849S625 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for \( V_{CC} = 3.3V + 5\% = 3.465V \), which gives worst case results.

The maximum current at 85°C is as follows:

- \( I_{CC\_MAX} = 100mA \)
- \( I_{CCA\_MAX} = 15mA \)
- \( I_{CCO\_MAX} = 212mA \)

- Power (core) \( MAX = V_{CC\_MAX} \times (I_{CC\_MAX} + I_{CCA\_MAX}) = 3.465V \times (100mA + 15mA) = 398.475mW \)
- Power (outputs) \( MAX = V_{CCO\_MAX} \times I_{CCO\_MAX} = 3.465V \times 212mA = 734.58mW \)

Total Power \( MAX = 398.475mW + 734.58mW = 1133.1mW \)

2. Junction Temperature.

Junction temperature, \( T_j \), is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, \( T_j \), to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for \( T_j \) is as follows:

\[ T_j = \theta_{JA} \times P_d\_total + T_A \]

\( T_j \) = Junction Temperature

\( \theta_{JA} \) = Junction-to-Ambient Thermal Resistance

\( P_d\_total \) = Total Device Power Dissipation (example calculation is in section 1 above)

\( T_A \) = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance \( \theta_{JA} \) must be used. Assuming no air flow and a multi-layer board, the appropriate value is 33.1°C/W per Table 8 below.

Therefore, \( T_j \) for an ambient temperature of 85°C with all outputs switching is:

\[ 85°C + 1.133W \times 33.1°C/W = 122.5°C \]. This is below the limit of 125°C.

This calculation is only an example. \( T_j \) will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 8. Thermal Resistance \( \theta_{JA} \) for 48 Lead TQFP, E-Pad, Forced Convection

<table>
<thead>
<tr>
<th>( \theta_{JA} ) by Velocity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Meters per Second</td>
</tr>
<tr>
<td>Multi-Layer PCB, JEDEC Standard Test Boards</td>
</tr>
</tbody>
</table>
Reliability Information

Table 9. $\theta_{JA}$ vs. Air Flow Table for a 48 Lead TQFP, E-Pad

<table>
<thead>
<tr>
<th>Meters per Second</th>
<th>$\theta_{JA}$ vs. Air Flow</th>
<th>0</th>
<th>1</th>
<th>2.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multi-Layer PCB, JEDEC Standard Test Boards</td>
<td>$\theta_{JA}$</td>
<td>33.1°C/W</td>
<td>27.2°C/W</td>
<td>25.7°C/W</td>
</tr>
</tbody>
</table>

Transistor Count

The transistor count for 849S625 is: 3696
Table 10. Package Dimensions for 48 Lead TQFP, E-Pad

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Minimum</th>
<th>Nominal</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>N</td>
<td>0</td>
<td>48</td>
<td></td>
</tr>
<tr>
<td>A</td>
<td>0.05</td>
<td>0.10</td>
<td>0.15</td>
</tr>
<tr>
<td>A1</td>
<td>0.95</td>
<td>1.00</td>
<td>1.05</td>
</tr>
<tr>
<td>A2</td>
<td>0.17</td>
<td>0.22</td>
<td>0.27</td>
</tr>
<tr>
<td>b</td>
<td>0.09</td>
<td></td>
<td>0.20</td>
</tr>
<tr>
<td>D &amp; E</td>
<td>9.00</td>
<td>Basic</td>
<td></td>
</tr>
<tr>
<td>D1 &amp; E1</td>
<td>7.00</td>
<td>Basic</td>
<td></td>
</tr>
<tr>
<td>D2 &amp; E2</td>
<td>5.50</td>
<td>Ref.</td>
<td></td>
</tr>
<tr>
<td>D3 &amp; E3</td>
<td>3.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>e</td>
<td>0.5</td>
<td>Basic</td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>0.45</td>
<td>0.60</td>
<td>0.75</td>
</tr>
<tr>
<td>θ</td>
<td>0°</td>
<td>0.60</td>
<td>7°</td>
</tr>
</tbody>
</table>

Reference Document: JEDEC Publication 95, MS-026
## Ordering Information

Table 11. Ordering Information

<table>
<thead>
<tr>
<th>Part/Order Number</th>
<th>Marking</th>
<th>Package</th>
<th>Shipping Packaging</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>849S625BYILF</td>
<td>ICS49S625BIL</td>
<td>“Lead-Free” 48 Lead TQFP, E-Pad</td>
<td>Tray</td>
<td>-40°C to 85°C</td>
</tr>
<tr>
<td>849S625BYILFT</td>
<td>ICS49S625BIL</td>
<td>“Lead-Free” 48 Lead TQFP, E-Pad</td>
<td>Tape &amp; Reel</td>
<td>-40°C to 85°C</td>
</tr>
</tbody>
</table>
## Revision History Sheet

<table>
<thead>
<tr>
<th>Rev</th>
<th>Table</th>
<th>Page</th>
<th>Description of Change</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>T4E</td>
<td>6</td>
<td>VOD: changed units from V to mV</td>
<td>10/1/12</td>
</tr>
<tr>
<td></td>
<td>T11</td>
<td>22</td>
<td>Deleted quantity from Tape &amp; Reel. Deleted Lead-Free note.</td>
<td></td>
</tr>
</tbody>
</table>
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