

### Description

The 870161 is a low skew, 1:16 LVCMOS/LVTTL Clock Generator. The device has four banks of four outputs and each bank can be independently selected for  $\div 1$  or  $\div 2$  frequency operation. Each bank also has its own power supply pins so that the banks can operate at the following different voltage levels: 3.3V, 2.5V, and 1.8V. The low impedance LVCMOS/LVTTL outputs are designed to drive 50 $\Omega$  series or parallel terminated transmission lines.

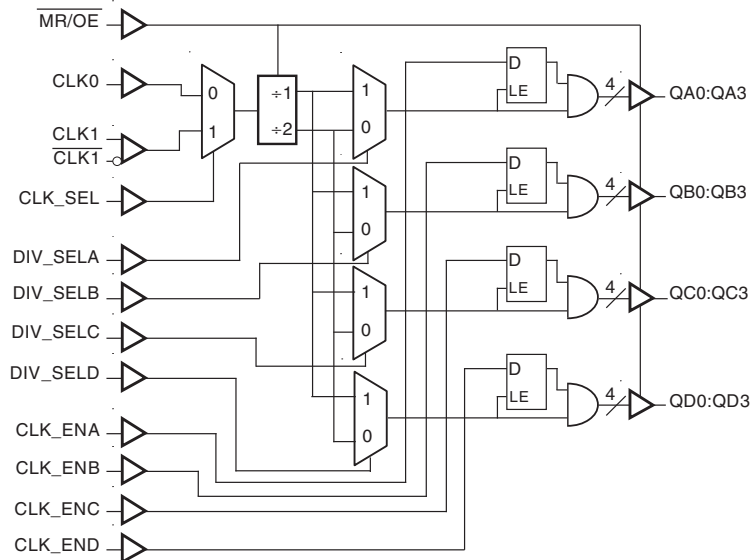
The divide select inputs, DIV\_SELA:DIV\_SELD, control the output frequency of each bank. The output banks can be independently selected for  $\div 1$  or  $\div 2$  operation. The bank enable inputs, CLK\_ENA:CLK\_END, support enabling and disabling each bank of outputs individually. The CLK\_ENA:CLK\_END circuitry has a synchronizer to prevent runt pulses when enabling or disabling the clock outputs. The master reset input, MR/OE, resets the  $\div 1/\div 2$  flip flops and also controls the active and high impedance states of all outputs. This pin has an internal pull-up resistor and is normally used only for test purposes or in systems which use low power modes.

The 870161 is characterized to operate with the core at 3.3V or 2.5V and the banks at 3.3V, 2.5V, or 1.8V. Guaranteed bank, output, and part-to-part skew characteristics make the 870161 ideal for those clock applications demanding well-defined performance and repeatability.

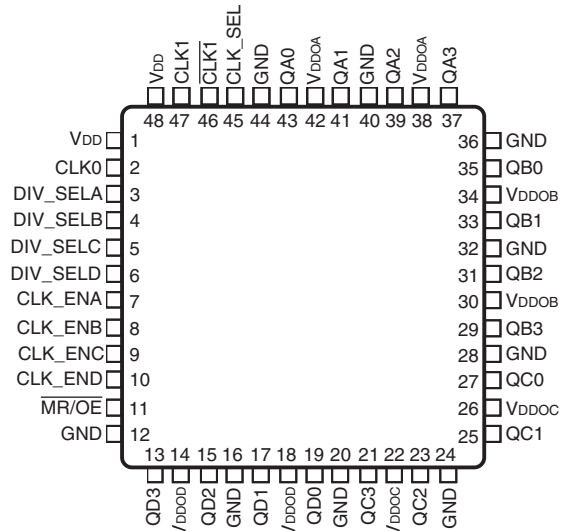
### Features

- Sixteen LVCMOS/LVTTL outputs (4 banks of 4 outputs)
- Selectable differential CLK1/CLK1 or LVCMOS/LVTTL clock input
- CLK1, CLK1 pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- CLK0 supports the following input types: LVCMOS, LVTTL
- Maximum output frequency: 250MHz
- Independent bank control for  $\div 1$  or  $\div 2$  operation
- Independent output bank voltage settings for 3.3V, 2.5V, or 1.8V operation
- Asynchronous clock enable/disable
- Output skew: 170ps (maximum)
- Bank skew: 50ps (maximum)
- Part-to-Part Skew: 800ps (maximum)
- Supply modes:  
Core/Output  
3.3V/3.3V  
3.3V/2.5V  
3.3V/1.8V  
2.5V/2.5V  
2.5V/1.8V
- -40°C to 85°C ambient operating temperature
- Lead-free packaging

### Block Diagram



### Pin Assignment



**870161**

**48-Lead LQFP**

**7mm x 7mm x 1.4mm package body**

**Y Package**

**Top View**

**Table 1. Pin Descriptions**

Number	Name	Type		Description
1, 48	V <sub>DD</sub>	Power		Positive supply pins.
2	CLK0	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
3	DIV_SELA	Input	Pullup	Controls frequency division for Bank A outputs. See Table 3. LVCMOS / LVTTL interface levels.
4	DIV_SELB	Input	Pullup	Controls frequency division for Bank B outputs. See Table 3. LVCMOS / LVTTL interface levels.
5	DIV_SELC	Input	Pullup	Controls frequency division for Bank C outputs. See Table 3. LVCMOS / LVTTL interface levels.
6	DIV_SELD	Input	Pullup	Controls frequency division for Bank D outputs. See Table 3. LVCMOS / LVTTL interface levels.
7	CLK_ENA	Input	Pullup	Output enable for Bank A outputs. Active HIGH. If pin is LOW, outputs drive low. LVCMOS/LVTTL interface levels. See Table 3.
8	CLK_ENB	Input	Pullup	Output enable for Bank A outputs. Active HIGH. If pin is LOW, outputs drive low. LVCMOS/LVTTL interface levels. See Table 3.
9	CLK_ENC	Input	Pullup	Output enable for Bank A outputs. Active HIGH. If pin is LOW, outputs drive low. LVCMOS/LVTTL interface levels. See Table 3.
10	CLK_END	Input	Pullup	Output enable for Bank A outputs. Active HIGH. If pin is LOW, outputs drive low. LVCMOS/LVTTL interface levels. See Table 3.
11	$\overline{\text{MR/OE}}$	Input	Pullup	Master reset. When LOW, resets the $\pm 1/\pm 2$ flip flops and sets the outputs to high impedance. LVCMOS / LVTTL interface levels.
12, 16, 20, 24, 28, 32, 36, 40, 44	GND	Power		Power supply ground
13, 15, 17, 19	QD3, QD2, QD1, QD0	Output		Bank D single-ended clock outputs. LVCMOS/LVTTL interface levels.
14, 18	V <sub>DDOD</sub>	Power		Bank D output supply pins.
21, 23, 25, 27	QC3, QC2, QC1, QC0	Output		Bank C single-ended clock outputs. LVCMOS/LVTTL interface levels.
22, 26	V <sub>DDOC</sub>	Power		Bank C output supply pins.
29, 31, 33, 35	QB3, QB2, QB1, QB0	Output		Bank C single-ended clock outputs. LVCMOS/LVTTL interface levels.
30, 34	V <sub>DDOB</sub>	Power		Bank B output supply pins.
37, 39, 41, 43	QA3, QA2, QA1, QA0	Output		Bank A single-ended clock outputs. LVCMOS/LVTTL interface levels.
38, 42	V <sub>DDOA</sub>	Power		Bank B output supply pins.
45	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK1, $\overline{\text{CLK1}}$ inputs. When LOW, selects CLK0 input. LVCMOS / LVTTL interface levels.
46	$\overline{\text{CLK1}}$	Input	Pullup	Inverting differential clock input.
47	CLK1	Input	Pulldown	Non-inverting differential clock input.

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$C_{IN}$	Input Capacitance			4		pF
$R_{PULLUP}$	Input Pullup Resistor			51		k $\Omega$
$R_{PULLDOWN}$	Input Pulldown Resistor			51		k $\Omega$
$C_{PD}$	Power Dissipation Capacitance (per output); NOTE 1	$V_{DD}, V_{DDOx} = 3.465V$			18	pF
		$V_{DD}, V_{DDOx} = 2.625V$			12	pF
		$V_{DD} = 3.465V,$ $V_{DDOx} = 2.625V$			20	pF
		$V_{DD} = 3.465V,$ $V_{DDOx} = 1.89V$			30	pF
		$V_{DD} = 2.625V,$ $V_{DDOx} = 1.89V$			14	pF
$R_{OUT}$	Output Impedance		5	7	12	$\Omega$

NOTE 1:  $V_{DDOx}$  denotes  $V_{DDOA}, V_{DDOB}, V_{DDOC}, V_{DDOD}$ .

## Function Tables

**Table 3. Function Table**

Inputs			Outputs	
$\overline{MR/OE}$	CLK_ENx	DIV_SELx	Bank [A:D]	Qx Frequency
0	X	X	Hi-Z	N/A
1	1	0	Active	fIN/2
1	1	1	Active	fIN
1	0	X	LOW	N/A

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{CC}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $V_O$	-0.5V to $V_{DD_{Ox}} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$	47.9°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDOx} = 3.3V \pm 5\%$ ,  $2.5V \pm 5\%$ ,  $1.8V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Positive Supply Voltage		3.135	3.3	3.465	V
$V_{DDOA}$ , $V_{DDOB}$ , $V_{DDOC}$ , $V_{DDOD}$	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
			1.71	1.8	1.89	V
$I_{DD}$	Power Supply Current				100	mA
$I_{DDOA}$ , $I_{DDOB}$ , $I_{DDOC}$ , $I_{DDOD}$	Output Supply Current				15	mA

**Table 4B. Power Supply DC Characteristics,  $V_{DD} = 2.5V \pm 5\%$ ,  $V_{DDOx} = 2.5V \pm 5\%$ ,  $1.8V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Positive Supply Voltage		2.375	2.5	2.625	V
$V_{DDOA}$ , $V_{DDOB}$ , $V_{DDOC}$ , $V_{DDOD}$	Output Supply Voltage		2.375	2.5	2.625	V
			1.71	1.8	1.89	V
$I_{DD}$	Power Supply Current				95	mA
$I_{DDOA}$ , $I_{DDOB}$ , $I_{DDOC}$ , $I_{DDOD}$	Output Supply Current				8	mA

**Table 4C. LVCMOS/LVTTL DC Characteristics,  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$** 

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		$V_{DD} = 3.465\text{V}$	2		$V_{DD} + 0.3$	V
			$V_{DD} = 2.625\text{V}$	1.7		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage		$V_{DD} = 3.465\text{V}$	-0.3		0.8	V
			$V_{DD} = 2.625\text{V}$	-0.3		0.7	V
$I_{IH}$	Input High Current	CLK0, CLK_SEL	$V_{DD} = V_{IN} = 3.465\text{V}$ or $2.625\text{V}$			150	$\mu\text{A}$
		CLK_EN[A:D], DIV_SEL[A:D], MR/OE	$V_{DD} = V_{IN} = 3.465\text{V}$ or $2.625\text{V}$			5	$\mu\text{A}$
$I_{IL}$	Input Low Current	CLK0, CLK_SEL	$V_{DD} = 3.465\text{V}$ or $2.625\text{V}$ , $V_{IN} = 0\text{V}$	-5			$\mu\text{A}$
		CLK_EN[A:D], DIV_SEL[A:D], MR/OE	$V_{DD} = 3.465\text{V}$ or $2.625\text{V}$ , $V_{IN} = 0\text{V}$	-150			$\mu\text{A}$
$V_{OH}$	Output High Voltage; NOTE 1		$V_{DDOX} = 3.3\text{V} \pm 5\%$	2.6			V
			$V_{DDOX} = 2.5\text{V} \pm 5\%$	1.8			V
			$V_{DDOX} = 1.8\text{V} \pm 5\%$ ; $I_{OH} = -2\text{mA}$	$V_{DDOX} - 0.45$			V
$V_{OL}$	Output Low Voltage; NOTE 1		$V_{DDOX} = 3.3\text{V} \pm 5\%$			0.5	V
			$V_{DDOX} = 2.5\text{V} \pm 5\%$			0.5	V
			$V_{DDOX} = 1.8\text{V} \pm 5\%$ ; $I_{OH} = 2\text{mA}$			0.45	V
$I_{OZL}$	Output Hi-Z Current Low			-5		$\mu\text{A}$	
$I_{OZH}$	Output Hi-Z Current High					5	$\mu\text{A}$

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{DDOX}/2$ . See Parameter Measurement Information, *Output Load Test Circuit diagrams*.

**Table 4D. Differential DC Characteristics,  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$** 

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	$\overline{\text{CLK1}}$	$V_{DD} = V_{IN} = 3.465\text{V}$ or $2.625\text{V}$			5	$\mu\text{A}$
		CLK1	$V_{DD} = V_{IN} = 3.465\text{V}$ or $2.625\text{V}$			150	$\mu\text{A}$
$I_{IL}$	Input Low Current	$\overline{\text{CLK1}}$	$V_{DD} = 3.465\text{V}$ or $2.625\text{V}$ , $V_{IN} = 0\text{V}$	-150			$\mu\text{A}$
		CLK1	$V_{DD} = 3.465\text{V}$ or $2.625\text{V}$ , $V_{IN} = 0\text{V}$	-5			$\mu\text{A}$
$V_{PP}$	Peak-to-Peak Voltage			0.15		1.3	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		$V_{DD} - 0.85$	V

NOTE 1: Common mode input voltage is defined as  $V_{IH}$ .

NOTE 2: For single-ended applications, the maximum input voltage for CLK1,  $\overline{\text{CLK1}}$  is  $V_{DD} + 0.3\text{V}$ .

## AC Electrical Characteristics

**Table 5A. AC Characteristics,  $V_{DD} = V_{DDOX} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				250	MHz
$t_{PLH}$	Propagation Delay, Low to High	CLK0; NOTE 1A	2.8	3.4	3.9	ns
		CLK1/ $\overline{CLK1}$ ; NOTE 1B	2.75	3.4	4.1	ns
$t_{sk(b)}$	Bank Skew; NOTE 2, 6	Measured on the Rising Edge			50	ps
$t_{sk(o)}$	Output Skew; NOTE 3, 6	Measured on the Rising Edge			170	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 4, 6				800	ps
$t_R / t_F$	Output Rise/Fall Time; NOTE 5	20% to 80%	200		700	ps
odc	Output Duty Cycle	$f < 175MHz$	45		55	%
		$f \geq 175MHz$	40		60	%
$t_{EN}$	Output Enable Time; NOTE 5				10	ns
$t_{DIS}$	Output Disable Time; NOTE 5				10	ns

All parameters measured at 250MHz unless noted otherwise.

NOTE 1A: Measured from the  $V_{DD}/2$  of the input to  $V_{DDOX}/2$  of the output.

NOTE 1B: Measured from the differential input crossing point to  $V_{DDOX}/2$  of the output.

NOTE 2: Defined as skew within a bank with equal load conditions.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDOX}/2$ .

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at  $V_{DDOX}/2$ .

NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

**Table 5B. AC Characteristics,  $V_{DD} = V_{DDOX} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				250	MHz
$t_{PLH}$	Propagation Delay, Low to High	CLK0; NOTE 1A	2.9	3.8	4.7	ns
		CLK1/ $\overline{CLK1}$ ; NOTE 1B	3.0	3.6	4.3	ns
$t_{sk(b)}$	Bank Skew; NOTE 2, 6	Measured on the Rising Edge			70	ps
$t_{sk(o)}$	Output Skew; NOTE 3, 6	Measured on the Rising Edge			210	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 4, 6				800	ps
$t_R / t_F$	Output Rise/Fall Time; NOTE 5	20% to 80%	150		700	ps
odc	Output Duty Cycle	$f \leq 125MHz$	40		60	%
$t_{pw}$	Output Pulse Width	$f > 125MHz$	$t_{Period}/2 - 800$		$t_{Period}/2 + 800$	ps
$t_{EN}$	Output Enable Time; NOTE 5				10	ns
$t_{DIS}$	Output Disable Time; NOTE 5				10	ns

For NOTES, please see above, Table 5A.

**Table 5C. AC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDOX} = 2.5V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				250	MHz
$t_{PLH}$	Propagation Delay, Low to High	CLK0; NOTE 1A	2.9	3.5	4.0	ns
		CLK1/ $\overline{CLK1}$ ; NOTE 1B	3.0	3.5	4.0	ns
$t_{sk}(b)$	Bank Skew; NOTE 2, 6	Measured on the Rising Edge			50	ps
$t_{sk}(o)$	Output Skew; NOTE 3, 6	Measured on the Rising Edge			170	ps
$t_{sk}(pp)$	Part-to-Part Skew; NOTE 4, 6				800	ps
$t_R / t_F$	Output Rise/Fall Time; NOTE 5	20% to 80%	200		700	ps
odc	Output Duty Cycle	$f < 175MHz$	45		55	%
		$f \geq 175MHz$	40		60	%
$t_{EN}$	Output Enable Time; NOTE 5				10	ns
$t_{DIS}$	Output Disable Time; NOTE 5				10	ns

All parameters measured at 250MHz unless noted otherwise.

NOTE 1A: Measured from the  $V_{DD}/2$  of the input to  $V_{DDOX}/2$  of the output.

NOTE 1B: Measured from the differential input crossing point to  $V_{DDOX}/2$  of the output.

NOTE 2: Defined as skew within a bank with equal load conditions.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDOX}/2$ .

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at  $V_{DDOX}/2$ .

NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

**Table 5D. AC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDOX} = 1.8V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				250	MHz
$t_{PLH}$	Propagation Delay, Low to High	CLK0; NOTE 1A	3.0	3.9	4.7	ns
		CLK1/ $\overline{CLK1}$ ; NOTE 1B	3.0	3.9	4.7	ns
$t_{sk}(b)$	Bank Skew; NOTE 2, 6	Measured on the Rising Edge			50	ps
$t_{sk}(o)$	Output Skew; NOTE 3, 6	Measured on the Rising Edge			170	ps
$t_{sk}(pp)$	Part-to-Part Skew; NOTE 4, 6				800	ps
$t_R / t_F$	Output Rise/Fall Time; NOTE 5	20% to 80%	200		700	ps
odc	Output Duty Cycle	$f < 175MHz$	45		55	%
		$f \geq 175MHz$	40		60	%
$t_{EN}$	Output Enable Time; NOTE 5				10	ns
$t_{DIS}$	Output Disable Time; NOTE 5				10	ns

For NOTES, please see above, Table 5C.

**Table 5E. AC Characteristics,  $V_{DD} = 2.5V \pm 5\%$ ,  $V_{DDOX} = 1.8V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				250	MHz
$t_{PLH}$	Propagation Delay, Low to High	CLK0; NOTE 1A	3.1	4.1	5.2	ns
		CLK1/ $\overline{CLK1}$ ; NOTE 1B	3.0	3.9	4.7	ns
$t_{sk(b)}$	Bank Skew; NOTE 2, 6	Measured on the Rising Edge			70	ps
$t_{sk(o)}$	Output Skew; NOTE 3, 6	Measured on the Rising Edge			210	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 4, 6				800	ps
$t_R / t_F$	Output Rise/Fall Time; NOTE 5	20% to 80%	150		700	ps
odc	Output Duty Cycle	$f < 175MHz$	45		55	%
		$f \geq 175MHz$	40		60	%
$t_{EN}$	Output Enable Time; NOTE 5				10	ns
$t_{DIS}$	Output Disable Time; NOTE 5				10	ns

All parameters measured at 250MHz unless noted otherwise.

NOTE 1A: Measured from the  $V_{DD}/2$  of the input to  $V_{DDOX}/2$  of the output.

NOTE 1B: Measured from the differential input crossing point to  $V_{DDOX}/2$  of the output.

NOTE 2: Defined as skew within a bank with equal load conditions.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDOX}/2$ .

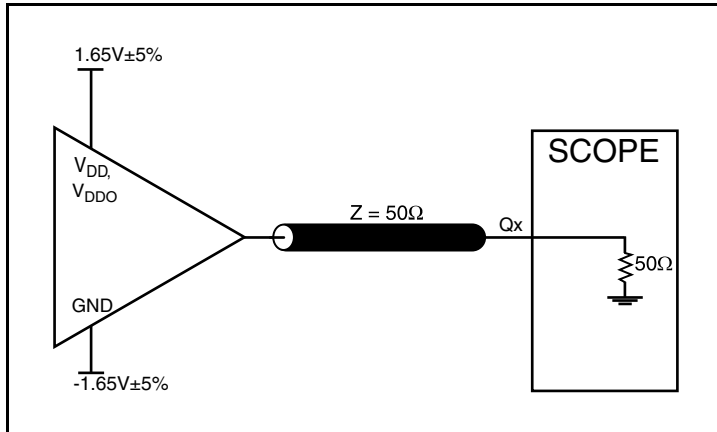
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at  $V_{DDOX}/2$ .

NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

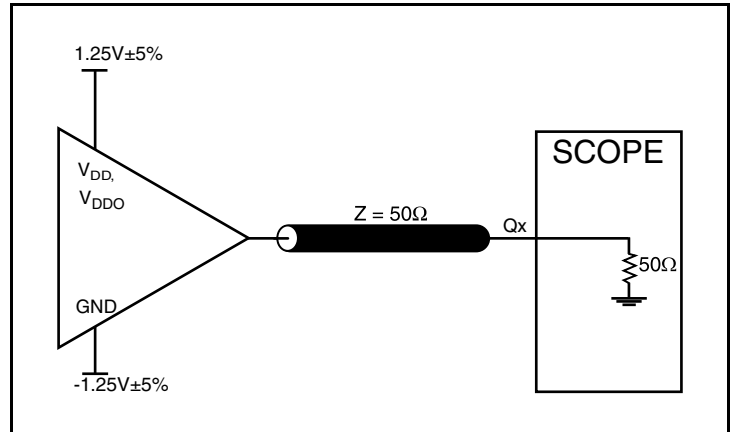
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.



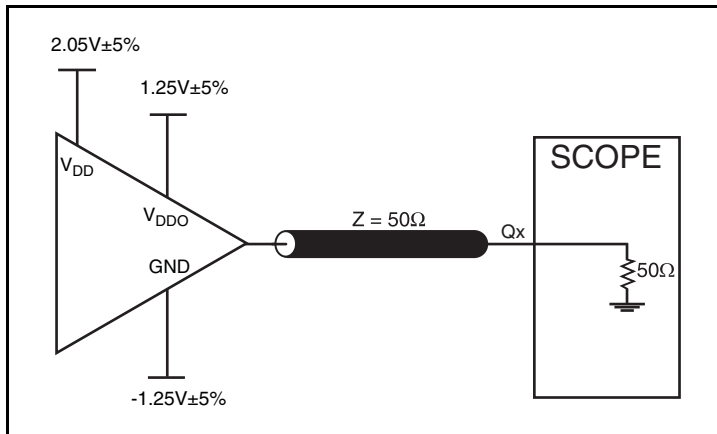
### Parameter Measurement Information



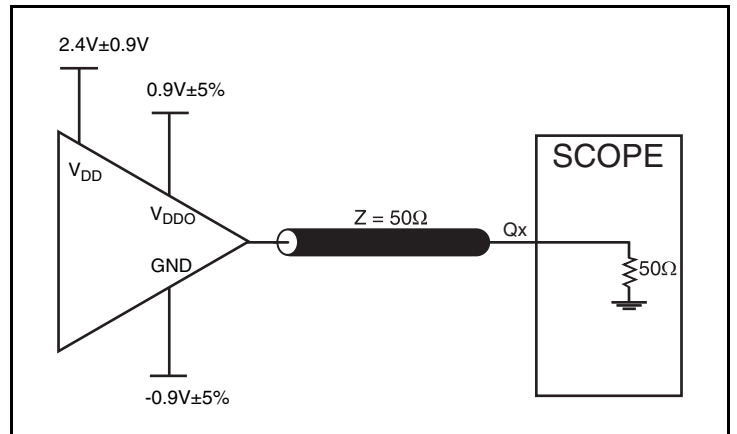
3.3V Core/3.3V LVCMOS Output Load Test Circuit



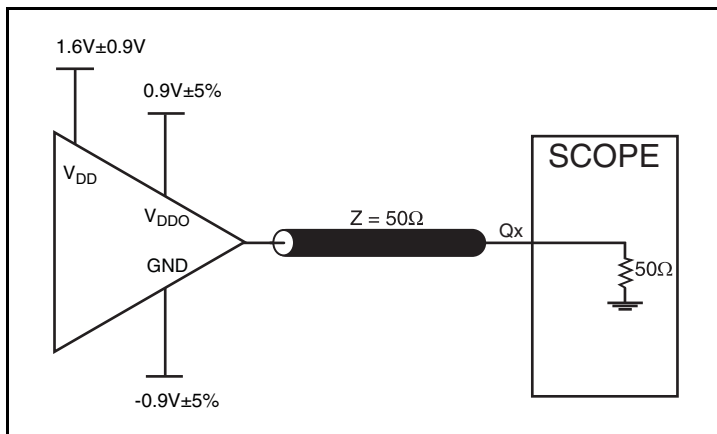
2.5V Core/2.5V LVCMOS Output Load Test Circuit



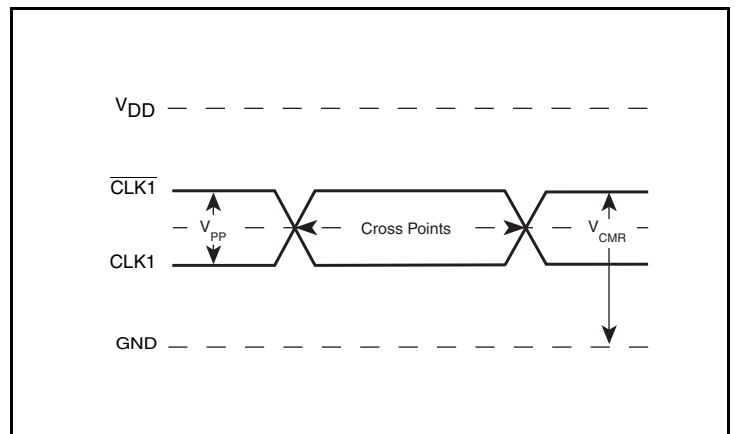
3.3V Core/2.5V LVCMOS Output Load Test Circuit



3.3V Core/1.8V LVCMOS Output Load Test Circuit

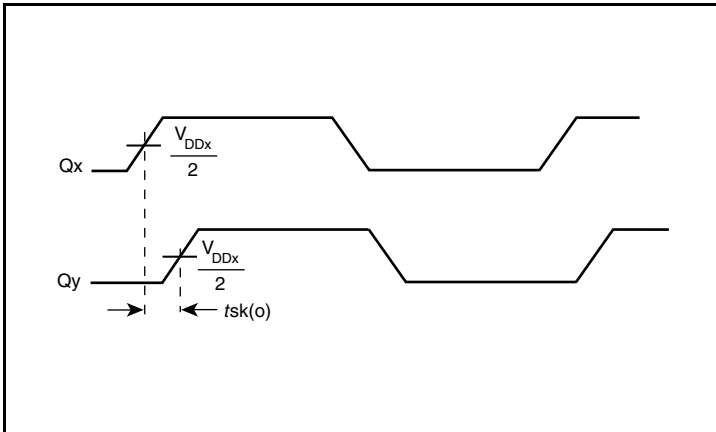


2.5V Core/1.8V LVCMOS Output Load Test Circuit

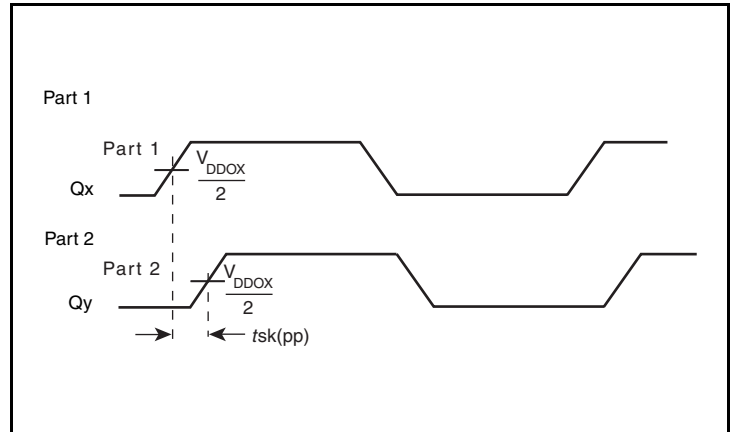


Differential Input Level

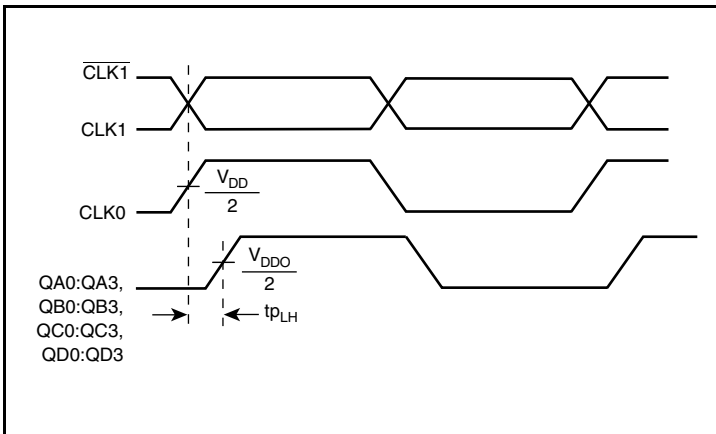
### Parameter Measurement Information, continued



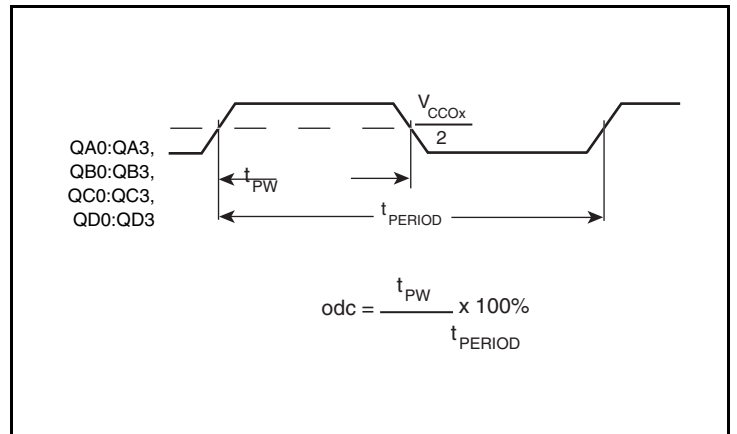
**Output Skew**



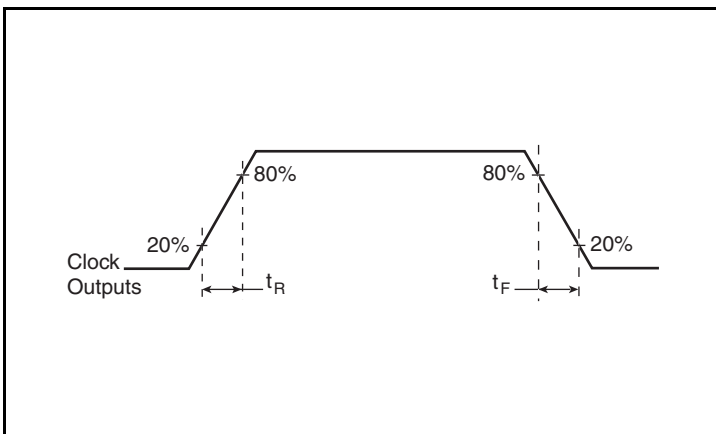
**Part-to-Part Skew**



**Propagation Delay**



**Output Duty Cycle/Pulse Width/Period**



**Output Rise/Fall Time**

## Application Information

### Wiring the Differential Input to Accept Single Ended Levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{DD}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{DD} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R2/R1 = 0.609$ .

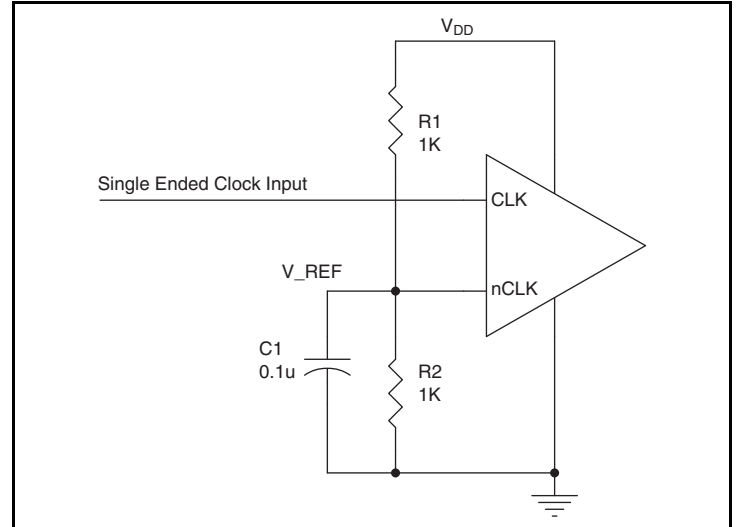


Figure 1. Single-Ended Signal Driving Differential Input

### Recommendations for Unused Input and Output Pins

#### Inputs:

##### CLK/ $\overline{\text{CLK}}$ Inputs:

For applications not requiring the use of the differential input, both CLK and  $\overline{\text{CLK}}$  can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from CLK to ground.

##### CLK Input:

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from the CLK input to ground.

##### LVC MOS Control Pins:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

#### Outputs:

##### LVC MOS Outputs:

All unused LVC MOS output can be left floating. There should be no trace attached.

### Differential Clock Input Interface

The CLK/ $\overline{\text{CLK}}$  accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both signals must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 2A to 2E show interface examples for the CLK/ $\overline{\text{CLK}}$  input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the

vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2A, the input termination applies for IDT LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

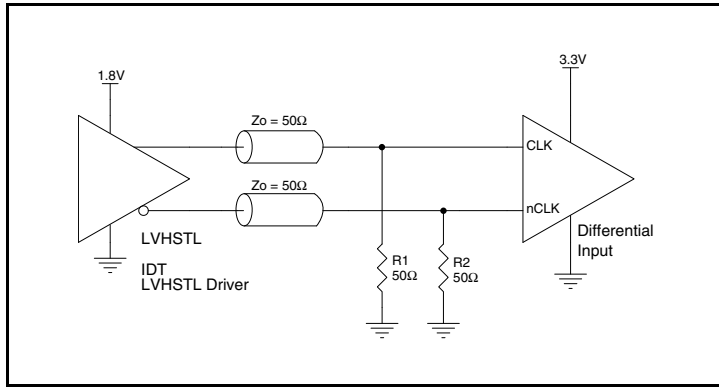


Figure 2A. CLK/ $\overline{\text{CLK}}$  Input Driven by an IDT LVHSTL Driver

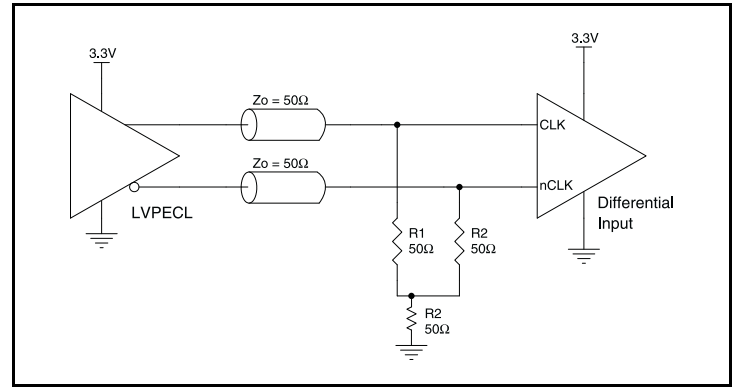


Figure 2B. CLK/ $\overline{\text{CLK}}$  Input Driven by a 3.3V LVPECL Driver

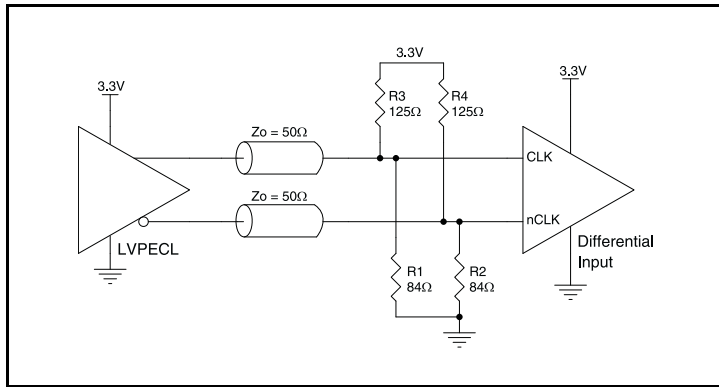


Figure 2C. CLK/ $\overline{\text{CLK}}$  Input Driven by a 3.3V LVPECL Driver

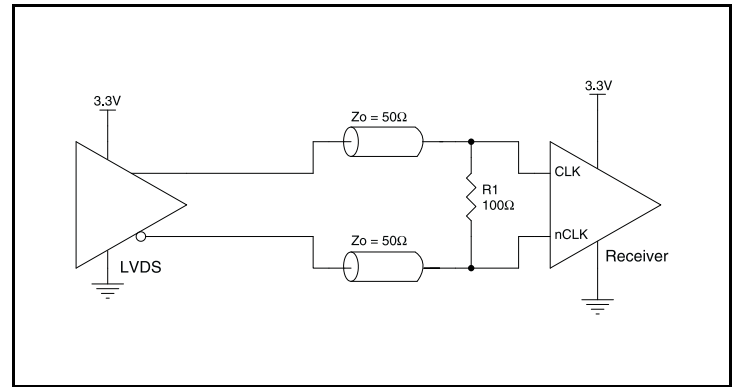


Figure 2D. CLK/ $\overline{\text{CLK}}$  Input Driven by a 3.3V LVDS Driver

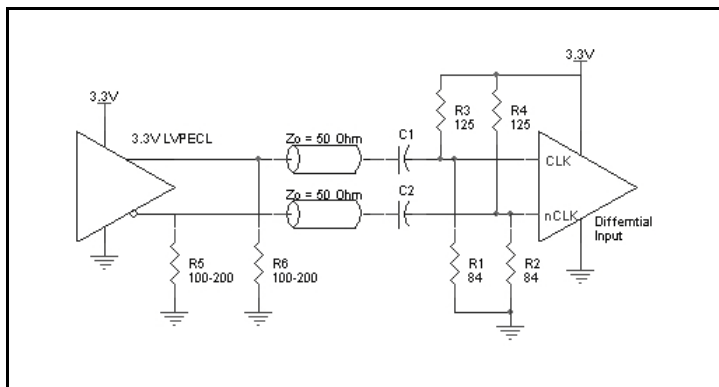


Figure 2E. CLK/ $\overline{\text{CLK}}$  Input Driven by a 3.3V LVPECL Driver with AC Couple

## Reliability Information

**Table 6.  $\theta_{JA}$  vs. Air Flow Table for a 48 Lead LQFP**

$\theta_{JA}$ vs. Air Flow			
Linear Feet per Minute	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB design use multi-layered boards. The data in the second row pertains to most designs.

## Transistor Count

The transistor count for 870161 is: 2034

# Package Outline and Package Dimension

## Package Outline - Y Suffix for 48 Lead LQFP

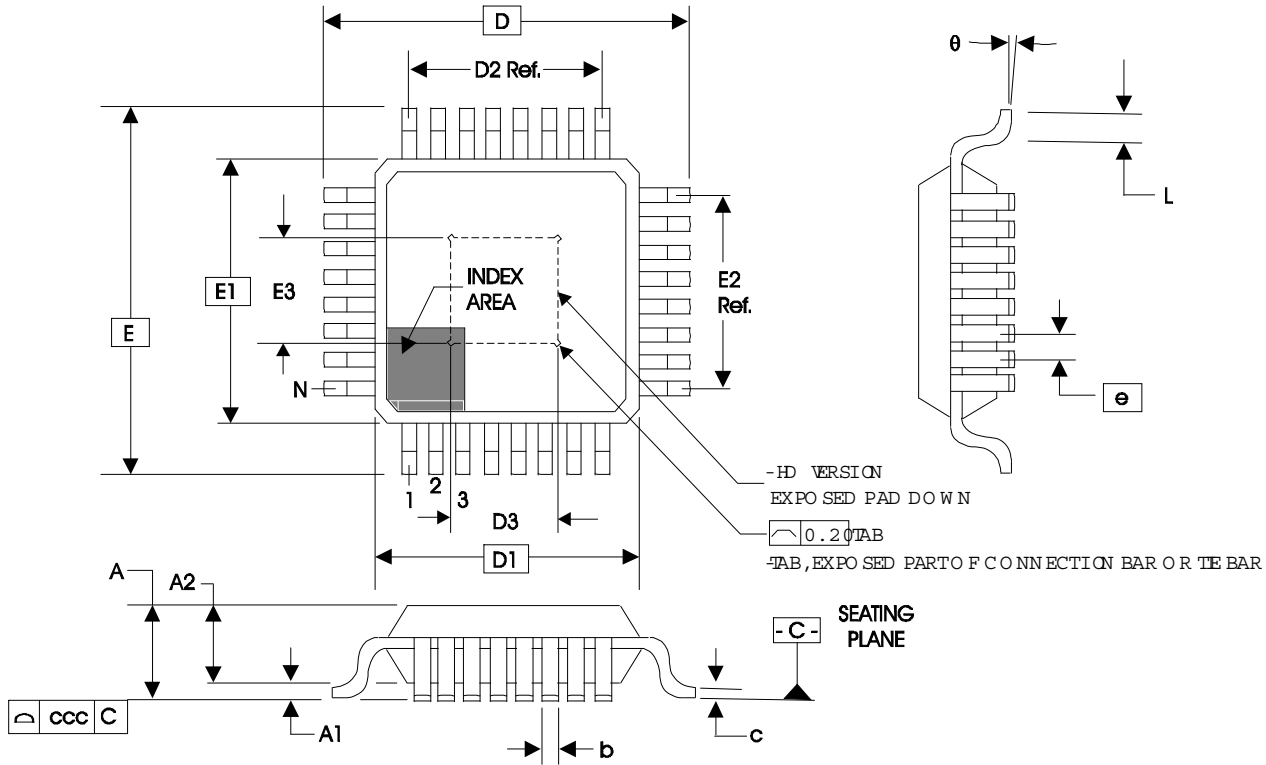


Table 7. Package Dimensions for 48 Lead LQFP

JEDEC Variation: ABC - HD			
All Dimensions in Millimeters			
Symbol	Minimum	Nominal	Maximum
N	48		
A			1.20
A1	0.05	0.10	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09		0.20
D & E	9.00 Basic		
D1 & E1	7.00 Basic		
D2 & E2	5.50 Ref.		
D3 & E3	2.0		7.0
e	0.5 Basic		
L	0.45	0.60	0.75
theta	0°		7°
ccc			0.08

Reference Document: JEDEC Publication 95, MS-026

## Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS87016AYILF	ICS87016AYIL	"Lead-Free" 48 Lead LQFP	Tray	-40°C to 85°C
ICS87016AYILFT	ICS87016AYIL	"Lead-Free" 48 Lead LQFP	Tape & Reel	-40°C to 85°C

## Revision History Sheet

Rev	Table	Page	Description of Change	Date
B		1	Features Section - added 2.5V/2.5V and 2.5V/1.8V to supply mode bullet. Added lead-free bullet	3/30/07
	T2	3	Pin Characteristics Table - added 2.5V/2.5V and 2.5V/1.8V to $C_{PD}$ .	
	T4B	4	Added 2.5V Power Supply DC Characteristics Table.	
	T4C	5	LVC MOS DC Characteristics Table - added 2.5V to $V_{IH}/V_{IL}$ .	
	T4D	5	Differential DC Characteristics Table - added 2.5V to $I_{IH}/I_{IL}$ .	
	T5B	6	Added 2.5V Power Supply DC Characteristics Table.	
	T5E	8	Added 2.5V/1.8V Power Supply DC Characteristics Table.	
	9	Parameter Measurement Information - added <i>2.5V Core/2.5V Output Load Test Circuit</i> and <i>2.5V Core/1.8V Output Load Test Circuit diagrams</i> . Added <i>Recommendations for Unused Input and Output Pins</i> .		
	11	Ordering Information Table - added lead-free Order/Part Number.		
	15			
C	T5B	6	2.5V AC Characteristics Table - changed <i>Output Duty Cycle</i> test condition and limits. Added Output Pulse Width.	5/25/07
C	T8	15	Remove leaded parts from Ordering Information table	11/15/12
C	4C	5	Corrected typo, VOH: $V_{DD} - 0.45$ to $V_{DDOX} - 0.45$	3/28/13
C	T8	15	Ordering Information - updated part marking. Updated data sheet format.	3/23/15





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