

**FEATURES:**

- Guaranteed Low Skew < 40ps (max)
- Very low duty cycle distortion < 125ps (max)
- High speed propagation delay < 1.75ns (max)
- Additive phase jitter, RMS 0.159ps (typical) @ 125MHz
- Up to 1GHz operation
- Selectable inputs
- Hot insertable and over-voltage tolerant inputs
- 3.3V / 2.5V LVTTTL, HSTL, eHSTL, LVEPECL (2.5V), LVPECL (3.3V), CML, or LVDS input interface
- Selectable differential inputs to six LVDS outputs
- Power-down mode
- 2.5V VDD
- Available in VFQFPN package

**APPLICATIONS:**

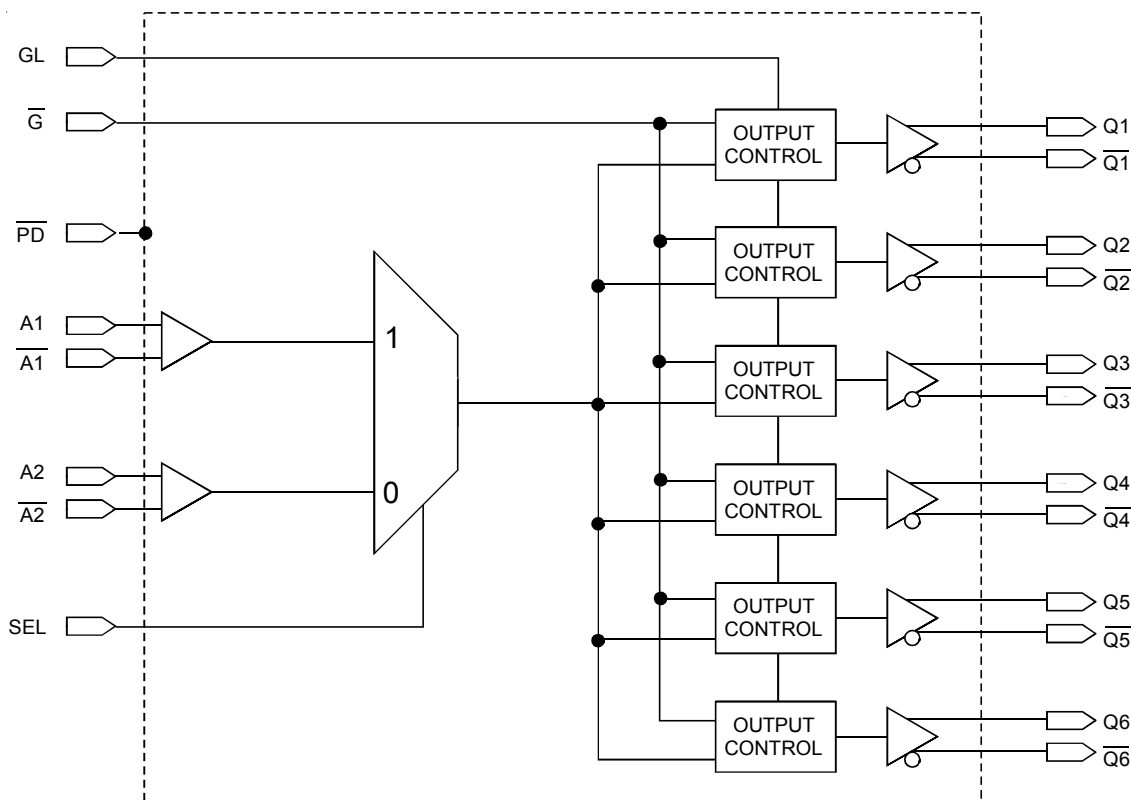
- Clock distribution

**DESCRIPTION:**

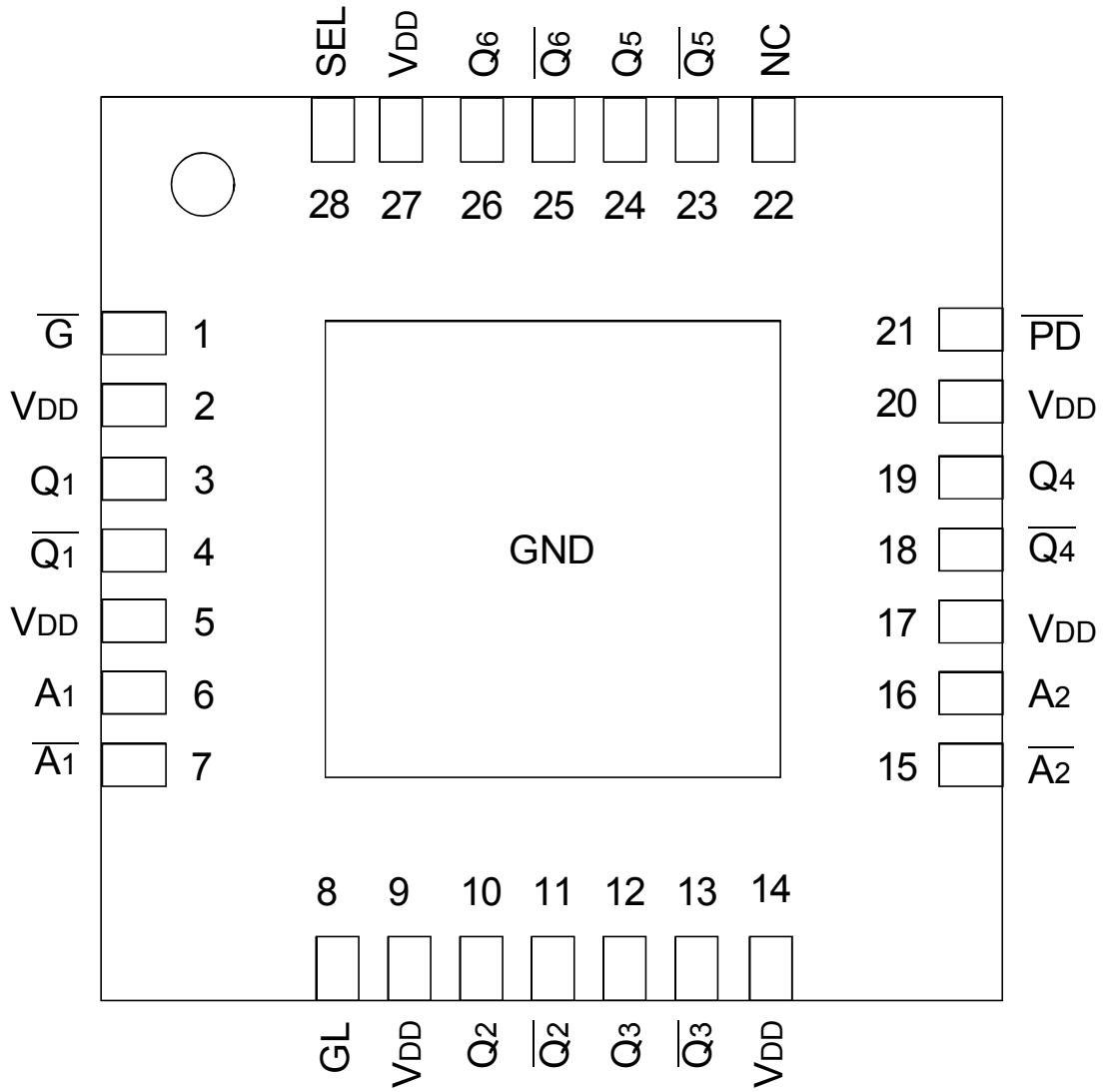
The IDT5T9306 2.5V differential clock buffer is a user-selectable differential input to six LVDS outputs. The fanout from a differential input to six LVDS outputs reduces loading on the preceding driver and provides an efficient clock distribution network. The IDT5T9306 can act as a translator from a differential HSTL, eHSTL, LVEPECL (2.5V), LVPECL (3.3V), CML, or LVDS input to LVDS outputs. A single-ended 3.3V / 2.5V LVTTTL input can also be used to translate to LVDS outputs. The redundant input capability allows for an asynchronous change-over from a primary clock source to a secondary clock source. Selectable reference inputs are controlled by SEL.

The IDT5T9306 outputs can be asynchronously enabled/disabled. When disabled, the outputs will drive to the value selected by the GL pin. Multiple power and grounds reduce noise.

**FUNCTIONAL BLOCK DIAGRAM**



PIN CONFIGURATION



VFQFPN  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
V <sub>DD</sub>	Power Supply Voltage	-0.5 to +3.6	V
V <sub>I</sub>	Input Voltage	-0.5 to +3.6	V
V <sub>O</sub>	Output Voltage <sup>(2)</sup>	-0.5 to V <sub>DD</sub> +0.5	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
T <sub>J</sub>	Junction Temperature	150	°C

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Not to exceed 3.6V.

## CAPACITANCE<sup>(1)</sup> (T<sub>A</sub> = +25°C, F = 1.0MHz)

Symbol	Parameter	Min	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	—	—	3	pF

### NOTE:

- This parameter is measured at characterization but not tested

## RECOMMENDED OPERATING RANGE

Symbol	Description	Min.	Typ.	Max.	Unit
T <sub>A</sub>	Ambient Operating Temperature	-40	+25	+85	°C
V <sub>DD</sub>	Internal Power Supply Voltage	2.3	2.5	2.7	V

## PIN DESCRIPTION

Symbol	I/O	Type	Description
A <sub>[1:2]</sub>	I	Adjustable <sup>(1,4)</sup>	Clock input. A <sub>[1:2]</sub> is the "true" side of the differential clock input.
$\bar{A}$ <sub>[1:2]</sub>	I	Adjustable <sup>(1,4)</sup>	Complementary clock inputs. $\bar{A}$ <sub>[1:2]</sub> is the complementary side of A <sub>[1:2]</sub> . For LVTTTL single-ended operation, $\bar{A}$ <sub>[1:2]</sub> should be set to the desired toggle voltage for A <sub>[1:2]</sub> : 3.3V LVTTTL V <sub>REF</sub> = 1650mV 2.5V LVTTTL V <sub>REF</sub> = 1250mV
$\bar{G}$	I	LVTTTL	Gate control for differential outputs Q <sub>1</sub> and $\bar{Q}$ <sub>1</sub> through Q <sub>6</sub> and $\bar{Q}$ <sub>6</sub> . When $\bar{G}$ is LOW, the differential outputs are active. When $\bar{G}$ is HIGH, the differential outputs are asynchronously driven to the level designated by GL <sup>(2)</sup> .
GL	I	LVTTTL	Specifies output disable level. If HIGH, "true" outputs disable HIGH and "complementary" outputs disable LOW. If LOW, "true" outputs disable LOW and "complementary" outputs disable HIGH.
Q <sub>n</sub>	O	LVDS	Clock outputs
$\bar{Q}$ <sub>n</sub>	O	LVDS	Complementary clock outputs
SEL	I	LVTTTL	Reference clock select. When LOW, selects A <sub>2</sub> and $\bar{A}$ <sub>2</sub> . When HIGH, selects A <sub>1</sub> and $\bar{A}$ <sub>1</sub> .
$\bar{P}$ <sub>D</sub>	I	LVTTTL	Power-down control. Shuts off entire chip. If LOW, the device goes into low power mode. Inputs and outputs are disabled. Both "true" and "complementary" outputs will pull to V <sub>DD</sub> . Set HIGH for normal operation. <sup>(3)</sup>
V <sub>DD</sub>		PWR	Power supply for the device core and inputs
GND		PWR	Power supply return for all power
NC			No connect; recommended to connect to GND

### NOTES:

- Inputs are capable of translating the following interface standards:
  - Single-ended 3.3V and 2.5V LVTTTL levels
  - Differential HSTL and eHSTL levels
  - Differential LVEPECL (2.5V) and LVPECL (3.3V) levels
  - Differential LVDS levels
  - Differential CML levels
- Because the gate controls are asynchronous, runt pulses are possible. It is the user's responsibility to either time the gate control signals to minimize the possibility of runt pulses or be able to tolerate them in down stream circuitry.
- It is recommended that the outputs be disabled before entering power-down mode. It is also recommended that the outputs remain disabled until the device completes power-up after asserting  $\bar{P}$ <sub>D</sub>.
- The user must take precautions with any differential input interface standard being used in order to prevent instability when there is no input signal.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR LVTTTL<sup>(1)</sup>

Symbol	Parameter	Test Conditions	Min.	Typ. <sup>(2)</sup>	Max	Unit
<b>Input Characteristics</b>						
I <sub>IH</sub>	Input HIGH Current	V <sub>DD</sub> = 2.7V	—	—	±5	μA
I <sub>IL</sub>	Input LOW Current	V <sub>DD</sub> = 2.7V	—	—	±5	
V <sub>IK</sub>	Clamp Diode Voltage	V <sub>DD</sub> = 2.3V, I <sub>IN</sub> = -18mA	—	-0.7	-1.2	V
V <sub>IN</sub>	DC Input Voltage		-0.3	—	+3.6	V
V <sub>IH</sub>	DC Input HIGH		1.7	—	—	V
V <sub>IL</sub>	DC Input LOW		—	—	0.7	V
V <sub>THI</sub>	DC Input Threshold Crossing Voltage		—	V <sub>DD</sub> / 2	—	V
V <sub>REF</sub>	Single-Ended Reference Voltage <sup>(3)</sup>	3.3V LVTTTL	—	1.65	—	V
		2.5V LVTTTL	—	1.25	—	

**NOTES:**

1. See RECOMMENDED OPERATING RANGE table.
2. Typical values are at V<sub>DD</sub> = 2.5V, +25°C ambient.
3. For A<sub>[1:2]</sub> single-ended operation,  $\bar{A}_{[1:2]}$  is tied to a DC reference voltage.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR DIFFERENTIAL INPUTS<sup>(1)</sup>

Symbol	Parameter	Test Conditions	Min.	Typ. <sup>(2)</sup>	Max	Unit
<b>Input Characteristics</b>						
I <sub>IH</sub>	Input HIGH Current	V <sub>DD</sub> = 2.7V	—	—	±5	μA
I <sub>IL</sub>	Input LOW Current	V <sub>DD</sub> = 2.7V	—	—	±5	
V <sub>IK</sub>	Clamp Diode Voltage	V <sub>DD</sub> = 2.3V, I <sub>IN</sub> = -18mA	—	-0.7	-1.2	V
V <sub>IN</sub>	DC Input Voltage		-0.3	—	+3.6	V
V <sub>DIF</sub>	DC Differential Voltage <sup>(3)</sup>		0.1	—	—	V
V <sub>CM</sub>	DC Common Mode Input Voltage <sup>(4)</sup>		0.05	—	V <sub>DD</sub>	V

**NOTES:**

1. See RECOMMENDED OPERATING RANGE table.
2. Typical values are at V<sub>DD</sub> = 2.5V, +25°C ambient.
3. V<sub>DIF</sub> specifies the minimum input differential voltage (V<sub>TR</sub> - V<sub>CP</sub>) required for switching where V<sub>TR</sub> is the "true" input level and V<sub>CP</sub> is the "complement" input level. The DC differential voltage must be maintained to guarantee retaining the existing HIGH or LOW input. The AC differential voltage must be achieved to guarantee switching to a new state.
4. V<sub>CM</sub> specifies the maximum allowable range of (V<sub>TR</sub> + V<sub>CP</sub>) / 2.

## DC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING RANGE FOR LVDS<sup>(1)</sup>

Symbol	Parameter	Test Conditions	Min.	Typ. <sup>(2)</sup>	Max	Unit
<b>Output Characteristics</b>						
V <sub>OT(+)</sub>	Differential Output Voltage for the True Binary State		247	—	454	mV
V <sub>OT(-)</sub>	Differential Output Voltage for the False Binary State		247	—	454	mV
ΔV <sub>OT</sub>	Change in V <sub>OT</sub> Between Complementary Output States		—	—	50	mV
V <sub>OS</sub>	Output Common Mode Voltage (Offset Voltage)		1.125	1.2	1.375	V
ΔV <sub>OS</sub>	Change in V <sub>OS</sub> Between Complementary Output States		—	—	50	mV
I <sub>OS</sub>	Outputs Short Circuit Current	V <sub>OUT+</sub> and V <sub>OUT-</sub> = 0V	—	12	24	mA
I <sub>OSD</sub>	Differential Outputs Short Circuit Current	V <sub>OUT+</sub> = V <sub>OUT-</sub>	—	6	12	mA

**NOTES:**

1. See RECOMMENDED OPERATING RANGE table.
2. Typical values are at V<sub>DD</sub> = 2.5V, T<sub>A</sub> = +25°C ambient.

## DIFFERENTIAL INPUT AC TEST CONDITIONS FOR HSTL

Symbol	Parameter	Value	Units
V <sub>DIF</sub>	Input Signal Swing <sup>(1)</sup>	1	V
V <sub>X</sub>	Differential Input Signal Crossing Point <sup>(2)</sup>	750	mV
D <sub>H</sub>	Duty Cycle	50	%
V <sub>THI</sub>	Input Timing Measurement Reference Level <sup>(3)</sup>	Crossing Point	V
t <sub>R</sub> , t <sub>F</sub>	Input Signal Edge Rate <sup>(4)</sup>	2	V/ns

### NOTES:

1. The 1V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V<sub>DIF</sub> (AC) specification under actual use conditions.
2. A 750mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V<sub>X</sub> specification under actual use conditions.
3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.
4. The input signal edge rate of 2V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

## DIFFERENTIAL INPUT AC TEST CONDITIONS FOR eHSTL

Symbol	Parameter	Value	Units
V <sub>DIF</sub>	Input Signal Swing <sup>(1)</sup>	1	V
V <sub>X</sub>	Differential Input Signal Crossing Point <sup>(2)</sup>	900	mV
D <sub>H</sub>	Duty Cycle	50	%
V <sub>THI</sub>	Input Timing Measurement Reference Level <sup>(3)</sup>	Crossing Point	V
t <sub>R</sub> , t <sub>F</sub>	Input Signal Edge Rate <sup>(4)</sup>	2	V/ns

### NOTES:

1. The 1V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V<sub>DIF</sub> (AC) specification under actual use conditions.
2. A 900mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V<sub>X</sub> specification under actual use conditions.
3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.
4. The input signal edge rate of 2V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

## DIFFERENTIAL INPUT AC TEST CONDITIONS FOR LVEPECL (2.5V) AND LVPECL (3.3V)

Symbol	Parameter	Value	Units
V <sub>DIF</sub>	Input Signal Swing <sup>(1)</sup>	732	mV
V <sub>X</sub>	Differential Input Signal Crossing Point <sup>(2)</sup>	LVEPECL	1082
		LVPECL	1880
D <sub>H</sub>	Duty Cycle	50	%
V <sub>THI</sub>	Input Timing Measurement Reference Level <sup>(3)</sup>	Crossing Point	V
t <sub>R</sub> , t <sub>F</sub>	Input Signal Edge Rate <sup>(4)</sup>	2	V/ns

### NOTES:

1. The 732mV peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V<sub>DIF</sub> (AC) specification under actual use conditions.
2. 1082mV LVEPECL (2.5V) and 1880mV LVPECL (3.3V) crossing point levels are specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V<sub>X</sub> specification under actual use conditions.
3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.
4. The input signal edge rate of 2V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

## DIFFERENTIAL INPUT AC TEST CONDITIONS FOR LVDS

Symbol	Parameter	Value	Units
V <sub>DIF</sub>	Input Signal Swing <sup>(1)</sup>	400	mV
V <sub>X</sub>	Differential Input Signal Crossing Point <sup>(2)</sup>	1.2	V
D <sub>H</sub>	Duty Cycle	50	%
V <sub>THI</sub>	Input Timing Measurement Reference Level <sup>(3)</sup>	Crossing Point	V
t <sub>R</sub> , t <sub>F</sub>	Input Signal Edge Rate <sup>(4)</sup>	2	V/ns

### NOTES:

1. The 400mV peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V<sub>DIF</sub> (AC) specification under actual use conditions.
2. A 1.2V crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V<sub>X</sub> specification under actual use conditions.
3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.
4. The input signal edge rate of 2V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

## AC DIFFERENTIAL INPUT SPECIFICATIONS<sup>(1)</sup>

Symbol	Parameter	Min.	Typ.	Max	Unit
V <sub>DIF</sub>	AC Differential Voltage <sup>(2)</sup>	0.1	—	3.6	V
V <sub>IX</sub>	Differential Input Crosspoint Voltage	0.05	—	V <sub>DD</sub>	V
V <sub>CM</sub>	Common Mode Input Voltage Range <sup>(3)</sup>	0.05	—	V <sub>DD</sub>	V
V <sub>IN</sub>	Input Voltage	-0.3		+3.6	V

### NOTES:

1. The output will not change state until the inputs have crossed and the minimum differential voltage range defined by V<sub>DIF</sub> has been met or exceeded.
2. V<sub>DIF</sub> specifies the minimum input voltage (V<sub>TR</sub> - V<sub>CP</sub>) required for switching where V<sub>TR</sub> is the "true" input level and V<sub>CP</sub> is the "complement" input level. The AC differential voltage must be achieved to guarantee switching to a new state.
3. V<sub>CM</sub> specifies the maximum allowable range of (V<sub>TR</sub> + V<sub>CP</sub>) / 2.

## POWER SUPPLY CHARACTERISTICS FOR LVDS OUTPUTS<sup>(1)</sup>

Symbol	Parameter	Test Conditions	Typ.	Max	Unit
I <sub>DDQ</sub>	Quiescent V <sub>DD</sub> Power Supply Current	V <sub>DD</sub> = Max., All Input Clocks = LOW <sup>(2)</sup> Outputs enabled	—	240	mA
I <sub>TOT</sub>	Total Power V <sub>DD</sub> Supply Current	V <sub>DD</sub> = 2.7V., F <sub>REFERENCE CLOCK</sub> = 1GHz	—	250	mA
I <sub>PD</sub>	Total Power Down Supply Current	$\overline{PD}$ = LOW	—	5	mA

### NOTES:

1. These power consumption characteristics are for all the valid input interfaces and cover the worst case conditions.
2. The true input is held LOW and the complementary input is held HIGH.

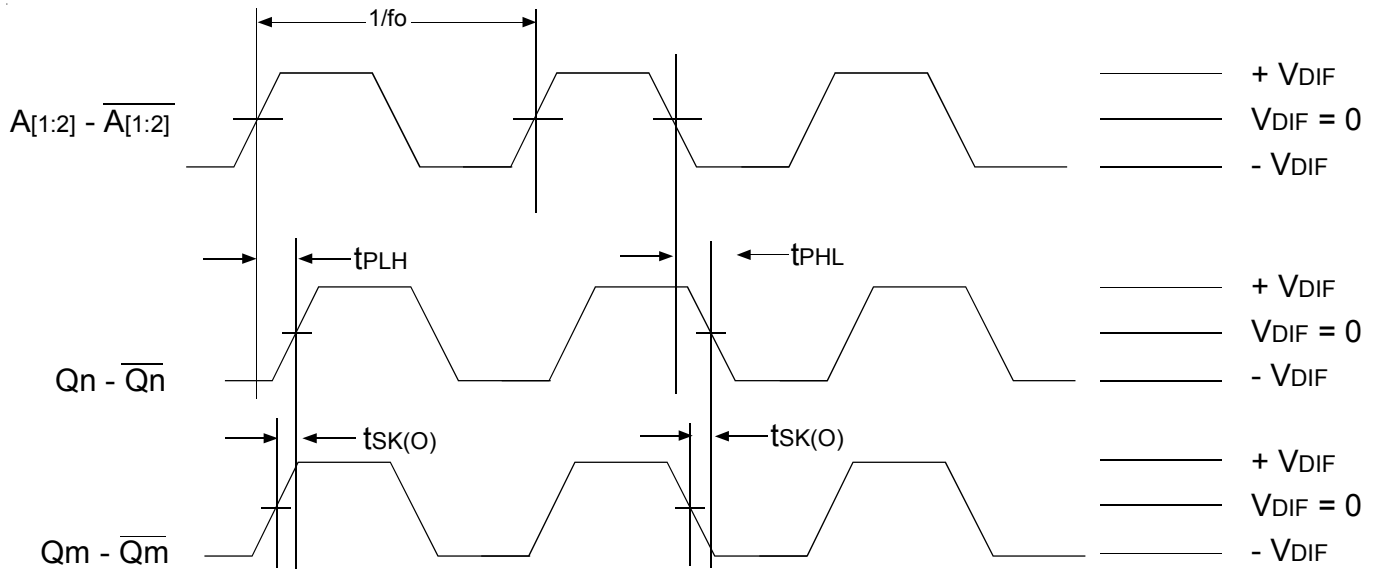
## AC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE<sup>(1,5)</sup>

Symbol	Parameter	Min.	Typ.	Max	Unit
<b>Skew Parameters</b>					
$t_{SK(O)}$	Same Device Output Pin-to-Pin Skew <sup>(2)</sup>	—	—	40	ps
$t_{SK(P)}$	Pulse Skew <sup>(3)</sup>	—	—	125	ps
$t_{SK(PP)}$	Part-to-Part Skew <sup>(4)</sup>	—	—	300	ps
<b>Propagation Delay</b>					
$t_{PLH}$	Propagation Delay A, $\bar{A}$ Crosspoint to $Q_n$ , $\bar{Q}_n$ Crosspoint	—	1.25	1.75	ns
$t_{PHL}$					
$f_o$	Frequency Range <sup>(6)</sup>	—	—	1	GHz
<b>Output Gate Enable/Disable Delay</b>					
$t_{PGE}$	Output Gate Enable Crossing $V_{THI}$ to $Q_n/\bar{Q}_n$ Crosspoint	—	—	3.5	ns
$t_{PGD}$	Output Gate Disable Crossing $V_{THI}$ to $Q_n/\bar{Q}_n$ Crosspoint Driven to GL Designated Level	—	—	3.5	ns
<b>Power Down Timing</b>					
$t_{PWRDN}$	$\bar{P}\bar{D}$ Crossing $V_{THI}$ to $Q_n = V_{DD}$ , $\bar{Q}_n = V_{DD}$	—	—	100	$\mu$ S
$t_{PWRUP}$	Output Gate Disable Crossing $V_{THI}$ to $Q_n/\bar{Q}_n$ Driven to GL Designated Level	—	—	100	$\mu$ S
<b>RMS Additive Phase Jitter</b>					
$t_{JIT}$	RMS Additive Phase Jitter @ 25MHz (12kHz – 10MHz Integration Range)		0.541		ps
	RMS Additive Phase Jitter @ 125MHz (12kHz – 20MHz Integration Range)		0.159		ps
	RMS Additive Phase Jitter @ 156.25MHz (12kHz – 20MHz Integration Range)		0.185		ps
<b>Output Rise/Fall Time</b>					
$t_{R}/t_{F}$	Output Rise/Fall Time <sup>(6)</sup> , (20% - 80%)	125		600	ps

### NOTES:

1. AC propagation measurements should not be taken within the first 100 cycles of startup.
2. Skew measured between crosspoints of all differential output pairs under identical input and output interfaces, transitions and load conditions on any one device.
3. Skew measured is the difference between propagation delay times  $t_{PHL}$  and  $t_{PLH}$  of any differential output pair under identical input and output interfaces, transitions and load conditions on any one device.
4. Skew measured is the magnitude of the difference in propagation times between any single differential output pair of two devices, given identical transitions and load conditions at identical  $V_{DD}$  levels and temperature.
5. All parameters are tested with a 50% input duty cycle.
6. Guaranteed by design but not production tested.

DIFFERENTIAL AC TIMING WAVEFORMS



Output Propagation and Skew Waveforms

NOTES:

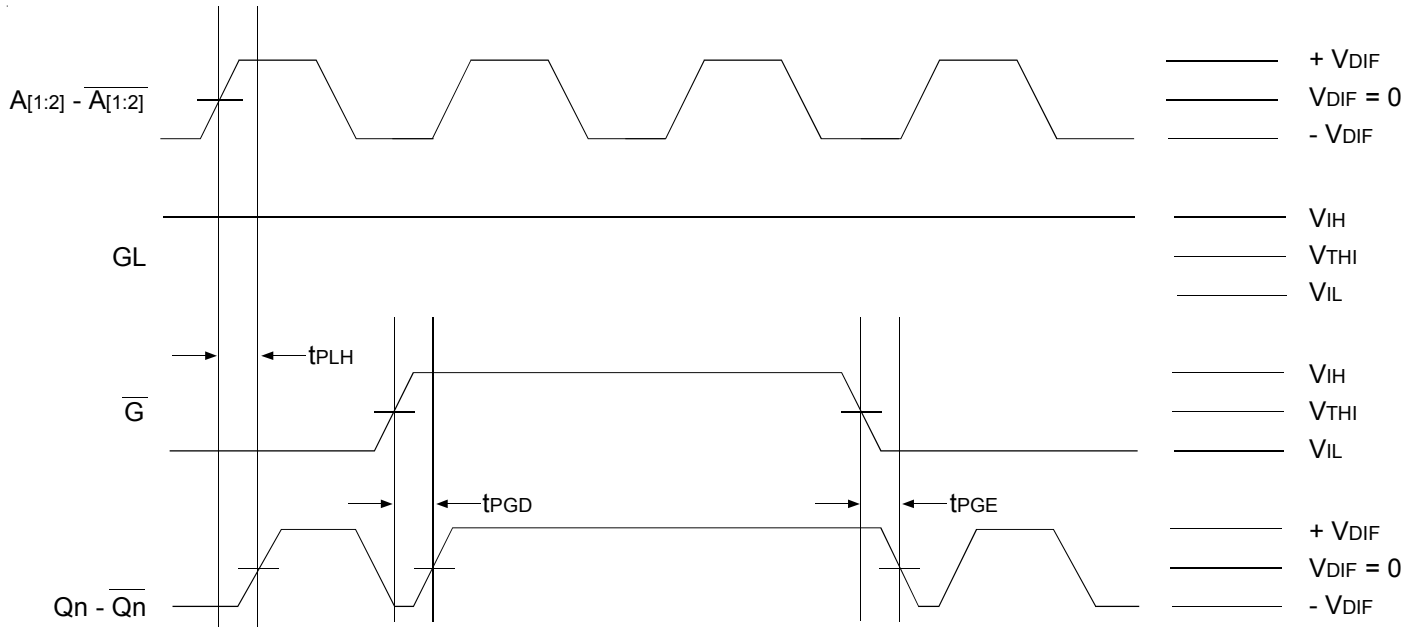
1. Pulse skew is calculated using the following expression:

$$t_{SK(P)} = |t_{PHL} - t_{PLH}|$$

Note that the tPHL and tPLH shown above are not valid measurements for this calculation because they are not taken from the same pulse.

2. AC propagation measurements should not be taken within the first 100 cycles of startup.

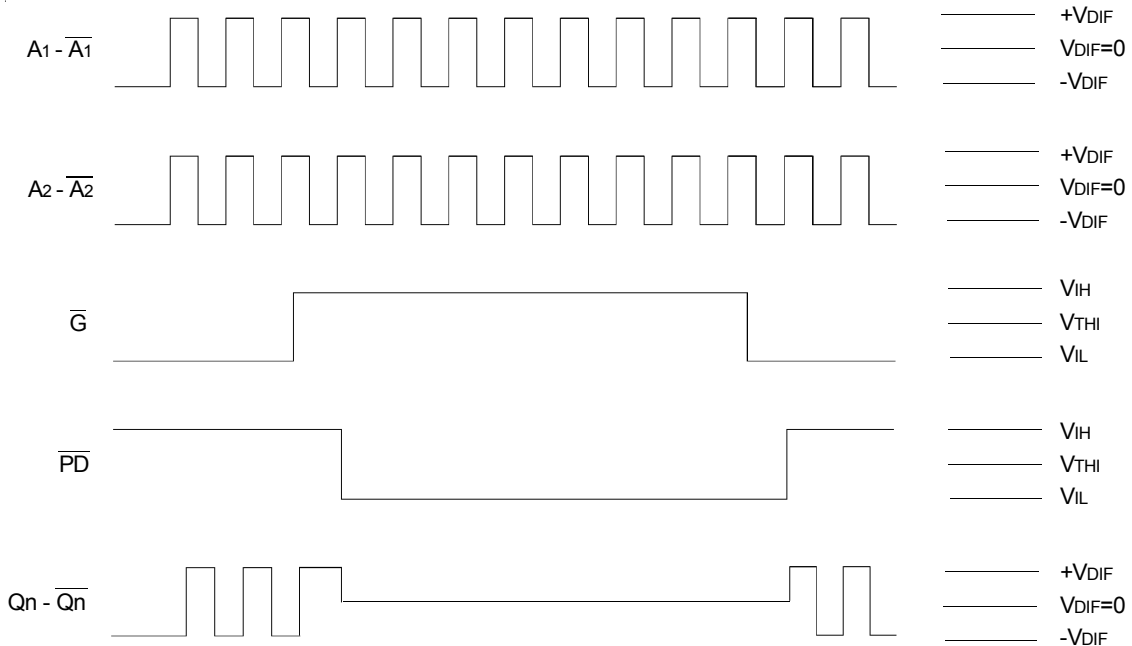




**Differential Gate Disable/Enable Showing Runt Pulse Generation**

**NOTE:**

1. As shown, it is possible to generate runt pulses on gate disable and enable of the outputs. It is the user's responsibility to time the  $\overline{G}$  signal to avoid this problem.

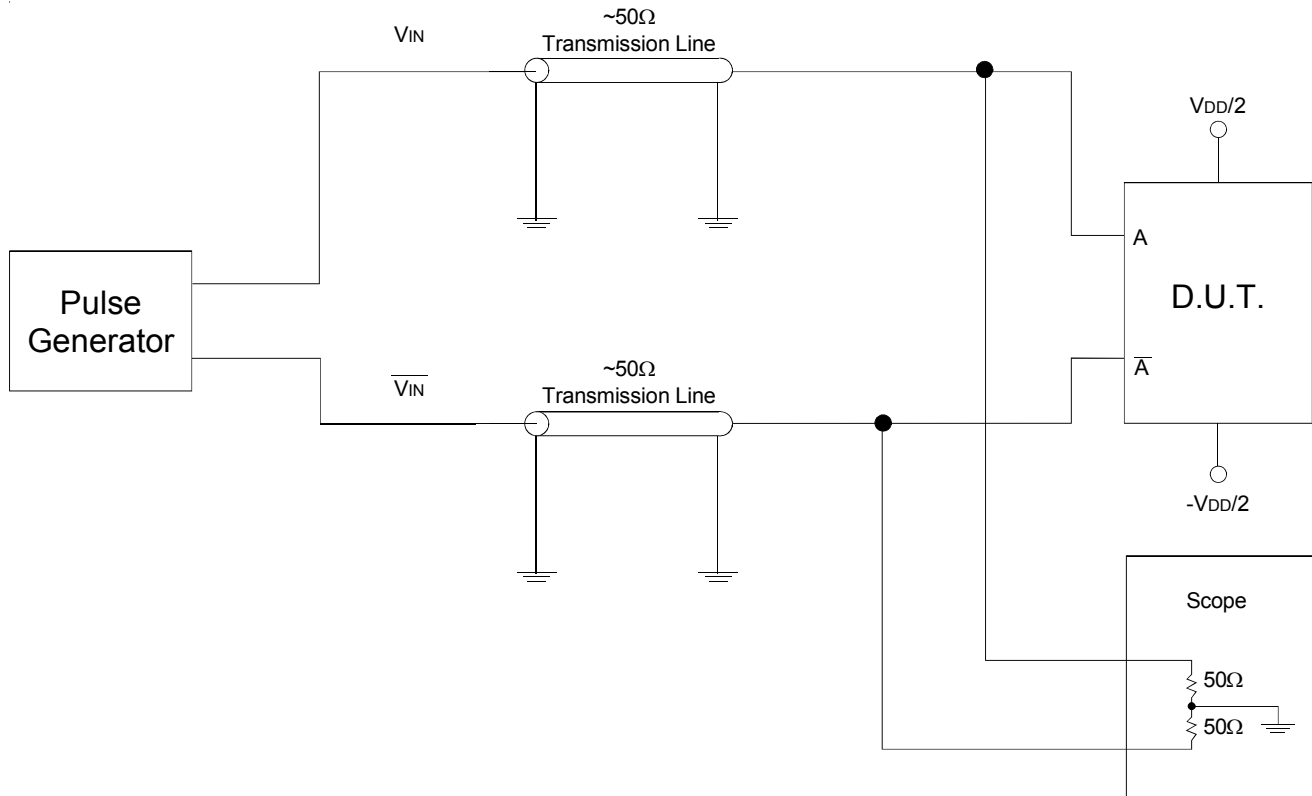


**Power Down Timing**

**NOTES:**

1. It is recommended that outputs be disabled before entering power-down mode. It is also recommended that the outputs remain disabled until the device completes power-up after asserting  $\overline{PD}$ .
2. The POWER DOWN TIMING diagram assumes that  $GL$  is HIGH.
3. It should be noted that during power-down mode, the outputs are both pulled to  $V_{DD}$ . In the POWER DOWN TIMING diagram this is shown when  $Q_n - \overline{Q_n}$  goes to  $V_{DIF} = 0$ .

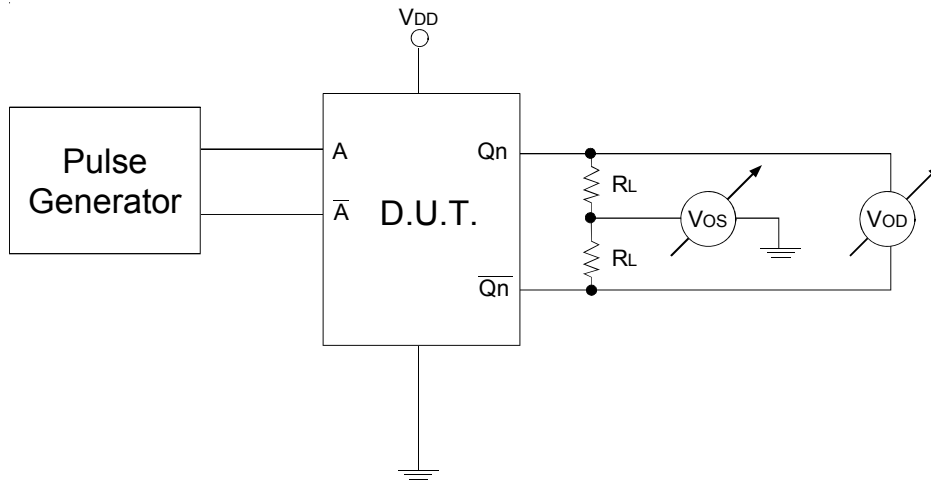
TEST CIRCUITS AND CONDITIONS



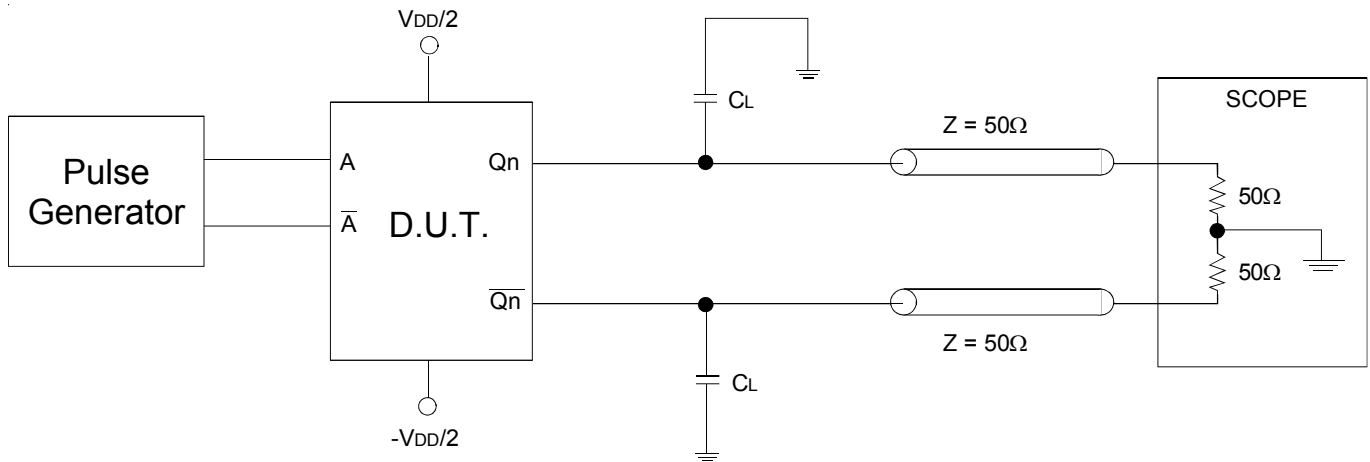
Test Circuit for Differential Input

DIFFERENTIAL INPUT TEST CONDITIONS

Symbol	$V_{DD} = 2.5V \pm 0.2V$	Unit
$V_{THI}$	Crossing of A and $\overline{A}$	V



Test Circuit for DC Outputs and Power Down Tests



Test Circuit for Propagation, Skew, and Gate Enable/Disable Timing

LVDS OUTPUT TEST CONDITION

Symbol	$V_{DD} = 2.5V \pm 0.2V$	Unit
$C_L$	0 <sup>(1)</sup>	pF
	8 <sup>(1,2)</sup>	
$R_L$	50	$\Omega$

NOTES:

1. Specifications only apply to "Normal Operations" test condition. The  $T_{IA}/E_{IA}$  specification load is for reference only.
2. The scope inputs are assumed to have a 2pF load to ground.  $T_{IA}/E_{IA}$  - 644 specifies 5pF between the output pair. With  $C_L = 8pF$ , this gives the test circuit appropriate 5pF equivalent load.

## VFQFPN EPAD THERMAL RELEASE PATH

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 1*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground

through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

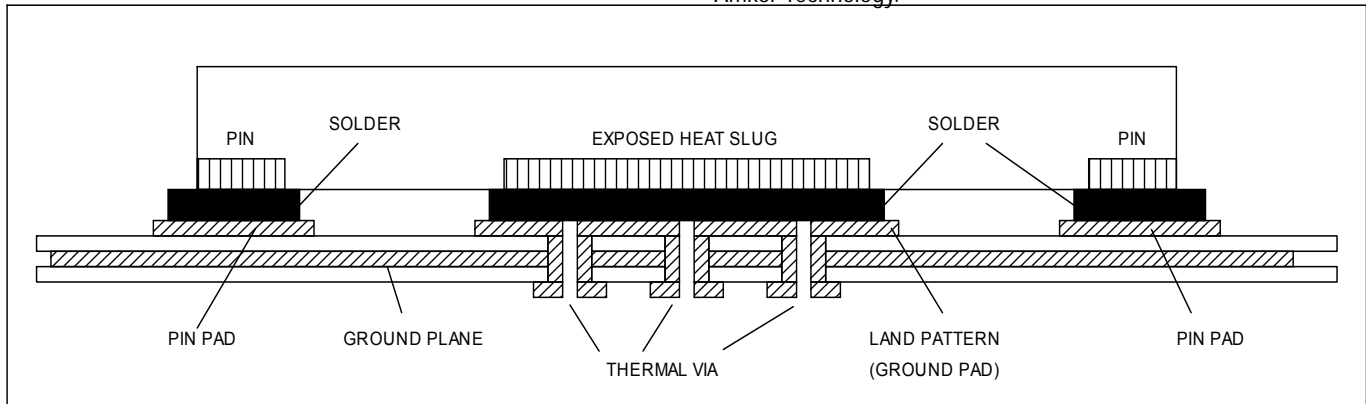


FIGURE 1. P.C.ASSEMBLY FOR EXPOSED PAD THERMAL RELEASE PATH –SIDE VIEW (DRAWING NOT TO SCALE)

## SCHEMATIC LAYOUT

Figure 2 shows an example of IDT5T9306 schematic. In this example, the device is operated at  $V_{DD} = 2.5V$ . As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the  $0.1\mu F$  capacitor in each power pin filter should be placed on the device side of the PCB and the other components can be placed on the opposite side.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the

devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set.

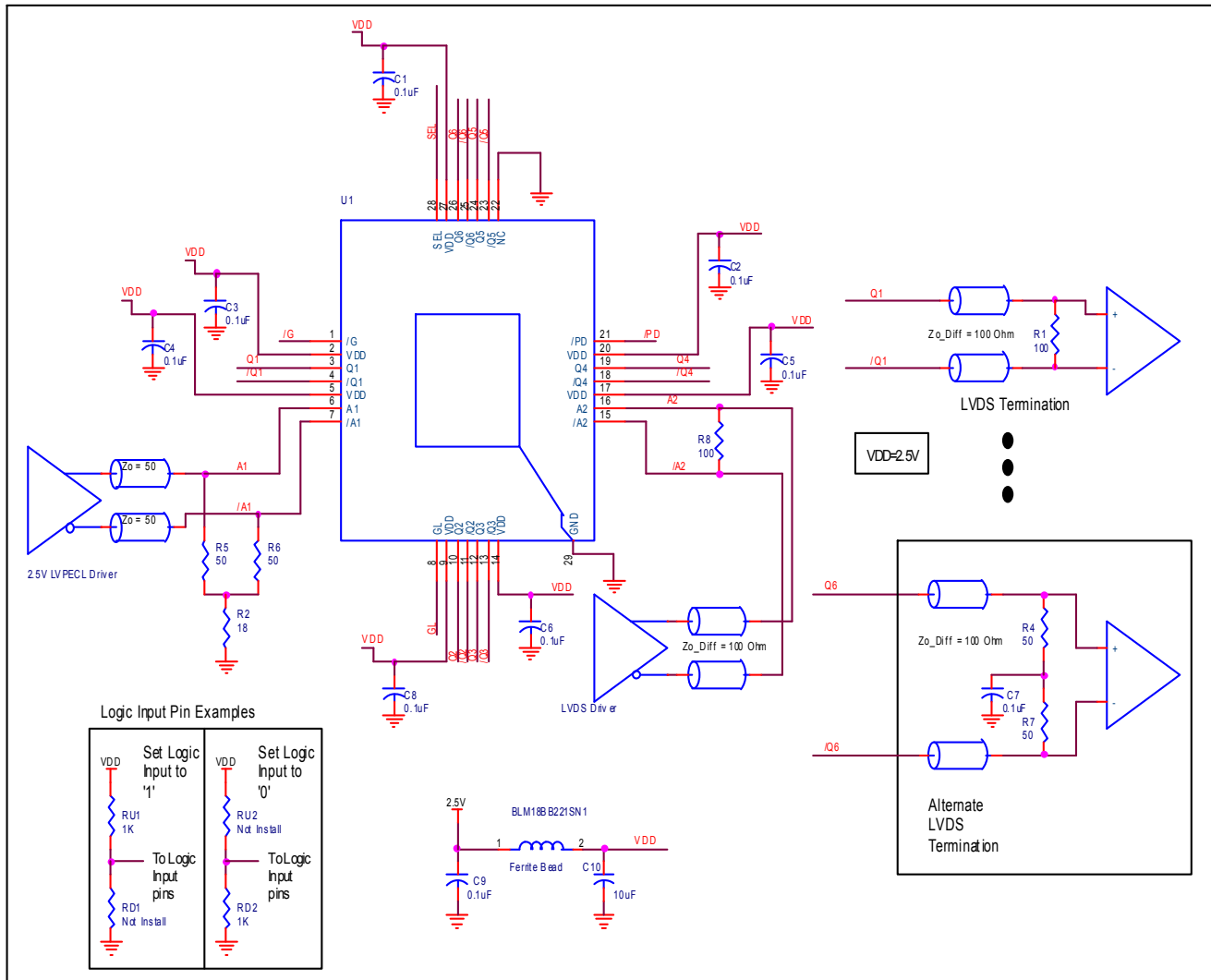
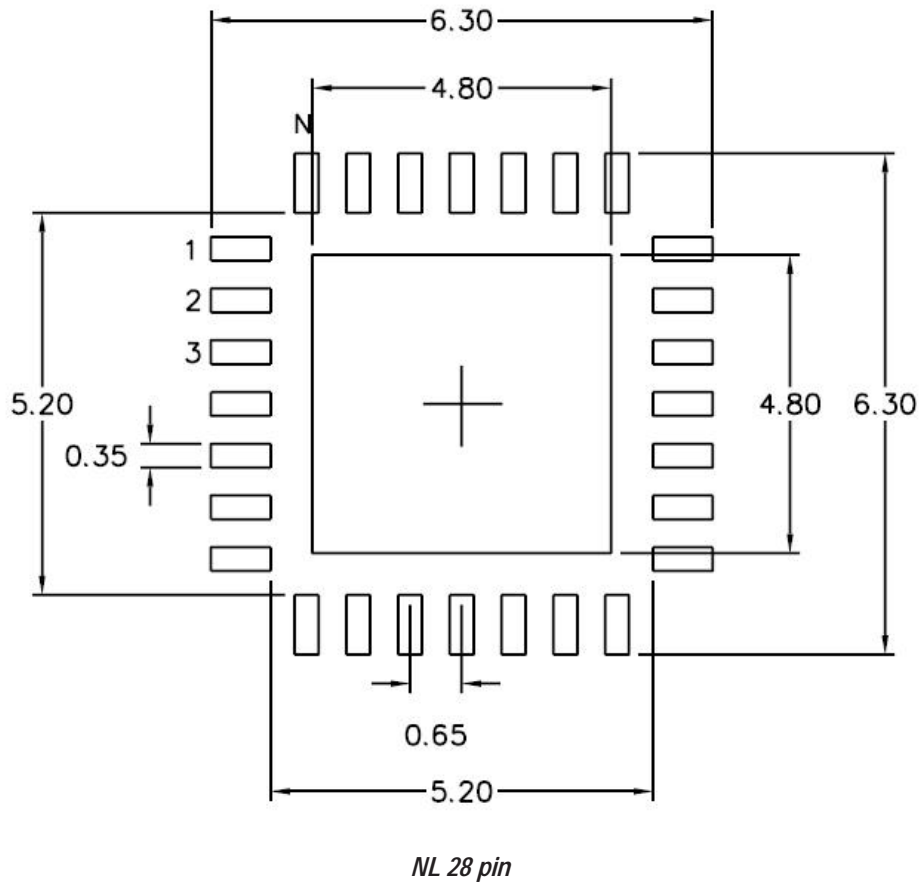


FIGURE 2. IDT5T3906 SCHEMATIC EXAMPLE

RECOMMENDED LANDING PATTERN

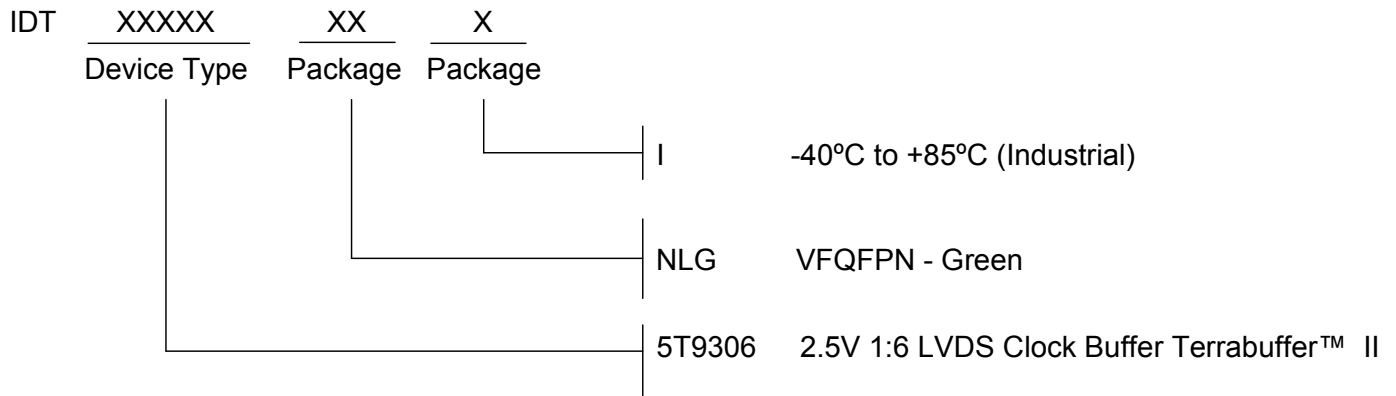


NOTE: All dimensions are in millimeters.

REVISION HISTORY SHEET

July 23, 2002	Datasheet creation
October 8, 2002	Page 1, entire page changed; page 2, both diagrams; page 3, Pin Description and notes; page 4, DC Cha. for LVPECL and Differential Input tables; page 6, DC Cha. and Power Supply tables; page 7, entire page; page 9, added note 3; page 10, entire page; page 11, entire page; page 12, Ordering Info; added 3 new pages (10 thru 12) of diagrams.
October 10, 2002	Page 1, entire page changed; page 2, both diagrams; page 3, Pin Description and notes; page 7, AC Cha. table; page 8, added new LVPECL table; page 10, removed Input Clock Switching diagram; page 11, deleted entire page; page 12, changed Power Down Timing; page 15, Ordering Info.
October 24, 2002	Page 2, added note 1 to TQFP TOP VIEW text; page 3, added note 4 to Pin Description; page 4, replaced "Compliant devices must meet" with the text "This device meets" in four instances; page 5, Differential Input table, note 1, changed 1V to 732mV and replaced "Compliant devices must meet" with the text "This device meets"; page 6, DC Electrical table, Vdif row, changed Min. value to 0.1, and under Differential Input table replaced "Compliant devices must meet" with the text "This device meets" page 7, Power Supply table, replaced ((TBD)) with 800MHz, and under AC Electrical table, replaced ((TBD)) with 500; page 8, completely altered AC Differential table; page 12, LVDS Output table, replaced ((TBD)) with 3.
November 1, 2002	Radical changes to entire document.
December 12, 2002	Radical changes to entire document, using 5T9316 as a base.
December 16, 2002	Throughout document, removed "Differential" from title; page 7, Power Supply table, changed Max values, changed REFERENCE value; page 10, note 1, changed $\bar{G}_x$ to $\bar{G}$ .
May 8, 2003	Page 2, corrected pinout diagram.
August 7, 2003	Page 1, Features text, 3rd bullet, changed 2ns to 1.75ns, 4th bullet, changed 800MHz to 1GHz, and 7th bullet, added CML, on Description, 3rd line, added CML to list; page 4, Pin Descr., note 1, added "Differential CML levels", for Description of PD row, replaced 2nd sentence with "Both 'true' and 'complementary' output will pull to Vdd"; page 5, DC... for Differential Inputs table, removed note 5 and changed Vcm Max. from 3.5 to Vdd; page 7, Power Supply table, changed 800MHz to 1GHz; page 8, AC Differential table, changed Vix and Vcm Max specs from 3.5V to Vdd, removed notes 4 and 5, and placed entire table on page 7, for AC Elect. table, added notes 5 and 6, changed ((TBD)) to 300ps, tplh Type to 1.25ns, and Max from 2ns to 1.75ns, and changed fo Max from 800MHz to 1GHz.
October 2, 2003	Page 1, Features, 7th bullet, added "3.3V / 2.5V LVTTTL" to front, Description, added to 1st paragraph "A single-ended 3.3V/2.5V LVTTTL input can also be used to translate to LVDS outputs."; page 4, Pin Description table, added large block of text to 2nd row, added "Single-ended 3.3V and 2.5V LVTTTL levels" to note 1; page 5, DC for LVTTTL table, added Vref row and note 3, for DC for LVDS table, changed los ratings from 5 Typ, 7.5 Max to 12 Typ, 24 Max, and changed losd ratings from 5 Typ, 7.5 Max to 6 Typ, 12 Max; page 7, Power Supply table, changed Ipd from 3 to 5.
March 26, 2004	Page 2, changed pin 22 to NC; page 3, changed pin 25 to NC; page 4, added NC row to Pin Description.
June 22, 2004	Removed TQFP package.
October 26, 2004	Inserted a page before Ordering Info and added Landing Pattern.
October 27, 2004	Added note to Landing Pattern.
October 29, 2004	Changed landing pattern diagram.
March 9, 2005	Page 6, switched Iddq and Itot values.
October 23, 2007	Page 7, added Additive Phase Jitter, RMS specs to the AC Electrical Characterisitcs Table.
April 15, 2008	Page 7, added Rise/Fall Time spec. to the AC Electrical Characteristics Table.
January 31, 2011	Page 12, added VFQFPN Thermal Release Path application note. Updated to header/footer to new format.
March 13, 2012	Page 13, added schematic layout. Page 16, corrected ordering information table.
May 30, 2012	Page 1, Features Section - changed Low Skew spec to <40ps (max) from <25ps. Page 7, AC Charastics Table - tsk(o) Max from 25ps to 40ps.
November 29, 2012	Page 16, Removed leaded parts from Ordering Information

ORDERING INFORMATION







## Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
  - "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
  - "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

## Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

## Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:  
[www.renesas.com/contact/](http://www.renesas.com/contact/)

## Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.