FemtoClock® NG Crystal-to-3.3V, 2.5V LVPECL Clock Generator w/Fanout Buffer

General Description

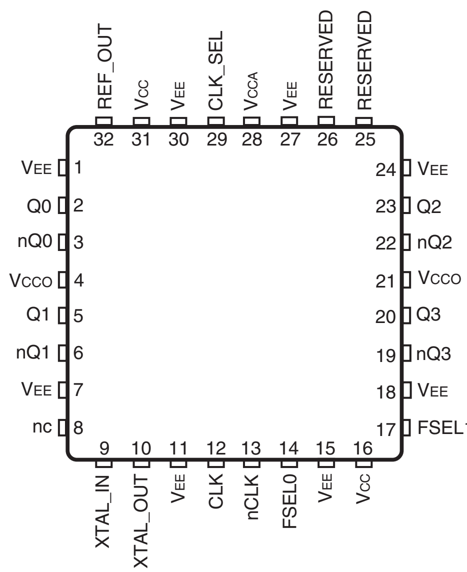
The IDT8V89704I is a four output Clock Generator with LVPECL outputs. The IDT8V89704I can generate any one of four frequencies from a single crystal or reference clock. The four frequencies are selected from the Function Table (Table 3) by two frequency selection pins. Note the desired programmed frequencies must be used with the corresponding crystal as indicated in Table 3.

Excellent phase noise performance is maintained with IDT's Fourth Generation FemtoClock® NG PLL technology.

Features

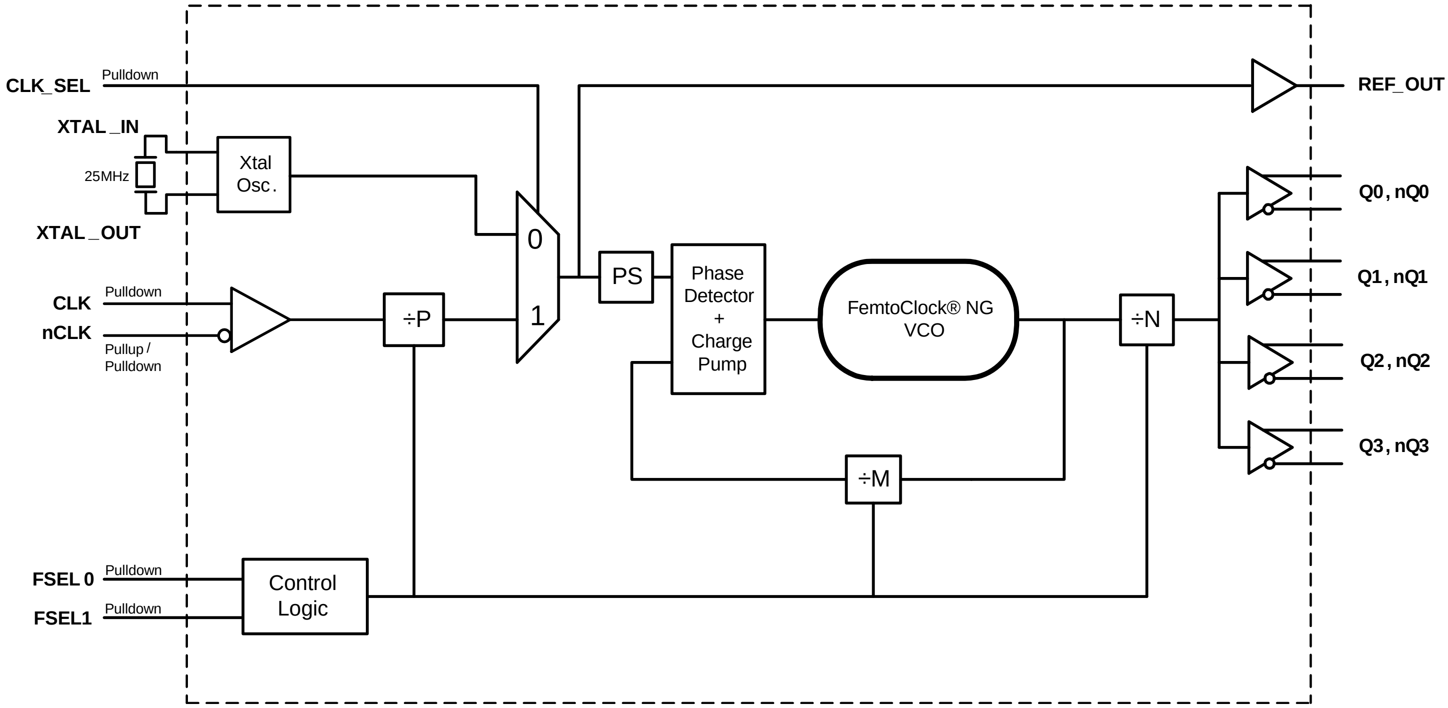
- Fourth Generation FemtoClock® NG PLL technology
- Ideal for 10G EPON ONU and 1G/10G OLT Line Card
- Four LVPECL outputs
- One Reference LVCMOS clock output
- The CLK, nCLK input pair can accept the following differential input levels: LVPECL, LVDS, HCSL
- RMS phase jitter at 156.25MHz (12kHz - 20MHz): 0.239ps (typical)
- Full 2.5V or 3.3V power supply
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) packaging

Pin Assignment



IDT8V89704I
32 Lead VFQFN
5mm x 5mm x 0.925mm package body
3.15mm x 3.15mm EPad
NL Package

Block Diagram



Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 7, 11, 15, 18, 24, 27, 30	V_{EE}	Power		Negative supply pins.
2, 3	Q0, nQ0	Output		Differential output pair. LVPECL interface levels.
4, 21	V_{CCO}	Power		Output supply pins.
5, 6	Q1, nQ1	Output		Differential output pair. LVPECL interface levels.
8	nc	Unused		No connect.
9, 10	XTAL_IN XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output. Crystal frequency is selected from Table 3A.
12	CLK	Input	Pulldown	Non-inverting differential clock input.
13	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input. Internal resistor bias to $V_{CC}/2$.
14, 17	FSEL0, FSEL1	Input	Pulldown	Frequency select pins. LVCMOS/LVTTL interface levels.
16, 31	V_{CC}	Power		Core supply pins.
19, 20	nQ3, Q3	Output		Differential output pair. LVPECL interface levels.
22, 23	nQ2, Q2	Output		Differential output pair. LVPECL interface levels.
25, 26	RESERVED			Reserved.
28	V_{CCA}	Power		Analog supply pin.
29	CLK_SEL	Input	Pulldown	Input source control pin. LVCMOS/LVTTL interface levels.
32	REF_OUT	Output		Single-ended reference output. LVCMOS/LVTTL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

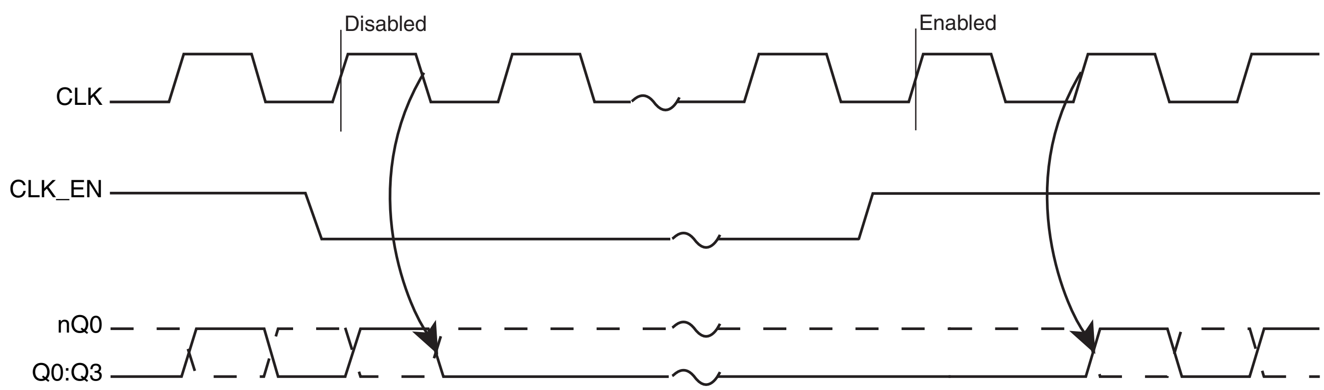
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				2		pF
C_{PD}	Power Dissipation Capacitance				10		pF
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ
R_{PULLUP}	Input Pullup Resistor				51		kΩ
R_{OUT}	Output Impedance	REF_OUT			20		Ω

Function Table

Table 3A. Control Input Function Table

Inputs			Outputs		
CLK_EN	CLK_SEL	Selected Source	Q0	nQ0	Q1:Q3
0	0	CLK	Disabled; LOW	Disabled; HIGH	Disabled; LOW
0	1	XTAL_IN, XTAL_OUT	Disabled; LOW	Disabled; HIGH	Disabled; LOW
1	0	CLK	Enabled	Enabled	Enabled
1	1	XTAL_IN, XTAL_OUT	Enabled	Enabled	Enabled

NOTE: After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock or crystal oscillator edge as shown in Figure 1.
NOTE: In the active mode, the state of the outputs are a function of the CLK input as described in Table 3B.



Frequency Configuration

Table 3B. Frequency Configuration Examples

FSEL1	FSEL0	Output Frequency (MHz)	Input Frequency (MHz)	Input Clock Divider (P)	Input Clock Pre-scale (PS)	M Divider	N Divider	VCO Frequency (MHz)
0 (default)	0 (default)	125	25	1	x2	40	16	2000
0	1	156.25	25	1	x2	50	16	2500
1	0	250	25	1	x2	40	8	2000
1	1	100	25	1	x2	40	20	2000

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	3.6V
Inputs, V_I XTAL_IN Other Input	 0V to 2V -0.5V to V_{CC} + 0.5V
Outputs, V_O (LVCMOS)	-0.5V to V_{CC} + 0.5V
Outputs, I_O (LVPECL) Continuous Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	33.1°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.32	3.3	V_{CC}	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{CCA}	Analog Supply Current			28	32	mA
I_{EE}	Power Supply Current			183	204	mA

Table 4B. Power Supply DC Characteristics, $V_{CC} = V_{CCO} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.375	2.5	2.625	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.15	2.5	V_{CC}	V
V_{CCO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{CCA}	Analog Supply Current			26	30	mA
I_{EE}	Power Supply Current			173	192	mA

Table 4C. LVCMOS/LVTTL DC Characteristics, $V_{CC} = V_{CCO}$ = 3.3V ± 5% or 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	FSEL[1:0], CLK_SEL	V_{CC} = 3.3V	2		V_{CC} + 0.3	V
			V_{CC} = 2.5V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	CLK_SEL	V_{CC} = 3.3V	-0.3		0.8	V
		CLK_SEL	V_{CC} = 2.5V	-0.3		0.7	V
		FSEL[1:0]	V_{CC} = 3.3V or 2.5V	-0.3		0.5	V
I_{IH}	Input High Current	FSEL[1:0], CLK_SEL	$V_{CC} = V_{IN}$ = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	FSEL[1:0], CLK_SEL	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage; NOTE 1	REF_OUT	V_{CCO} = 3.465V	2.6			V
		REF_OUT	V_{CCO} = 2.625V	1.8			V
V_{OL}	Output Low Voltage; NOTE 1	REF_OUT	V_{CCO} = 3.465V or 2.625V			0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{CCO}/2$. In the Parameter Measurement Information Section, see *Output Load Test Circuit Diagrams.*

Table 4D. Differential DC Characteristics, $V_{CC} = V_{CCO}$ = 3.3V ± 5% or 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK, nCLK	$V_{CC} = V_{IN}$ = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	nCLK	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
		CLK	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
V_{PP}	Peak-to-Peak Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1			V_{EE}		V_{EE} – 0.85	V

NOTE 1: Common mode input voltage is at the cross point.

Table 4E. LVPECL DC Characteristics, $V_{CC} = V_{CCO}$ = 3.3V±5% or 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} – 1.1		V_{CCO} – 0.75	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} – 2.0		V_{CCO} – 1.6	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs termination with 50Ω to V_{CCO} – 2V.

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

NOTE: Characterized using an 12pF parallel resonant crystal.

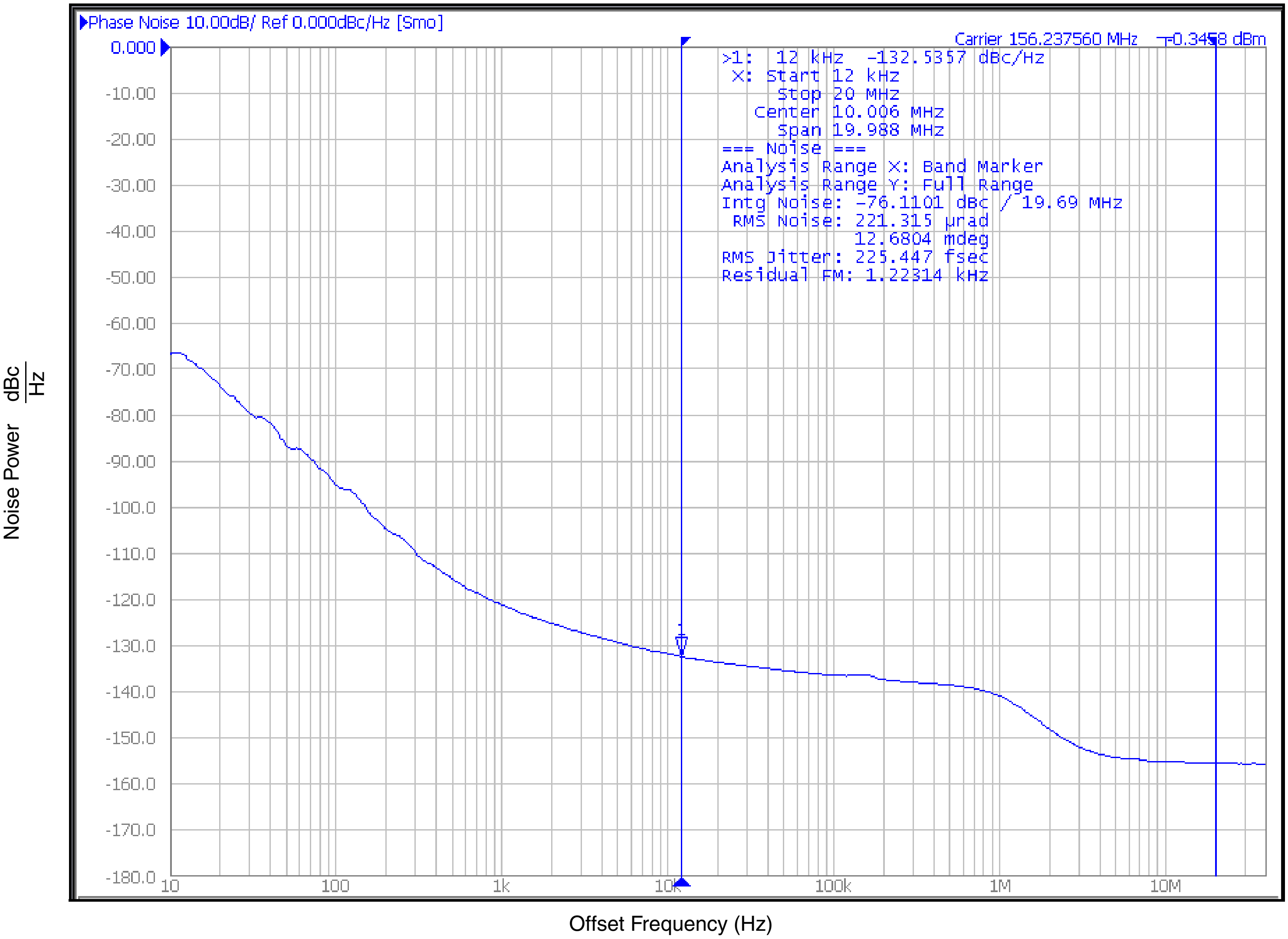
AC Electrical Characteristics

Table 6. AC Characteristics, $V_{CC} = V_{CCO}$ = 3.3V ± 5% or 2.5V ± 5% V_{EE} = 0V, T_A = -40°C to 85°C

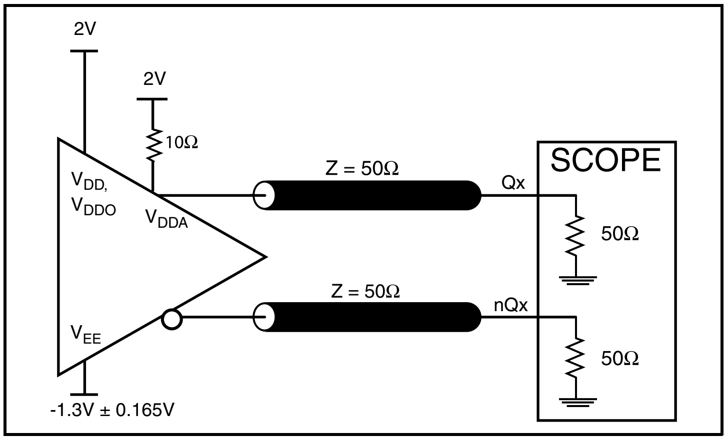
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{DIFF_IN}	Differential Input Frequency			25		MHz
tjit(Ø)	RMS Phase Jitter, Random; NOTE 1	25MHz, REF_OUT, Integration Range: 12kHz - 5MHz		0.215	0.305	ps
		100MHz, Integration Range: 12kHz – 20MHz		0.239	0.330	ps
		125MHz, Integration Range: 12kHz – 20MHz		0.230	0.320	ps
		125MHz, Integration Range: 10kHz – 1MHz		0.190	0.265	ps
		156.25MHz, Integration Range: 12kHz – 20MHz		0.239	0.325	ps
		156.25MHz, Integration Range: 10kHz – 1MHz		0.195	0.260	ps
		250MHz, Integration Range: 12kHz – 20MHz		0.215	0.295	ps
tsk(o)	Output Skew; NOTE 2, 3				35	ps
t_R / t_F	Output Rise/Fall Time	20% - 80%	100		400	ps
odc	Output Duty Cycle		48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Phase Noise Characterized using 25MHz, 12pF resonant crystal.
NOTE 1: Refer to Phase Noise plot.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crosspoint.
NOTE 3: These parameters are guaranteed by characterization. Not tested in production.

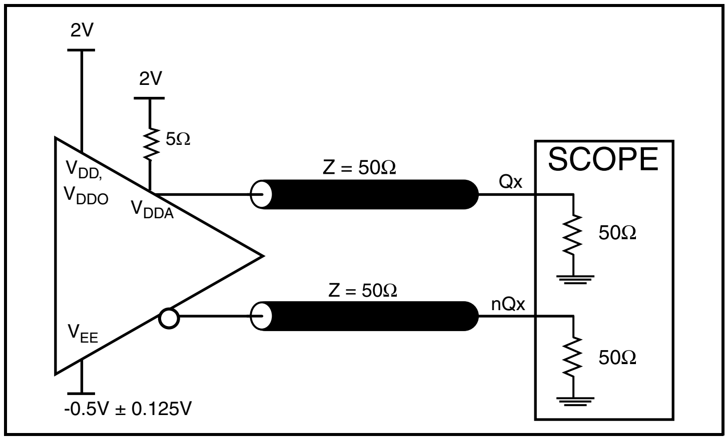
Typical Phase Noise at 156.25MHz (12k – 20MHz, 3.3V)



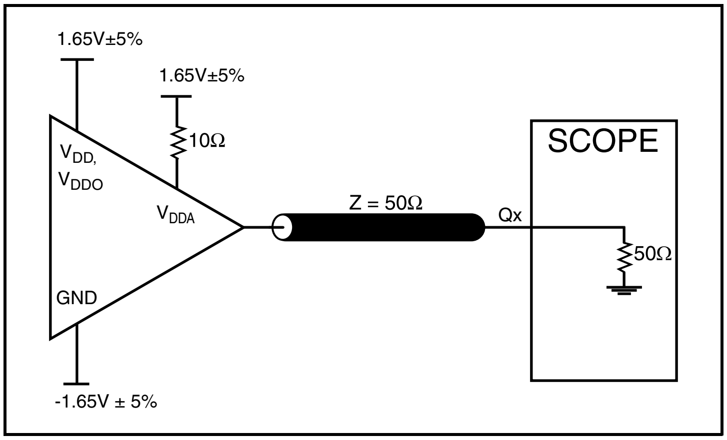
Parameter Measurement Information



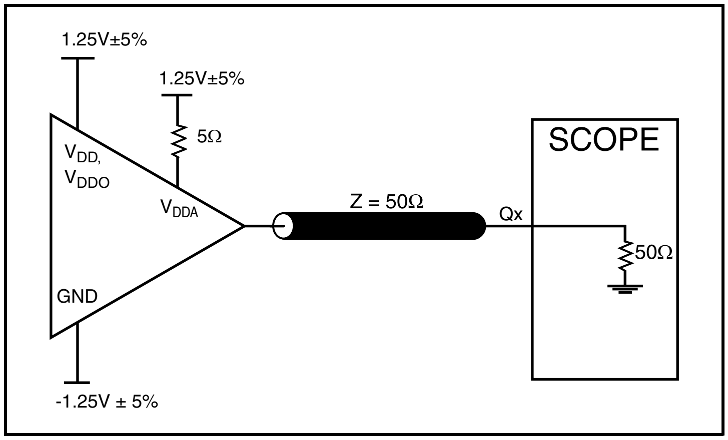
3.3V LVPECL Output Load Test Circuit



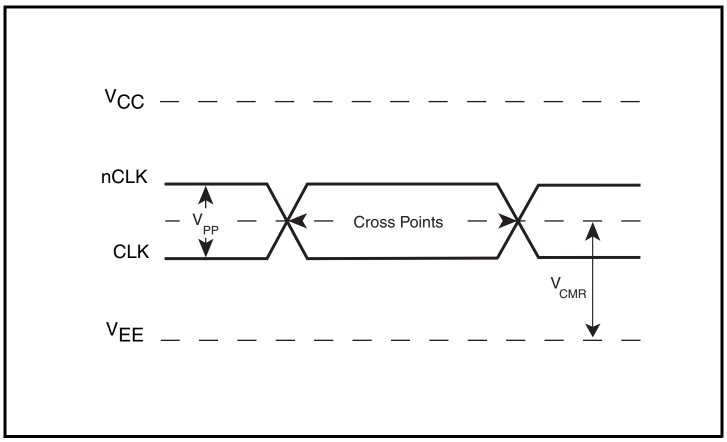
2.5V LVPECL Output Load Test Circuit



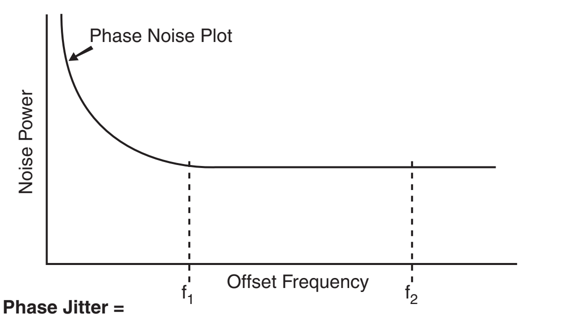
3.3V LVCMOS Output Load Test Circuit



2.5V LVCMOS Output Load Test Circuit



Differential Input Levels

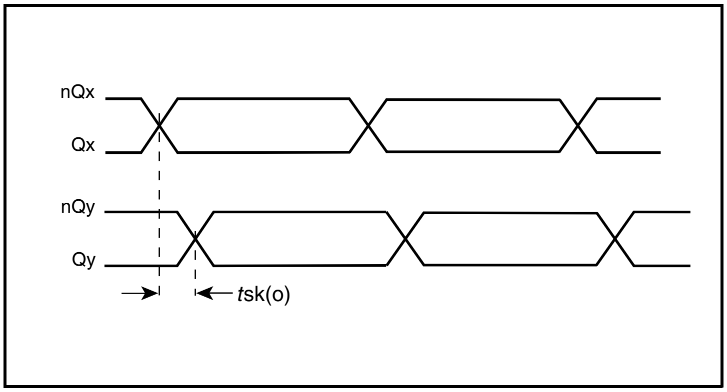


RMS Phase Jitter =

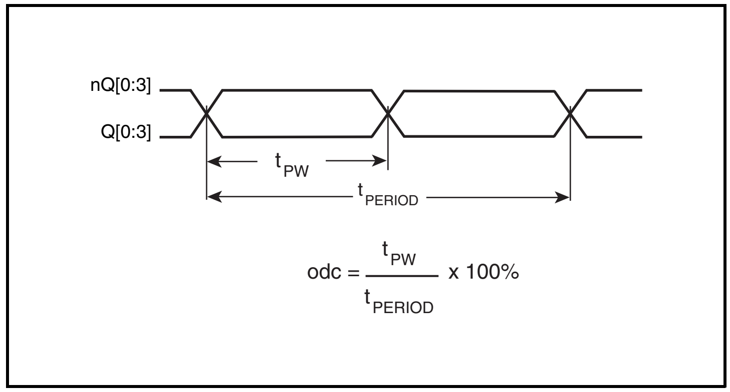
$$\frac{1}{\sqrt{2} * \pi * f} * \sqrt{\text{Area Under Curve Defined by the Offset Frequency Markers}}$$

RMS Phase Jitter

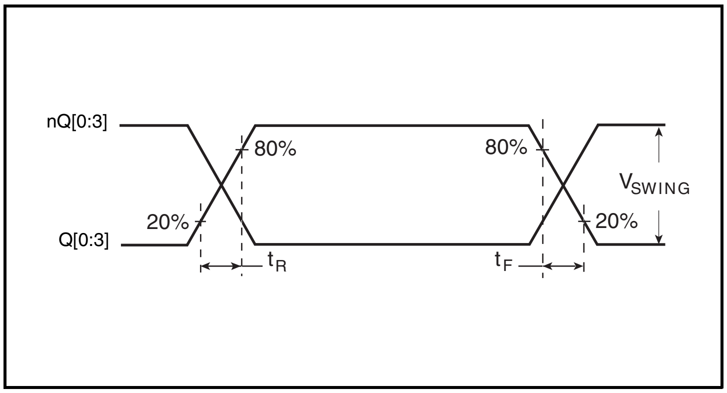
Parameter Measurement Information, continued



Output Skew



Output Duty Cycle/Pulse Width/Period



LVPECL Output Rise/Fall Time

Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

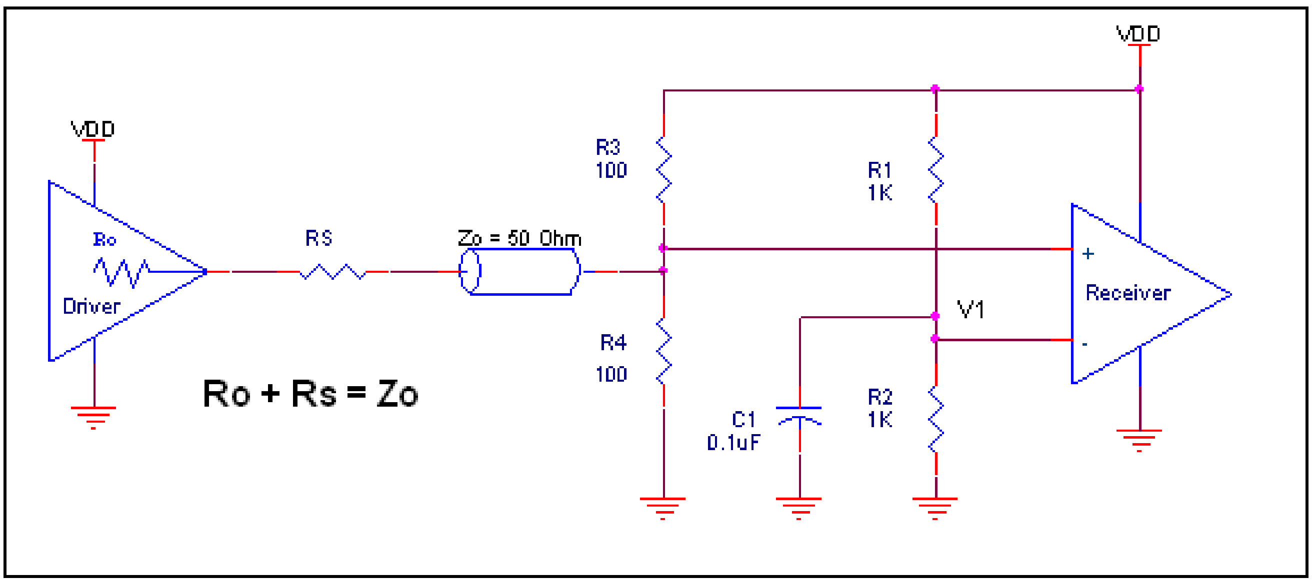


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Overdriving the XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 2A.* The XTAL_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

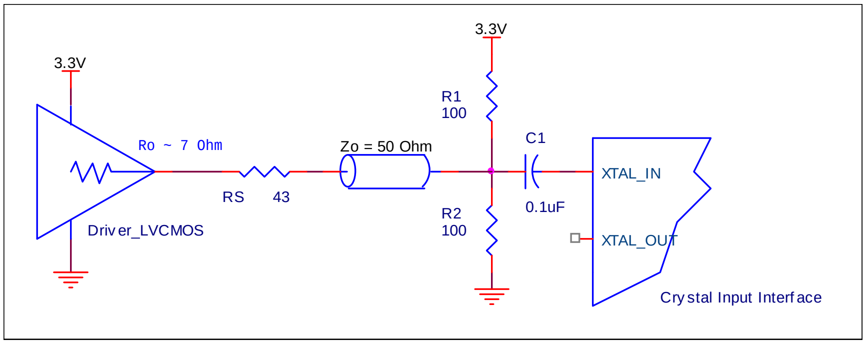


Figure 2A. General Diagram for LVCMOS Driver to XTAL Input Interface

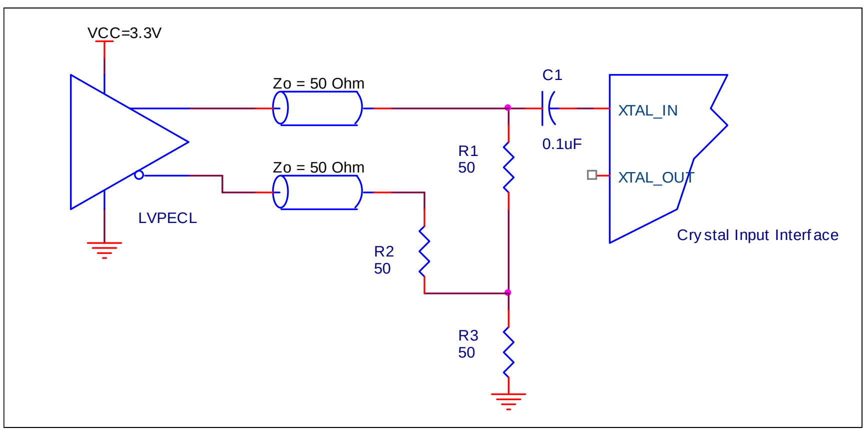


Figure 2B. General Diagram for LVPECL Driver to XTAL Input Interface

3.3V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3D* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

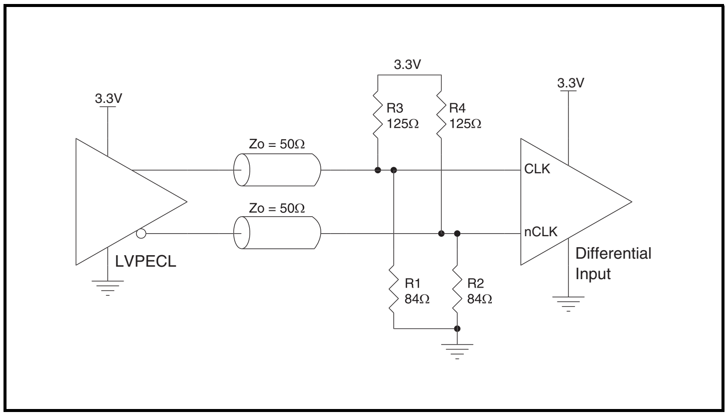


Figure 3A. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

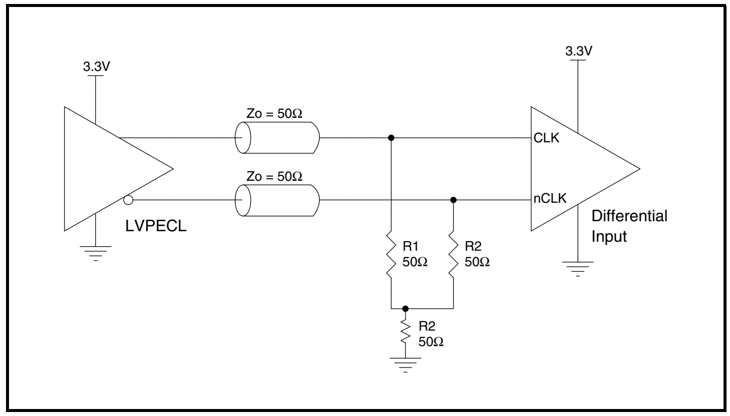


Figure 3B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

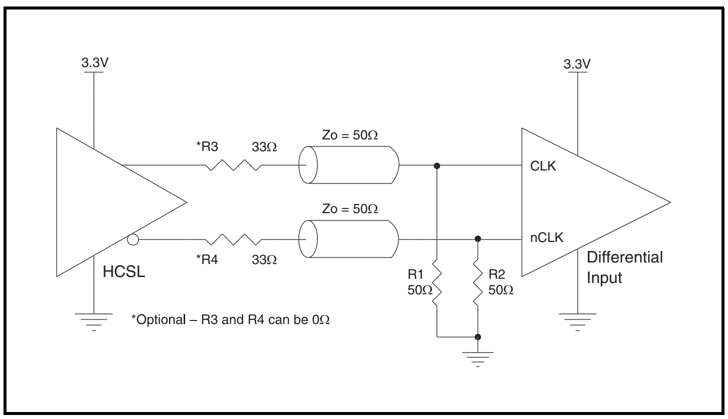


Figure 3C. CLK/nCLK Input Driven by a 3.3V HCSL Driver

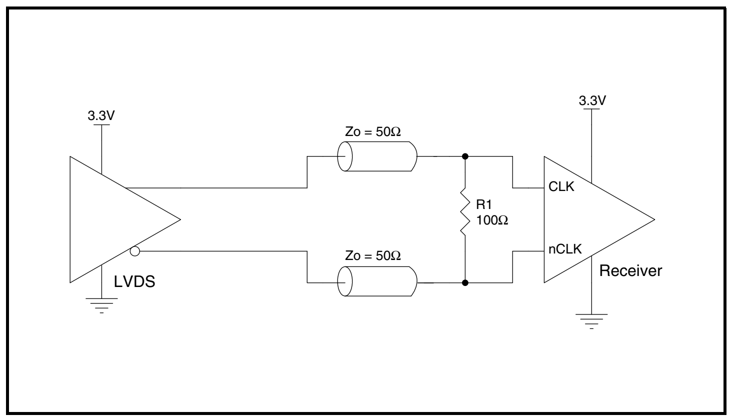


Figure 3D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

2.5V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 4A to 4D* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

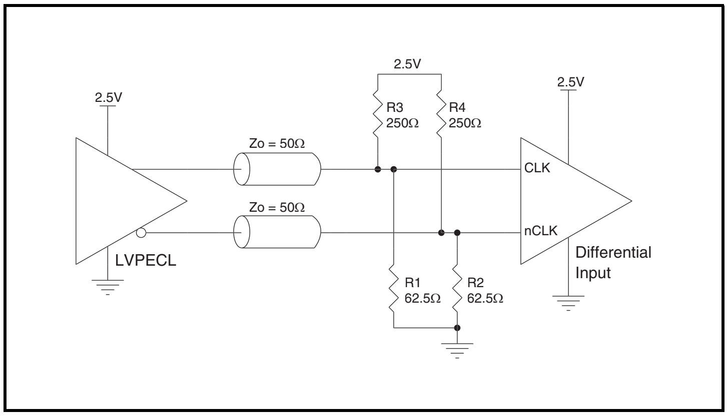


Figure 4A. CLK/nCLK Input Driven by a 2.5V LVPECL Driver

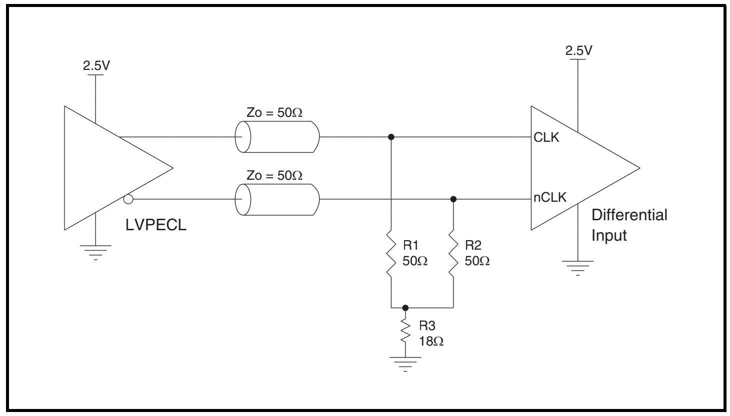


Figure 4B. CLK/nCLK Input Driven by a 2.5V LVPECL Driver

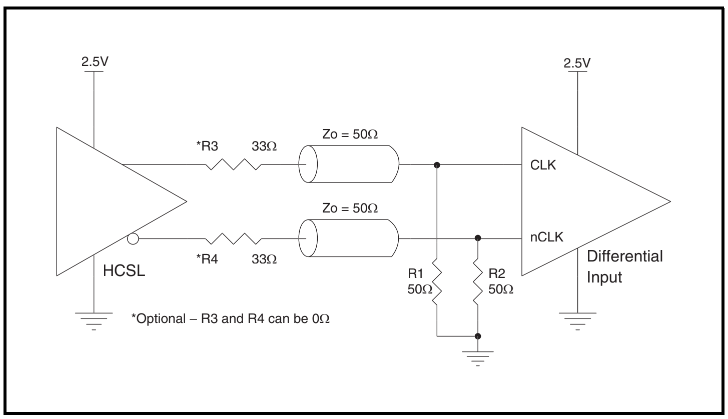


Figure 4C. CLK/nCLK Input Driven by a 2.5V HCSL Driver

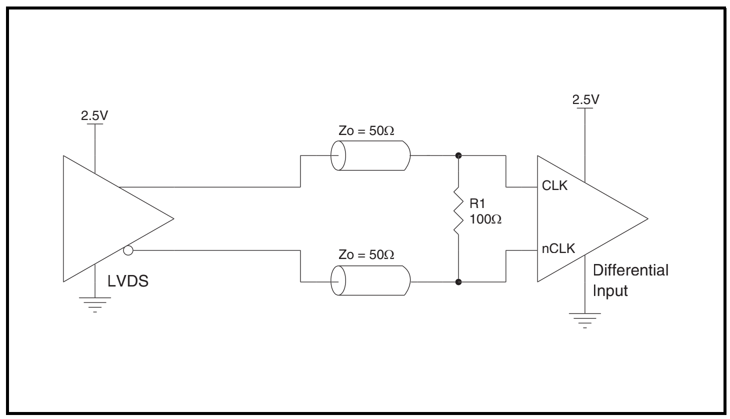


Figure 4D. CLK/nCLK Input Driven by a 2.5V LVDS Driver

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVCMOS Outputs

The unused LVCMOS output can be left floating. There should be no trace attached.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

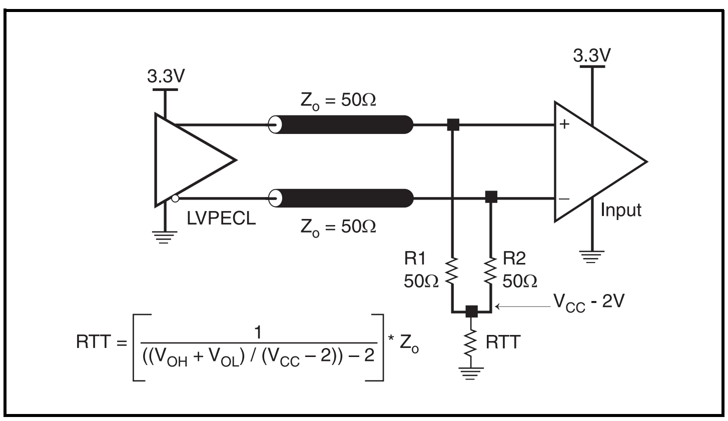


Figure 5A. 3.3V LVPECL Output Termination

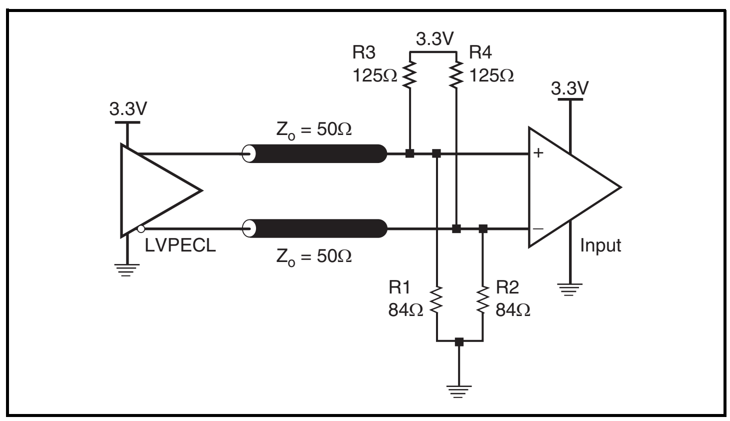


Figure 5B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 6A and *Figure 6B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CCO} – 2V. For V_{CCO} = 2.5V, the V_{CCO} – 2V is very close to ground level. The R3 in Figure 6B can be eliminated and the termination is shown in *Figure 6C.*

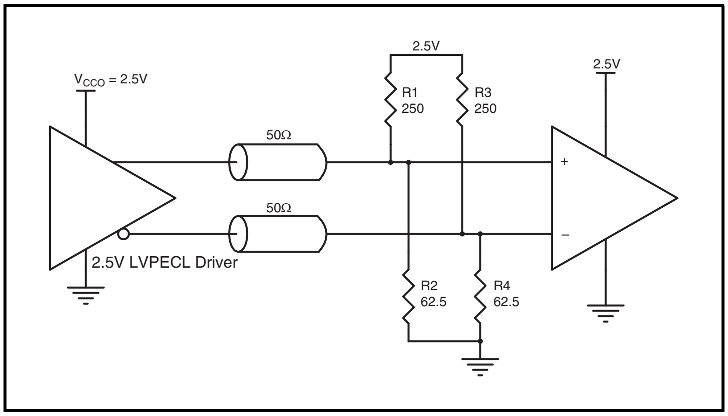


Figure 6A. 2.5V LVPECL Driver Termination Example

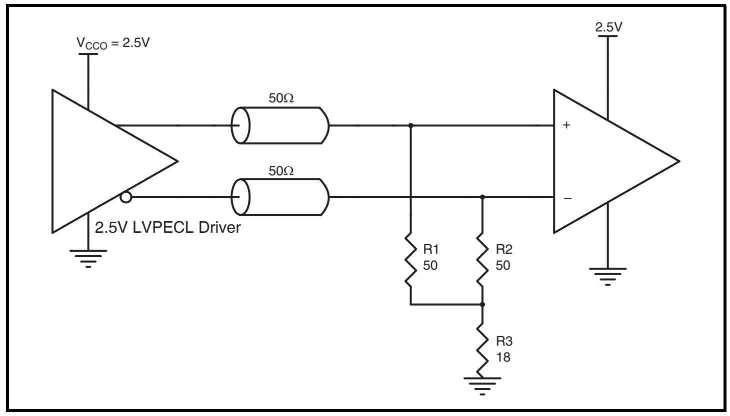


Figure 6B. 2.5V LVPECL Driver Termination Example

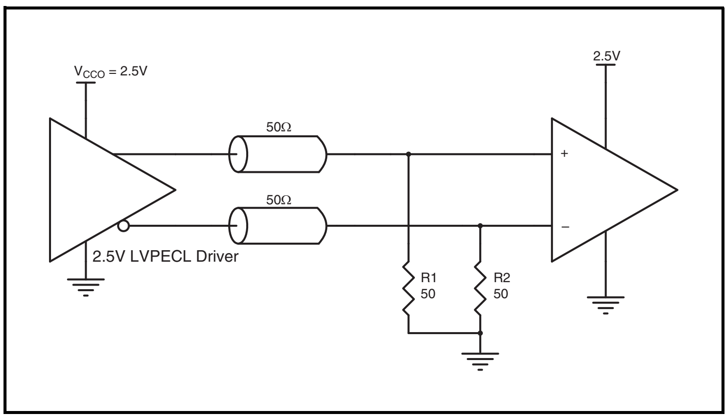


Figure 6C. 2.5V LVPECL Driver Termination Example

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 7.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor's Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

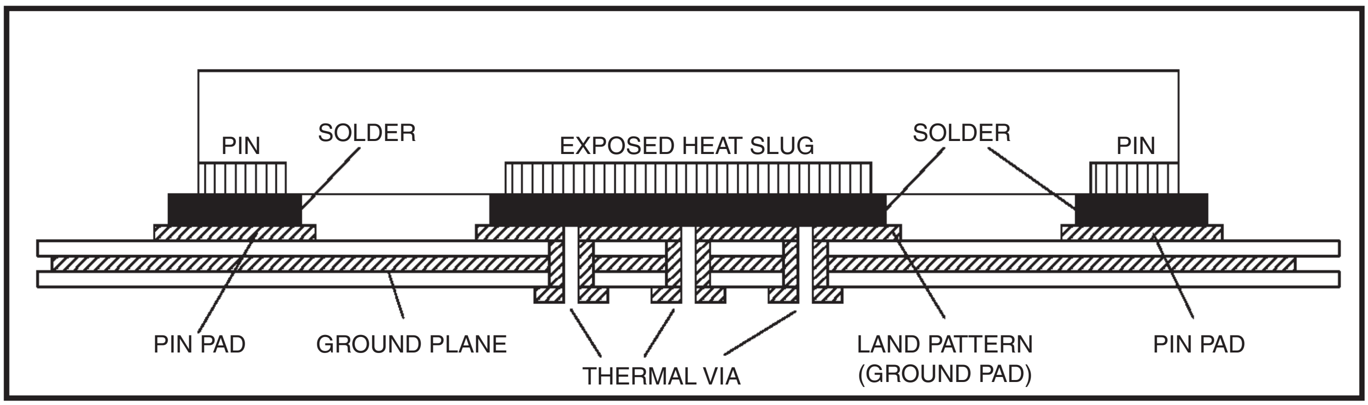


Figure 7. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Schematic Example

Figure 8 (next page) is an IDT8V89704I application example schematic. schematic focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set.

In this example the device is operated at V_{CC}= V_{CCA} = V_{CCO} = 3.3V rather than 2.5V. The CLK, nCLK inputs are provided by a 3.3V LVPECL driver and depicted with a Y-termination rather than the standard four resistor V_{CC} - 2V Thevinin termination for reasons of minimum termination power and layout simplicity. Three examples of LVPECL terminations are shown for the outputs to demonstrate mixing of PECL termination design options. For further options and a more detailed discussion of LVPECL terminations, consult the IDT application note “Termination – LVPECL”.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The IDT8V89704i provides separate power supply pins to isolate any high switching noise from coupling into the internal PLL.

The schematic indicates components that are to be placed close to the IDT8V89704I. Specifically the 0.1uF V_{CC}, V_{CCA} and V_{CCO} bypass capacitors, the 180 ohm Q3, nQ3 LVPECL bias resistors R11 and R12 and the REF_OUT LVCMOS source termination resistor R1. Similarly the 25MHz crystal and its associated load capacitors should also be close to the device.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. The 0.1uF capacitors in each power pin filter must be placed on the device side. If space is limited, the other components can be on the opposite side of the PCB. Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices.

The V_{CC} and V_{CCO} filters start to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

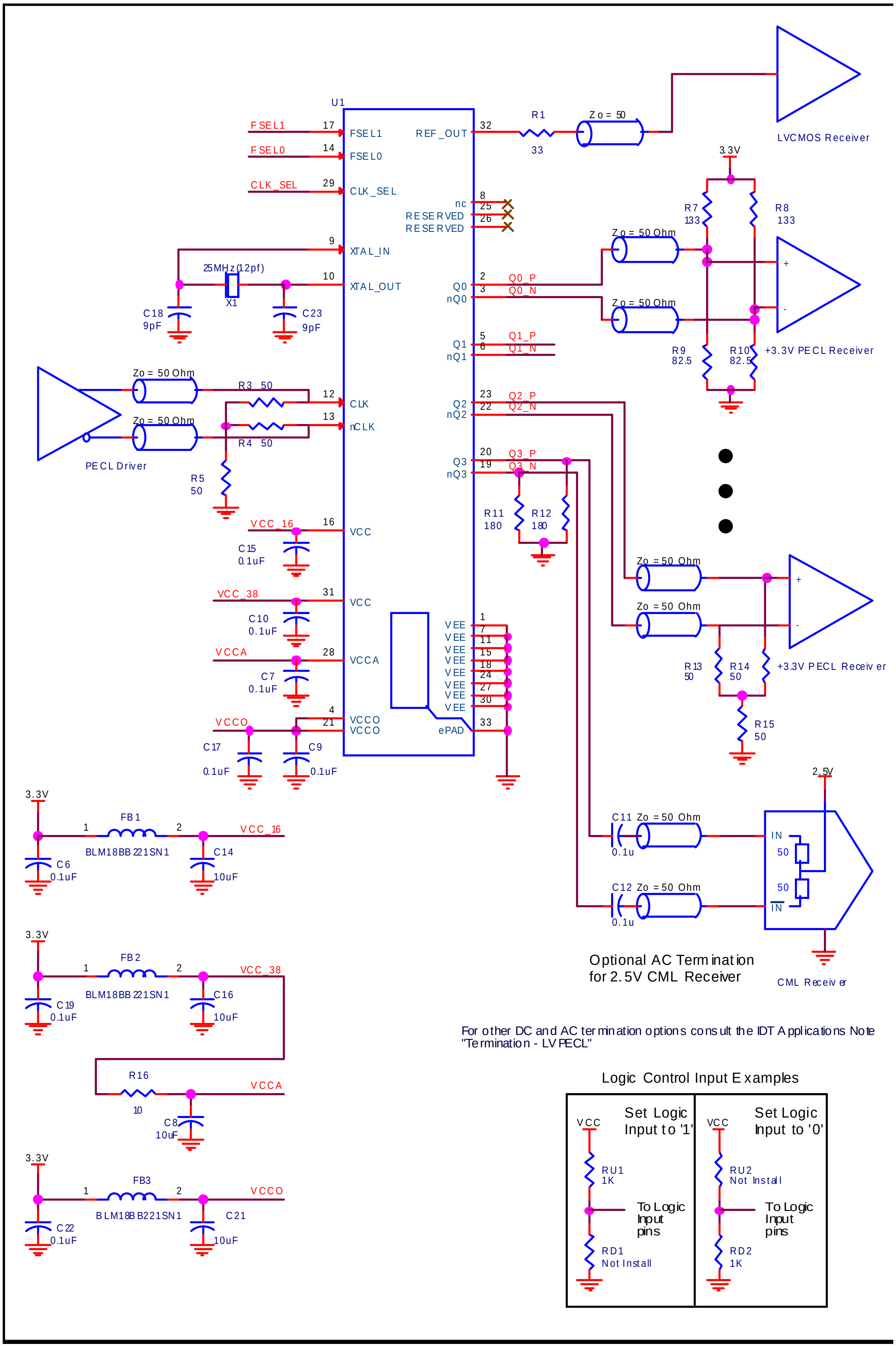


Figure 8. IDT8V89704I Schematic Layout

Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8V89704I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT8V89704I is the sum of the core power plus the power dissipated due to the load.
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated due to the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 204mA = **706.86mW**
- Power $(LVPECL\ outputs)_{MAX}$ = **31.55mW/Loaded Output pair**
- Power (LVPECL output) = 4 * 31.55mW = **126.2mW**

LVCMOS Output

- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to $V_{CCO}/2$
  Output Current $I_{OUT} = V_{CCO\_MAX}$ / [2 * (50Ω + R_{OUT})] = 3.465V / [2 * (50Ω + 20Ω)] = **24.75mA**
- Power Dissipation on the R_{OUT} per LVCMOS output
  Power $(R_{OUT}) = R_{OUT} * (I_{OUT})^2$ = 20Ω * $(24.75mA)^2$ = **12.251mW**

Dynamic Power Dissipation at 25MHz

- Power (25MHz) = C_{PD} * Frequency * $(V_{CCO})^2$ = 10pF * 25MHz * $(3.465V)^2$ = 3mW

Total Power Dissipation

- **Total Power**
  = Power (core) + Power (LVPECL) + Power (R_{OUT}) + Power (25MHz)
  = 706.86mW + 126.2mW + 12.251mW + 3mW **= 848.31mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 65.7°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 848W * 33.1°C/W = 113.1.°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 32 Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**3**
Multi-Layer PCB, JEDEC Standard Test Boards	33.1°C/W	28.1°C/W	25.4°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 8.*

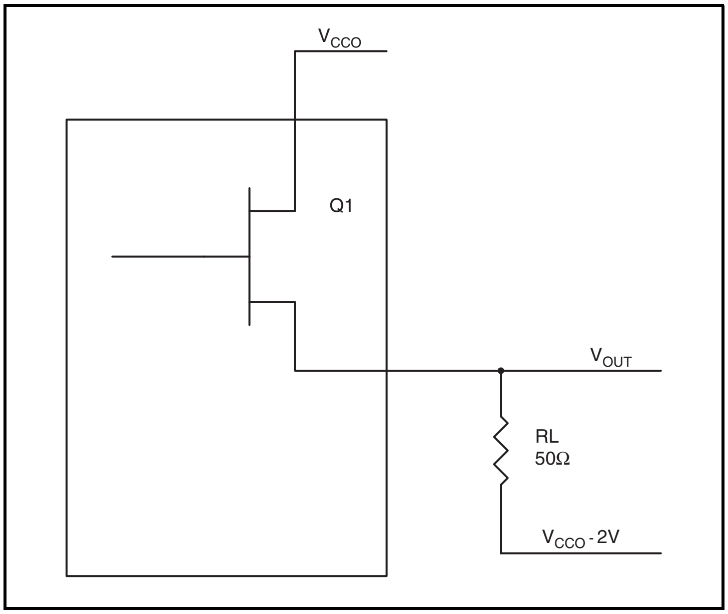


Figure 9. LVPECL Driver Circuit and Termination

To calculate power dissipation due to the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC} - 2V$.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 0.75V}$
  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.75V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.6V}$
  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.6V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.75V)/50\Omega] * 0.75V = \mathbf{18.75mW}$

$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.6V)/50\Omega] * 1.6V = \mathbf{12.80mW}$

Total Power Dissipation per output pair = Pd_H + Pd_L = **31.55mW**

Reliability Information

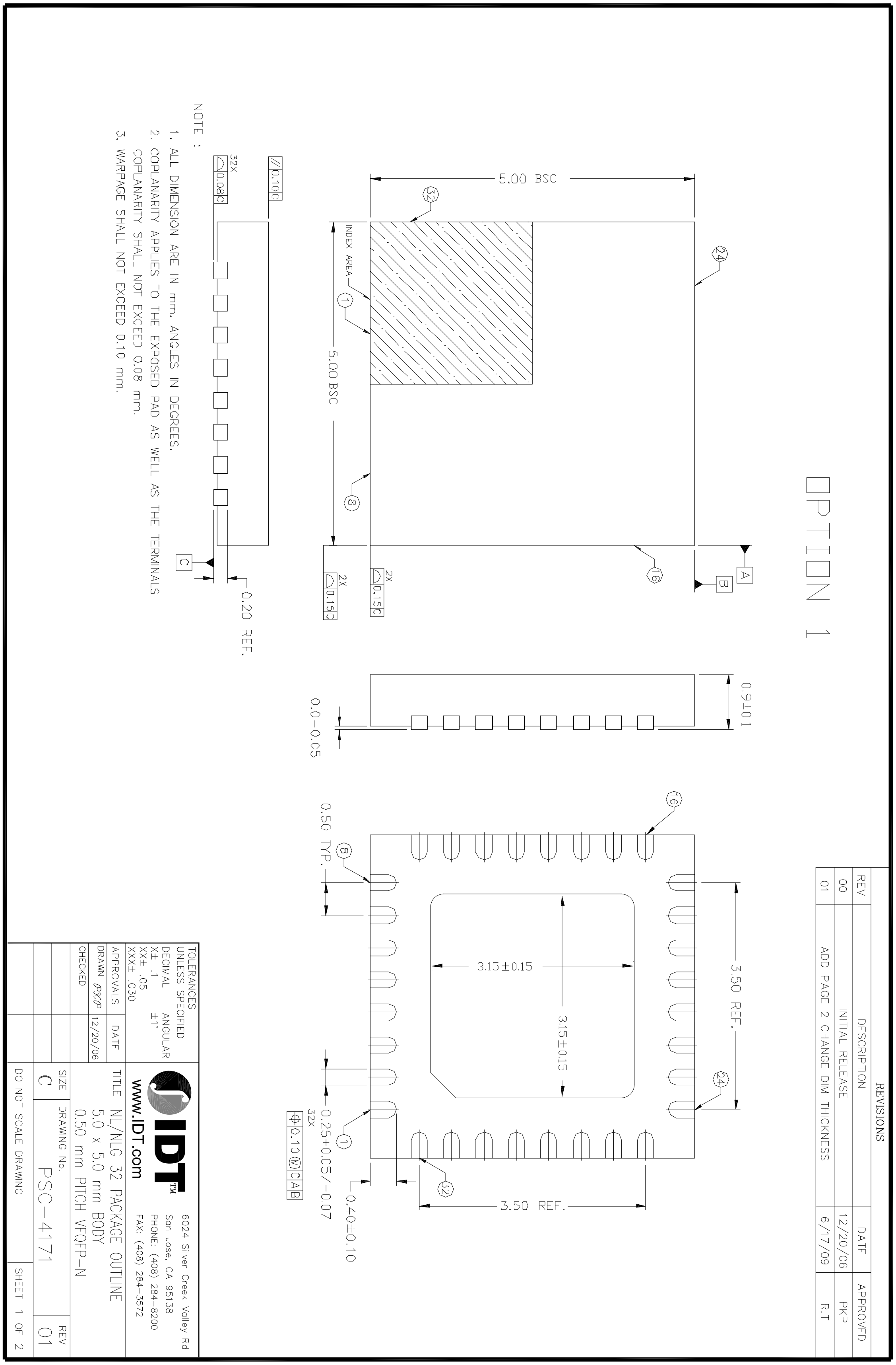
Table 8. θ_{JA} vs. Air Flow Table for a 32 Lead VFQFN

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**3**
Multi-Layer PCB, JEDEC Standard Test Boards	33.1°C/W	28.1°C/W	25.4°C/W

Transistor Count

The transistor count for IDT8V89704I is: 26,859.

32 Lead VFQFN Package Outline and Dimensions



Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8V89704ANLGI	IDT8V89704ANLGI	"Lead-Free" 32 Lead VFQFN	Tray	-40°C to 85°C
8V89704ANLGI8	IDT8V89704ANLGI	"Lead-Free" 32 Lead VFQFN	Tape & Reel	-40°C to 85°C

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