Intermediate Frequency Digital Variable Gain Amplifier

**General Description**

The IDTF1200 is a Digitally Controlled Intermediate Frequency Differential Variable Gain Amplifier for BaseStation and other commercial applications with a low IF frequency. The device offers extremely low Noise Figure over the entire gain control range. The device is packaged in compact 5x5 Thin QFNs with 200 ohm differential input and output impedances for ease of integration into the receiver lineup. Versions covering IF frequencies up to 300 MHz with low distortion are available.

**Competitive Advantage**

The F1200 acts to enhance system SNR when VGA gain is reduced. The F1200 noise figure (NF) degrades only slightly (NF slope ~ -0.16 dB/dB) over a 13 dB control range while holding the Output IP3 approximately constant. The resultant improvement in noise can enhance the system SNR up to 2 decibels at low gain settings relative to a standard VGA.

The device has excellent DNL and INL simplifying digital compensation. The device also offers the extremely low Harmonic, IM2, and IM3 distortion necessary to drive an ADC directly in an IF sub-sampling application.

**Applications**

- BaseStation Diversity Receivers
- Digital Pre-Distortion
- \(\mu\)Wave Point-to-Point Radios
- Public Safety Receivers

**Part# Matrix**

<table>
<thead>
<tr>
<th>Part#</th>
<th>Gain Range</th>
<th>IP3o</th>
<th>IF freq range</th>
<th>NF</th>
</tr>
</thead>
<tbody>
<tr>
<td>F1200</td>
<td>22 to -1</td>
<td>48</td>
<td>50 - 160</td>
<td>2.6</td>
</tr>
<tr>
<td>F1206*</td>
<td>20 to -11</td>
<td>47</td>
<td>150 - 250</td>
<td>3.6</td>
</tr>
<tr>
<td>F1207*</td>
<td>20 to -11</td>
<td>46</td>
<td>230 - 300</td>
<td>3.7</td>
</tr>
</tbody>
</table>

*Future Product

**Features**

- Ideal for high SNR systems
- 22 dB typ Maximum Gain
- 23 dB gain control range
- 7 bit parallel control
- 0.25 dB Gain Steps
- Excellent Noise Figure < 3.0 dB
- 5mm x 5mm 28 pin package
- 200 Ω Differential Input
- 200 Ω Differential Output
- NF degrades < 2dB @ 12dB reduced gain
- 50 MHz – 160 MHz frequency range
- Ultra-Linear: \(\text{IP3} \_0 +48 \text{ dBm typical}\)
- External current setting resistor
- Fast Gain Step Settling < 20 nsec

**Device Block Diagram**

**Ordering Information**

Omit IDT prefix

0.75 mm height package

Tape & Reel

RF product Line

Green

Industrial Temp range
Absolute Maximum Ratings

- $V_{CC}$ to GND: -0.3V to +5.5V
- All other Pins to GND: -0.3V to $(V_{CC} +0.25V)$
- $I_{SET}$ to GND: -0.3V to +2.2V
- RF Input Power (ATTN_IN+, ATTN_IN-) @ $G_{MAX}$: +10 dBm
- Continuous Power Dissipation: 1.5W
- $\theta_J$ (Junction – Ambient): +41°C/W
- $\theta_{JC}$ (Junction – Case): +4°C/W
- Operating Temperature Range (Case Temperature): $T_C = -40°C$ to +85°C
- Maximum Junction Temperature: 150°C
- Storage Temperature Range: -65°C to +150°C
- Lead Temperature (soldering, 10s): +260°C

Key Feature – Noise Figure Slope

Standard Variable Gain amplifiers exhibit a [NF/Gain] slope of -1 dB/dB. Practically speaking, as gain is reduced, Noise Figure degrades dB for dB. The F1200 utilizes new technology that flattens the Noise Figure response (~ -0.16 dB/dB) for most of the gain control range while keeping distortion (Output IP3) constant. The result is that NF is improved up to 16 dB vs. a standard VGA at low gain settings. The graph below illustrates this by showing the IDTF1200 NF and IP3O vs. Gain setting contours.
IDTF1200 SPECIFICATION

VCC = +5.0V, fRF = 100MHz, TC = +25°C, STBY = GND, R6 = 2.87K +/-1%, POUT = +3 dBm, unless otherwise noted in the condition column. EVkit trace, transformer & matching losses are de-embedded for specification purposes (note: de-embedded losses = 0.4dB input and 0.4dB output at 100MHz).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Symbol</th>
<th>min</th>
<th>typ</th>
<th>max</th>
<th>units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Temp. Range</td>
<td>Case Temperature Measured at the exposed paddle</td>
<td>TC</td>
<td>-40</td>
<td>+85</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Logic Input High</td>
<td></td>
<td>VIH</td>
<td>2.0†</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Logic Input Low</td>
<td></td>
<td>VIL</td>
<td>0.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Logic Current</td>
<td></td>
<td>IIL, IIL</td>
<td>-1</td>
<td></td>
<td>+1</td>
<td>μA</td>
</tr>
<tr>
<td>Operating voltage range</td>
<td>Analog &amp; Digital Supplies</td>
<td>VCC</td>
<td>4.75</td>
<td>5.25</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Supply Current</td>
<td>Total, All VCC, R6= 2.87K +/--1%</td>
<td>ISUPP</td>
<td>103</td>
<td></td>
<td>110</td>
<td>117</td>
</tr>
<tr>
<td>Standby Current</td>
<td>Total, All VCC</td>
<td>ISTBY</td>
<td>2.5</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Frequency Range</td>
<td>Output IP3 &gt; +40 dBm</td>
<td>fRF</td>
<td>50</td>
<td>160</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>Input Resistance</td>
<td>Differential</td>
<td>Rin</td>
<td>200</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>Output Resistance</td>
<td>Differential</td>
<td>Rout</td>
<td>200</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>Maximum Gain</td>
<td>GC = [0000000]</td>
<td>GMAX</td>
<td>20.7</td>
<td>21.7</td>
<td>22.6</td>
<td>dB</td>
</tr>
<tr>
<td>Minimum Gain</td>
<td>GC = [1011101]</td>
<td>GMIN</td>
<td>-2.8</td>
<td>-1.7</td>
<td>-0.7</td>
<td>dB</td>
</tr>
<tr>
<td>Gain Step</td>
<td></td>
<td>LSB</td>
<td>0.25</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Phase Slope</td>
<td>∆Φ due to change in gain</td>
<td>ΦSLOPE</td>
<td>0.3</td>
<td></td>
<td></td>
<td>deg/dB</td>
</tr>
<tr>
<td>Differential Gain Error</td>
<td>Between adjacent 1dB steps</td>
<td>DNL</td>
<td>.05</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Integral Gain Error</td>
<td>Error vs. straight line</td>
<td>INL</td>
<td>+/-0.20</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>At Maximum Gain</td>
<td>NF</td>
<td>2.6</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>GC = [0110100] (gain = 9dB)</td>
<td>NFBACK</td>
<td>4.55</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Output IP3</td>
<td></td>
<td>IP3O1</td>
<td>48</td>
<td></td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>Output IP3 – at Gback</td>
<td></td>
<td>IP3O2</td>
<td>44</td>
<td></td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>Settling Time</td>
<td></td>
<td>T1dB</td>
<td>15²</td>
<td></td>
<td></td>
<td>nsec</td>
</tr>
<tr>
<td>2nd Harmonic</td>
<td></td>
<td>H2</td>
<td>-82</td>
<td></td>
<td></td>
<td>dBc</td>
</tr>
<tr>
<td># Control Bits</td>
<td>Parallel</td>
<td>CB</td>
<td>7</td>
<td></td>
<td></td>
<td>#</td>
</tr>
<tr>
<td>1 dB Compression</td>
<td></td>
<td>P1dB0</td>
<td>+16.7</td>
<td>+19.4</td>
<td></td>
<td>dBm</td>
</tr>
</tbody>
</table>

1 – Items in bold italics are Guaranteed by Test
2 – See Graph on Page 8
**Typical Operating Parametric Curves**

- **Gain vs. Temperature**
  - Gain (dB) vs. Frequency (MHz) for different temperatures (40°C, 25°C, 85°C).

- **Gain vs. Voltage**
  - Gain (dB) vs. Frequency (MHz) for different voltages (4.75V, 5.00V, 5.25V).

- **S11 vs. Temperature**
  - Input Gamma [s11] (dB) vs. Frequency (MHz) for different temperatures.

- **S22 vs. Temperature**
  - Output Gamma [s22] (dB) vs. Frequency (MHz) for different temperatures.

- **S12 vs. Temperature**
  - Reverse Isolation [s12] (dB) vs. Frequency (MHz) for different temperatures.

- **Gain and NF vs. Frequency**
  - Gain (dB) and Noise Figure (dB) vs. Frequency (MHz).

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**IDT Proprietary**
**S11 vs. Gain Setting**

- Graph showing input gamma (dB) vs. gain setting (dB) for 50 MHz, 100 MHz, and 150 MHz.

**S22 vs. Gain Setting**

- Graph showing output gamma (dB) vs. gain setting (dB) for 50 MHz, 100 MHz, and 150 MHz.

**S21 vs. Gain Setting**

- Graph showing gain (dB) vs. gain setting (dB) for 50 MHz, 100 MHz, and 150 MHz.

**S21 Phase vs. Gain Setting**

- Graph showing normalized S21 phase response (degrees) vs. gain setting (dB) for 50 MHz, 100 MHz, and 150 MHz.

**EVKit NF & Output IP3 Correction**

- Graph showing NF correction and IP3 correction vs. frequency (MHz), indicating how to correct EVkit measured output IP3.

**EVKit Gain Correction**

- Graph showing EVkit loss (dB) vs. frequency (MHz), indicating how to correct EVkit measured gain.

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**Intermediate Frequency Digital Variable Gain Amplifier**

**IDTF1200**

**DATASHEET**

**TOCs CONTINUED**
Intermediate Frequency Digital Variable Gain Amplifier

TOCs CONTINUED

DNL vs. Frequency (1dB Steps)

DNL vs. Voltage (100 MHz, 1dB Steps)

DNL vs. Temperature (100 MHz, 1dB Steps)

DNL vs. Temperature (100 MHz, 0.5dB Steps)

DNL vs. Temperature (100 MHz, 0.25dB Steps)

INL vs. Frequency
TOCs CONTINUED

**INL vs. Temperature (100 MHz)**

![INL vs. Temperature (100 MHz) graph]

**INL vs. Voltage (100 MHz)**

![INL vs. Voltage (100 MHz) graph]

**Noise Figure vs. Frequency**

![Noise Figure vs. Frequency graph]

**Noise Figure vs. Voltage (100 MHz)**

![Noise Figure vs. Voltage (100 MHz) graph]

**Noise Figure vs. Temperature (100 MHz)**

![Noise Figure vs. Temperature (100 MHz) graph]

**Output P1dB vs. Voltage**

![Output P1dB vs. Voltage graph]
Intermediate Frequency Digital Variable Gain Amplifier

Output IP3 vs. Frequency

Output IP3 vs. Voltage (100 MHz)

Output IP3 vs. Temperature (100 MHz)

2nd Harmonic vs. Temperature (100 MHz)

Settling Time (16dB Step, 100 MHz)

Settling Time (1 dB Step, 100 MHz)
PIN DIAGRAM

TOP View
(looking through the top of the package)

Package Drawing

5 mm x 5 mm package dimension
3.25 mm x 3.25 mm exposed pad
0.5 mm pitch
28 pins
0.75 mm height
0.25 mm pad width
0.40 mm pad length
## Pin Descriptions

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Pin Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GND</td>
<td>Untested - SPI Chip Select Input</td>
</tr>
<tr>
<td>2</td>
<td>V_{CC} ATTN</td>
<td>Attenuator Power Supply</td>
</tr>
<tr>
<td>3</td>
<td>ATTN_IN+</td>
<td>Attenuator_0 Differential Input P</td>
</tr>
<tr>
<td>4</td>
<td>ATTN_IN-</td>
<td>Attenuator_0 Differential Input M</td>
</tr>
<tr>
<td>5</td>
<td>Ground</td>
<td>Untested - SPI Data Input</td>
</tr>
<tr>
<td>6</td>
<td>Ground</td>
<td>Untested - SPI Clock Input</td>
</tr>
<tr>
<td>7</td>
<td>Ground</td>
<td>Untested - SPI Clock Input</td>
</tr>
<tr>
<td>8</td>
<td>GC6</td>
<td>Parallel Gain Control Input – MSB (16 dB step)</td>
</tr>
<tr>
<td>9</td>
<td>GC5</td>
<td>Parallel Gain Control Input</td>
</tr>
<tr>
<td>10</td>
<td>GC4</td>
<td>Parallel Gain Control Input</td>
</tr>
<tr>
<td>11</td>
<td>GC3</td>
<td>Parallel Gain Control Input</td>
</tr>
<tr>
<td>12</td>
<td>GC2</td>
<td>Parallel Gain Control Input</td>
</tr>
<tr>
<td>13</td>
<td>GC1</td>
<td>Parallel Gain Control Input</td>
</tr>
<tr>
<td>14</td>
<td>GC0</td>
<td>Parallel Gain Control Input – LSB (0.25 dB step)</td>
</tr>
<tr>
<td>15</td>
<td>V_{CC} DIG</td>
<td>Digital Circuit Power Supply</td>
</tr>
<tr>
<td>16</td>
<td>DIG GND</td>
<td>Connect directly to Ground</td>
</tr>
<tr>
<td>17</td>
<td>V_{MODE}</td>
<td>Untested – SPI Enable</td>
</tr>
<tr>
<td>18</td>
<td>AMP_OUT+</td>
<td>Amplifier Differential Output P</td>
</tr>
<tr>
<td>19</td>
<td>AMP_OUT-</td>
<td>Amplifier Differential Output M</td>
</tr>
<tr>
<td>20</td>
<td>STBY</td>
<td>Amplifier Power Down.  Ground for Normal operation</td>
</tr>
<tr>
<td>21</td>
<td>I_SET</td>
<td>Current Setting Resistor. Connect recommended value (2.87K) to ground. Use 1% tolerance</td>
</tr>
<tr>
<td>22</td>
<td>V_{CC} Amp Bias</td>
<td>Amplifier Bias Circuit Power Supply</td>
</tr>
<tr>
<td>23</td>
<td>Bias Amp</td>
<td>Amplifier Bias External Pin for Decoupling Capacitor</td>
</tr>
<tr>
<td>24</td>
<td>AMP IN+</td>
<td>Amplifier Differential Input P</td>
</tr>
<tr>
<td>25</td>
<td>E Amp</td>
<td>Amplifier Common Emitter</td>
</tr>
<tr>
<td>26</td>
<td>AMP IN-</td>
<td>Amplifier Differential Input M</td>
</tr>
<tr>
<td>27</td>
<td>ATTN OUT-</td>
<td>Attenuator_0 Differential Output M</td>
</tr>
<tr>
<td>28</td>
<td>ATTN OUT+</td>
<td>Attenuator_0 Differential Output P</td>
</tr>
<tr>
<td></td>
<td>Exposed Paddle</td>
<td></td>
</tr>
</tbody>
</table>
**EVkit / APPLICATIONS CIRCUIT SCHEMATIC**

The diagram below describes the recommended applications / EVkit circuit:
EVKit & BOM (Email: RFsupport@IDT.com to request Controller SW and Cable)

The picture and table below describes the recommended EVkit operation and BOM:

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**Item #** | **Value** | **Size** | **Desc** | **Mfr. Part #** | **Mfr.** | **Ref Des**
--- | --- | --- | --- | --- | --- | ---
1 | 4:1 Balun | SM-22 | 4:1 Center Tap Balun | TC4-1TG2+ | Mini Circuits | T1,T2
2 | 2.87k | 0402 | RES 2.8K OHM 1/10W 1% 0402 SMD | ERJ-2RKF2871X | Panasonic | R6
3 | 47k | 0402 | Pullup resistors for STBY and VMODE jumpers | RC0402FR-0747KL | Yageo | R4, R13
4 | 0 | 0402 | RES 0.0 OHM 1/10W 0402 SMD | ERJ-2GE0R00X | Panasonic | R11
5 | 680 nH | 1008 | RF inductor, ceramic core, 5% tol, SMT, RoHS | 1008CS-681XJLC | Coilcraft | L1,L2
6 | 10 nF | 0402 | CAP CER 10000PF 16V 10% X7R 0402 | GRM155R71C103KA01D | MURATA | C1,C2,C8,C23,C24
7 | 1000 pF | 0402 | CAP CER 1000PF 50V C0G 0402 | GRM1555C1H102JA01D | MURATA | C4,C10,C13,C19
8 | 0.1uF | 0402 | CAP CER .1UF 10V 10% X5R 0402 | GRM155R61A104KA01D | MURATA | C9,C11,C17,C20
9 | SMA | .062 | SMA_END_LAUNCH | 142-0711-621 | Emerson Johnson | J1,J2,J3
10 | Header_2Pin | TH_2 | CONN HEADER VERT SGL 2POS GOLD | 961102-6404-AR | 3M | JP1,JP3
11 | Header_14Pin | TH_7x2 | CONN HEADER 14 POS STRGHT GOLD | N2514-6002-RB | 3M | JP5
12 | F1200ZD | QFN-28 | IF VGA | Q01B005M | IDT | U1
13 | PCB | | | F1200 EV Kit Rev 1 | | |
14 | DNP | 0402 | Resistors to ground on Gain ctrl lines | | | R14 thru R20
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