

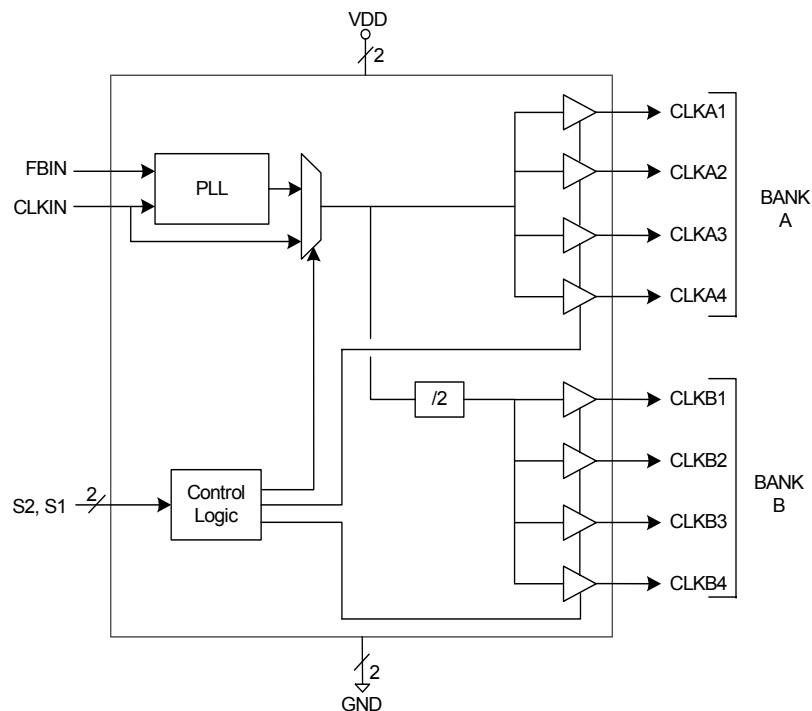
Description

The MK2308-2 is a low jitter, low skew, high performance Phase-Lock Loop (PLL) based zero delay buffer for high speed applications. Based on IDT's proprietary low jitter PLL techniques, the device provides eight low skew outputs at speeds up to 133.3 MHz at 3.3 V. The MK2308-2 includes a bank of four outputs running at 1/2X. In the zero delay mode, the rising edge of the input clock is aligned with the rising edges of all eight outputs. Compared to competitive CMOS devices, the MK2308-2 has the lowest jitter.

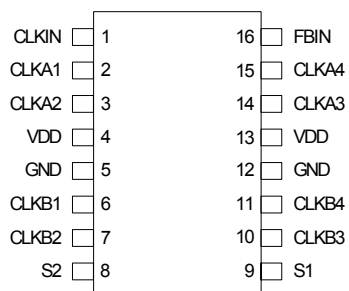
Features

- Packaged in 16-pin SOIC
- Pb (lead) free package
- Zero input-output delay
- Four 1X outputs plus four 1/2X outputs
- Output to output skew is less than 250 ps
- Output clocks up to 133.3 MHz at 3.3 V
- Ability to generate 2X the input
- Full CMOS outputs with 18 mA output drive capability at TTL levels at 3.3 V
- Spread Smart™ technology works with spread spectrum clock generators
- Advanced, low power, sub micron CMOS process
- Operating voltage of 3.3 V

Block Diagram



Pin Assignment



16-pin (150 mil) SOIC

Feedback Configuration Table

| Feedback From | CLKA1:A4 | CLKB1:B4 |
|---------------|----------|----------|
| Bank A | CLKIN | CLKIN/2 |
| Bank B | 2XCLKIN | CLKIN |

Output Clock Mode Select Table

| S2 | S1 | Clocks A1:A4 | Clocks B1:B4 | Internet Generation | PLL Status |
|----|----|----------------------------|----------------------------|-----------------------------|------------|
| 0 | 0 | Tri-state (high impedance) | Tri-state (high impedance) | None | On |
| 0 | 1 | Running | Tri-state (high impedance) | PLL | On |
| 1 | 0 | Running | Running | Buffer only (no zero delay) | Off |
| 1 | 1 | Running | Running | PLL | On |

Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|------------|----------|----------|---|
| 1 | CLKIN | Input | Clock input. Connect to input clock source. |
| 2 - 3 | CLKA1:A4 | Output | Clock A bank of four outputs. |
| 4 | VDD | Power | Power supply. Connect pin to same voltage as pin 13 (either 3.3 V). |
| 5 | GND | Power | Connect to ground. |
| 6 - 7 | CLKB1:B4 | Output | Clock B bank of four outputs. These are low skew divide by two of bank A. |
| 8 | S2 | Input | Select input 2. Selects mode for outputs per table above. |
| 9 | S1 | Input | Select input 1. Selects mode for outputs per table above. |
| 10 - 11 | CLKB1:B4 | Output | Clock B bank of four outputs. These are low skew divide by two of bank A. |
| 12 | GND | Power | Connect to ground. |
| 13 | VDD | Power | Power supply. Connect pin to same voltage as pin 4 (either 3.3 V). |
| 14 - 15 | CLKA1:A4 | Output | Clock A bank of four outputs. |
| 16 | FBIN | Input | Feedback input. Determines outputs per table above. |

External Components

The MK2308-2 requires a minimum number of external components for proper operation. Decoupling capacitors of 0.1 μ F should be connected between VDD and GND, as close to the part as possible. A 33 Ω series terminating resistor should be used on each clock output to reduce reflections.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK2308-2. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|-------------------------------|---------------------|
| Supply Voltage, VDD | 7 V |
| All Inputs and Outputs | -0.5 V to VDD+0.5 V |
| Ambient Operating Temperature | 0 to +70 °C |
| Storage Temperature | -65 to +150 °C |
| Junction Temperature | 175 °C |
| Soldering Temperature | 260 °C |

Recommended Operation Conditions

| Parameter | Min. | Typ. | Max. | Units |
|---|------|------|------|-------|
| Ambient Operating Temperature | 0 | | +70 | °C |
| Power Supply Voltage (measured in respect to GND) | +3.0 | | +5.5 | V |

DC Electrical Characteristics

VDD=3.3 V \pm 10%, Temp 0 to +70° / -40 to +85° C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---------------------|-----------------|--------------------------|-----------|-------|-----------|-------|
| Operating Voltage | VDD | | 3.0 | 3.3 | 3.6 | V |
| Input High Voltage | V _{IH} | CLKIN pin only | (VDD/2)+1 | VDD/2 | | V |
| Input Low Voltage | V _{IL} | CLKIN pin only | | VDD/2 | (VDD/2)-1 | V |
| Input High Voltage | V _{IH} | | 2 | | | V |
| Input Low Voltage | V _{IL} | | | | 0.8 | V |
| Output High Voltage | V _{OH} | I _{OH} = -18 mA | 2.4 | | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 18 mA | | | 0.4 | V |
| Output High Voltage | V _{OH} | I _{OH} = -5 mA | VDD-0.4 | | | V |

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|-----------------|--------------------|------|------|------|-------|
| Operating Supply Current 100 MHz, CLKIN | IDD | No Load S1=S2=1 | | 44 | | mA |
| Short Circuit Current | I _{OS} | Each output | | ± 65 | | mA |
| Input Capacitance | C _{IN} | S1, S1, FBIN | | 7 | | pF |

AC Electrical Characteristics

VDD = 3.3V ±10%, Temp 0 to +70°/ -40 to +85° C

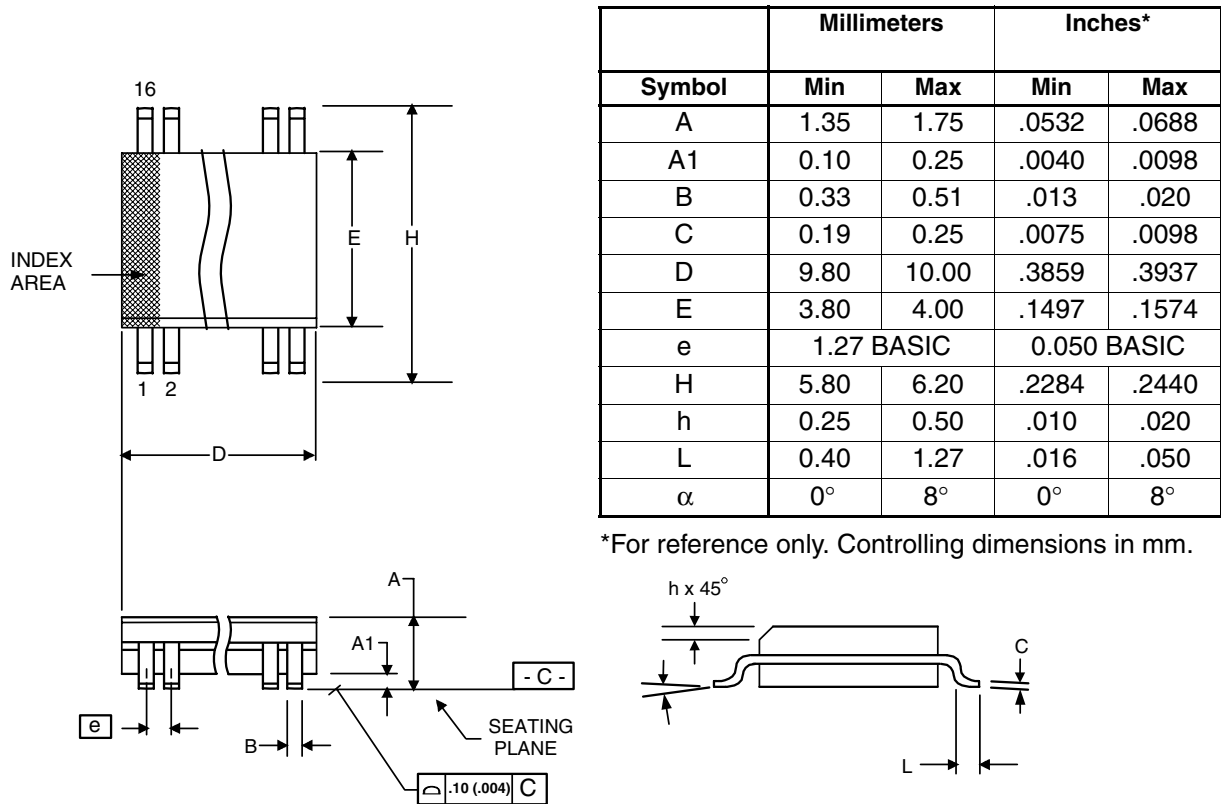
| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|-------------------|--|------|------|-----------|-------|
| Input Frequency | | FBIN to CLKA1 S1=S2=1 | 20 | | 133. 3 | MHz |
| Output Frequency | | FBIN to CLKA1 S1=S2=1 | 20 | | 133. 3 | MHz |
| Output Rise Time | t _{OR} | 0.8 to 2.0 V, C _L =30 pF | | | 1.5 | ns |
| Output Fall Time | t _{OF} | 0.8 to 2.0 V, C _L =30 pF | | | 1.5 | ns |
| Output Clock Duty Cycle | | at 1.4V | 40 | 50 | 60 | % |
| Device to Device skew, equally loaded | | rising edges at VDD/2 | | | 700 | ps |
| Output to Output skew, equally loaded | | rising edges at VDD/2 | | | 200 | ps |
| Maximum Absolute Jitter | | | | 300 | | ps |
| Cycle to Cycle Jitter | | 30 pF loads 66.67 MHz outputs | | | 400 | ps |
| | | 15 pF loads 66.67 MHz outputs | | | 400 | ps |
| Skew from Output Bank A to Output Bank B | | All outputs equally loaded | | | 400 | ps |
| Delay CLKIN Rising Edge to FBIN Rising Edge | | measured at VDD/2 | | | ±250 | ps |
| PLL Lock Time | t _{LOCK} | Stable power supply, valid clocks on CLKIN, FBIN | | | 1 | ms |

Thermal Characteristics

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|-----------------|----------------|------|------|------|-------|
| Thermal Resistance Junction to Ambient | θ _{JA} | Still air | | 120 | | °C/W |
| | θ _{JA} | 1 m/s air flow | | 115 | | °C/W |
| | θ _{JA} | 3 m/s air flow | | 105 | | °C/W |
| Thermal Resistance Junction to Case | θ _{JC} | | | 58 | | °C/W |

Package Outline and Package Dimensions (16-pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---------------------|-------------|--------------------|-------------|---------------|
| MK2308S-2LF | MK2308S-2LF | Tubes | 16-pin SOIC | 0 to 70° C |
| MK2308S-2LFT | MK2308S-2LF | Tape and Reel | 16-pin SOIC | 0 to 70° C |
| MK2308S-2ILF | 2308S-2ILF | Tubes | 16-pin SOIC | -40 to +85° C |
| MK2308S-2ILFT | 2308S-2ILF | Tape and Reel | 16-pin SOIC | -40 to +85° C |

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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