

Description

The MK5811C device generates a low EMI output clock from a clock or crystal input. The device is designed to dither a high emissions clock to lower EMI in consumer applications. Using IDT's proprietary mix of analog and digital Phase Locked Loop (PLL) technology, the device spreads the frequency spectrum of the output and reduces the frequency amplitude peaks by several dB. The MK5811C offers both centered and down spread from a high-speed clock input.

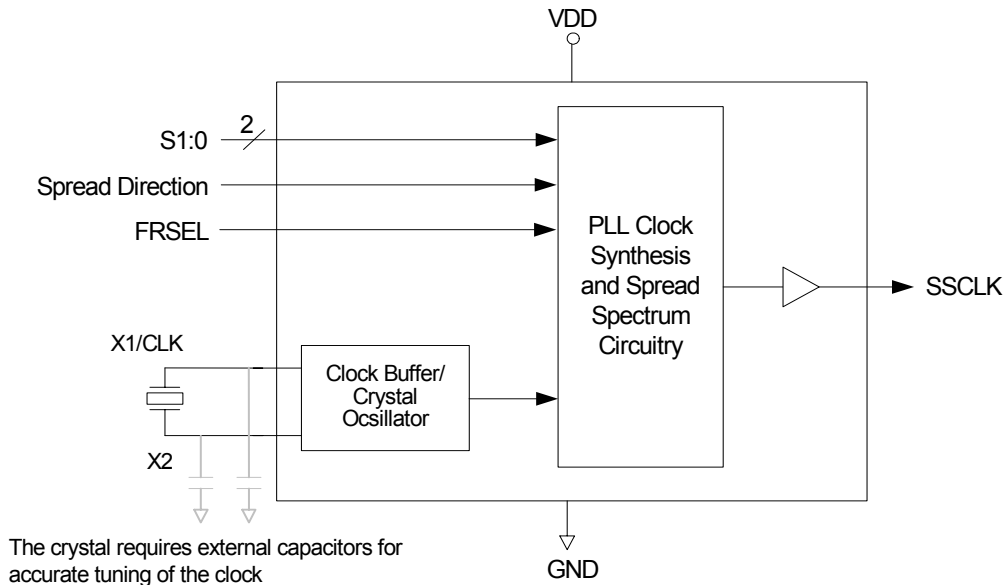
For different multiplier configurations, use the MK5812 (2x) or MK5814C (4x).

IDT offers many other clocks for computers and computer peripherals. Consult IDT when you need to remove crystals and oscillators from your board.

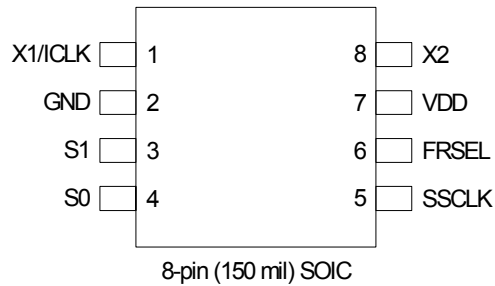
Features

- Packaged in 8-pin SOIC
- Pb (lead) free package, RoHS compliant
- Provides a spread spectrum output clock
- Supports printers and flat panel controllers
- Accepts a clock or crystal input (provides same frequency dithered output)
- Input frequency range of 4 to 32 MHz
- Output frequency range of 4 to 32 MHz
- 1X frequency multiplication
- Center and down spread
- Peak reduction by 8 dB to 16 dB typical on 3rd through 19th odd harmonics
- Low EMI feature can be disabled
- Operating voltage of 3.3 V
- Advanced, low-power CMOS process
- Industrial temperature range available (-40 to +85°C)

Block Diagram



Pin Assignment



Spread Direction and Spread Percentage

| S1 Pin 3 | S0 Pin 4 | Spread Direction | Spread Percentage |
|-------------|-------------|---------------------|----------------------|
| 0 | 0 | Center | ±1.4 |
| 0 | M | Center | ±1.1 |
| 0 | 1 | Center | ±0.6 |
| M | 0 | Center | ±0.5 |
| M | M | No Spread | - |
| M | 1 | Down | -1.6 |
| 1 | 0 | Down | -2.0 |
| 1 | M | Down | -0.7 |
| 1 | 1 | Down | -3.0 |

0 = connect to GND

M = unconnected (floating)

1 = connect directly to VDD

Frequency Selection

| Product | FRSEL (pin 6) | Input Freq. Range | Multiplier | Output Freq. Range |
|----------------------|------------------|----------------------|------------|-----------------------|
| MK5811C | 0 | 4.0 to 8.0 MHz | X1 | 4.0 to 8.0 MHz |
| | 1 | 8.0 to 16.0MHz | X1 | 8.0 to 16.0MHz |
| | M | 16.0 to 32.0MHz | X1 | 16.0 to 32.0MHz |
| MK5812 ¹ | 0 | 4.0 to 8.0 MHz | X2 | 8.0 to 16.0MHz |
| | 1 | 8.0 to 16.0MHz | X2 | 16.0 to 32.0MHz |
| | M | 16.0 to 32.0MHz | X2 | 32.0 to 64.0MHz |
| MK5814C ¹ | 0 | 4.0 to 8.0 MHz | X4 | 16.0 to 32.0MHz |
| | 1 | 8.0 to 16.0MHz | X4 | 32.0 to 64.0MHz |
| | M | 16.0 to 32.0MHz | X4 | 64.0 to 128MHz |

0 = connect to GND

M = unconnected (floating)

1 = connect directly to VDD

Note 1: The information in this datasheet does not apply to the MK5812 and MK5814C as each have independent datasheets available at www.idt.com.

Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|------------|----------|----------|---|
| 1 | X1/ICLK | Input | Connect to 4-32 MHz crystal or clock. |
| 2 | GND | Power | Connect to ground. |
| 3 | S1 | Input | Function select 1 input. Selects spread amount and direction per table above. (default-internal mid-level). |
| 4 | S0 | Input | Function select 0 input. Selects spread amount and direction per table above. (default-internal mid-level). |
| 5 | SSCLK | Output | Clock output with Spread spectrum |
| 6 | FRSEL | Input | Function select for input frequency range. Default to mid level "M". |
| 7 | VDD | Power | Connect to +3.3 V. |
| 8 | X2 | XO | Crystal connection to 4-32 MHz crystal. Leave unconnected for clock |

External Components

The MK5811C requires a minimum number of external components for proper operation.

Decoupling Capacitor

A decoupling capacitor of 0.01 μ F must be connected between VDD and GND on pins 7 and 2. Connect the capacitor as close to these pins as possible. For optimum device performance, mount the decoupling capacitor on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Series Termination Resistor

Use series termination when the PCB trace between the clock output and the load is over 1 inch. To series terminate a 50 Ω trace (a commonly used trace impedance), place a 20 Ω resistor in series with the clock line. Place the resistor as close to the clock output pin as possible. The nominal impedance of the clock output is 30 Ω .

Tri-level Select Pin Operation

The S1 and S0 select pins are tri-level, meaning that they have three separate states to make the selections shown in the table on page 2. To select the M (mid) level, the connection to these pins must be eliminated by either floating them originally, or tri-stating the GPIO pins which drive the select pins.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, observe the following guidelines:

- 1) Mount the 0.01 μ F decoupling capacitor on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitor and VDD pin. The PCB trace to the VDD pin and the PCB trace to the ground via should be kept as short as possible.
- 2) To minimize EMI, place the 20 Ω series-termination resistor (if needed) close to the clock output.
- 3) An optimum layout is one with all components on the same side of the board, thus minimizing vias through other signal layers. Other signal traces should be routed away from the MK5811C device. This includes signal traces located underneath the device, or on layers adjacent to the ground plane layer used by the device.

Crystal Information

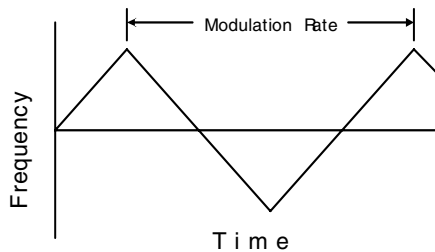
The crystal used should be a fundamental mode (do not use third overtone), parallel resonant crystal. To optimize the initial accuracy, connect crystal capacitors from pins X1 to ground and X2 to ground. The value of these capacitors is given by the following equation:

$$\text{Crystal caps (pF)} = (C_L - 6) \times 2$$

In the equation, C_L is the crystal load capacitance. For example, a crystal with a 16 pF load capacitance uses two 20 pF [(16-6) x 2] capacitors.

Spread Spectrum Profile

The MK5811C is a low EMI clock generator using a optimized frequency slew rate algorithm to facilitate down stream tracking of zero delay buffers and other PLL devices.



Modulation Rate

Spread Spectrum Clock Generators utilize frequency modulation (FM) to distribute energy over a specific band of frequencies. The maximum frequency of the clock (f_{max}) and minimum frequency of the clock (f_{min}) determine this band of frequencies. The time required to transition from f_{min} to f_{max} and back to f_{min} is the period of the Modulation Rate. The Modulation Rate of SSCG clocks are generally referred to in terms of frequency, or

$$f_{mod} = 1/T_{mod}$$

The input clock frequency, f_{in} , and the internal divider determine the Modulation Rate.

The Spread Spectrum modulation Rate, f_{mod} , is given by the following formula:

$$f_{mod} = f_{in}/DR$$

where; f_{mod} is the Modulation Rate, f_{in} is the Input Frequency and DR is the Divider Ratio as given in the "Modulation Rate Divider Ratios" table. Notice that Input Frequency Range is set by FRSEL.

Modulation Rate Divider Ratios

| FRSEL | Input Freq. Range | Divider Ratio (DR) |
|-------|-------------------|--------------------|
| 0 | 4 to 8 MHz | 128 |
| 1 | 8 to 16 MHz | 256 |
| M | 16 to 32 MHz | 512 |

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK5811C. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device, at these or any other conditions, above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|-------------------------------|---------------------|
| Supply Voltage, VDD | 7 V |
| All Inputs and Outputs | -0.5 V to VDD+0.5 V |
| Ambient Operating Temperature | -40 to +85° C |
| Storage Temperature | -65 to +150° C |
| Junction Temperature | 125° C |
| Soldering Temperature | 260° C |

Recommended Operation Conditions

| Parameter | Min. | Typ. | Max. | Units |
|---|------|------|------|-------|
| Ambient Operating Temperature | -40 | | +85 | °C |
| Power Supply Voltage (measured in respect to GND) | +3.0 | | 3.63 | V |

DC Electrical Characteristics

Unless stated otherwise, VDD = 3.3 V ±10%, Ambient Temperature -40 to +85° C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--------------------------|------------------|-------------------------------|---------|--------|---------|-------|
| Operating Voltage | VDD | | 3.0 | 3.3 | 3.63 | V |
| Supply Current | IDD | No load, at 3.3 V, Fin=12 MHz | | 23 | 25 | mA |
| | | No load, at 3.3 V, Fin=24 MHz | | | 30 | mA |
| | | No load, at 3.3 V, Fin=32 MHz | | | 35 | mA |
| Input High Voltage | V _{IH} | | 0.85VDD | VDD | VDD | V |
| Input middle Voltage | V _{IHM} | | 0.4VDD | 0.5VDD | 0.6VDD | V |
| Input Low Voltage | V _{IL} | | 0.0 | 0.0 | 0.15VDD | V |
| Output High Voltage | V _{OH} | CMOS, I _{OH} = 12 mA | 2.4 | | | V |
| Output High Voltage | V _{OH} | I _{OH} = 24 mA | 2.0 | | | V |
| Output Low Voltage | V _{OL} | I _{OL} = -12 mA | | | 0.4 | V |
| | | I _{OL} = -24 mA | | | 1.2 | V |
| Input Capacitance | C _{IN1} | S0, S1, FRSEL pins | | 4 | 6 | pF |
| | C _{IN2} | X1, X2 pins | | 6 | 9 | pF |
| Nominal Output Impedance | Z _O | | | 30 | | Ω |

AC Electrical Characteristics

Unless stated otherwise, VDD = 3.3 V ±10%, Ambient Temperature 0 to +85° C, CL = 15 pF

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|------------------------------------|----------------|--------------------------|------|---------|------|-------|
| Input Clock Frequency | | | 4 | 12 | 32 | MHz |
| Output Clock Frequency | | | 4 | 12 | 32 | MHz |
| Input Clock Duty Cycle | | Time above VDD/2 | 40 | | 60 | % |
| Output Clock Duty Cycle | | Time above 1.5 V | 45 | 50 | 55 | % |
| Cycle-to-cycle Jitter ¹ | | Fin= 4 MHz, Fout = 4 MHz | | 350 | 800 | ps |
| Cycle-to-cycle Jitter ¹ | | Fin= 8 MHz, Fout = 8 MHz | | 250 | 450 | ps |
| Output Rise Time | t _R | 0.4 to 2.4 V | | 4.4 | | ns |
| Output Fall Time | t _F | 2.4 to 0.4 V | | 3.57 | | ns |
| EMI Peak Frequency Reduction | | | | 8 to 16 | | dB |

Note 1: Spread is enabled.

AC Electrical Characteristics

Unless stated otherwise, VDD = 3.3 V ±10%, Ambient Temperature -40 to +85° C, CL = 15 pF

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|------------------------------------|----------------|------------------|------|---------|------|-------|
| Input Clock Frequency | | | 4 | 12 | 32 | MHz |
| Output Clock Frequency | | | 4 | 12 | 32 | MHz |
| Input Clock Duty Cycle | | Time above VDD/2 | 40 | | 60 | % |
| Output Clock Duty Cycle | | Time above 1.5 V | 45 | 50 | 55 | % |
| Cycle-to-cycle Jitter ² | | Fin = 6 MHz | | 450 | 650 | ps |
| | | Fin = 12 MHz | | 300 | 630 | ps |
| | | Fin = 24 MHz | | 300 | 520 | ps |
| Output Rise Time | t _R | 0.4 to 2.4 V | | 4.4 | | ns |
| Output Fall Time | t _F | 2.4 to 0.4 V | | 3.57 | | ns |
| EMI Peak Frequency Reduction | | | | 8 to 16 | | dB |

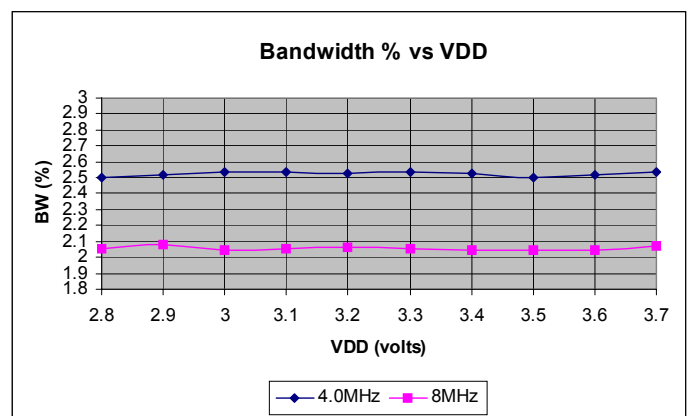
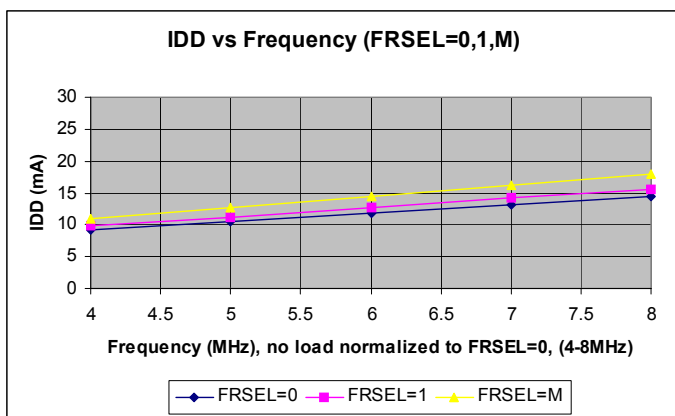
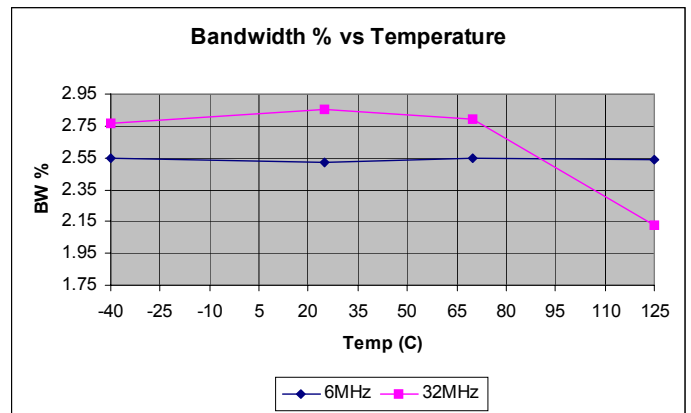
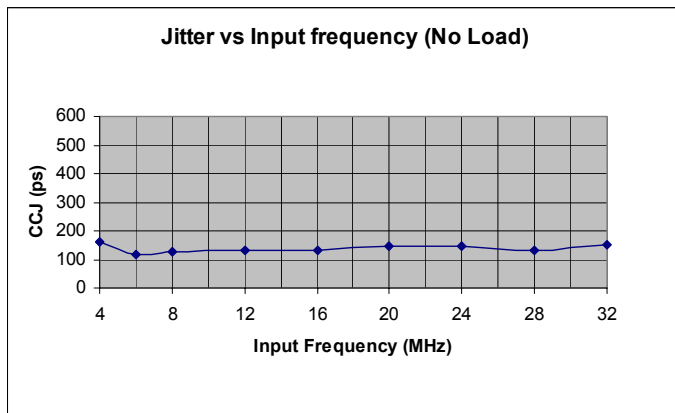
Note 2: Spread is enabled.

Thermal Characteristics for 8-pin SOIC

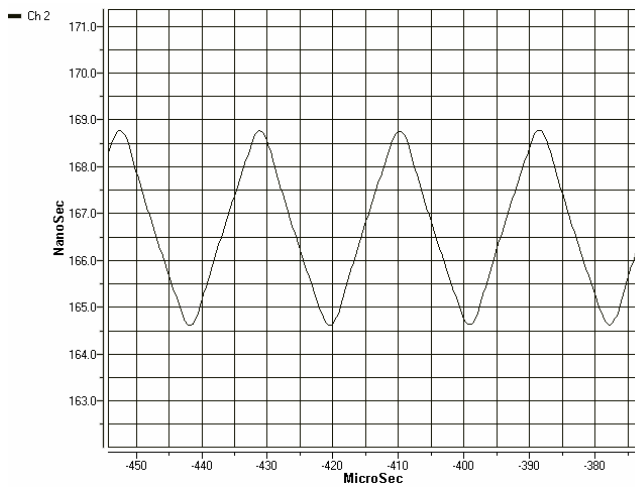
| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|---------------|----------------|------|------|------|----------------------|
| Thermal Resistance Junction to Ambient | θ_{JA} | Still air | | 150 | | $^{\circ}\text{C/W}$ |
| | θ_{JA} | 1 m/s air flow | | 140 | | $^{\circ}\text{C/W}$ |
| | θ_{JA} | 3 m/s air flow | | 120 | | $^{\circ}\text{C/W}$ |
| Thermal Resistance Junction to Case | θ_{JC} | | | 40 | | $^{\circ}\text{C/W}$ |

Characteristic Curves

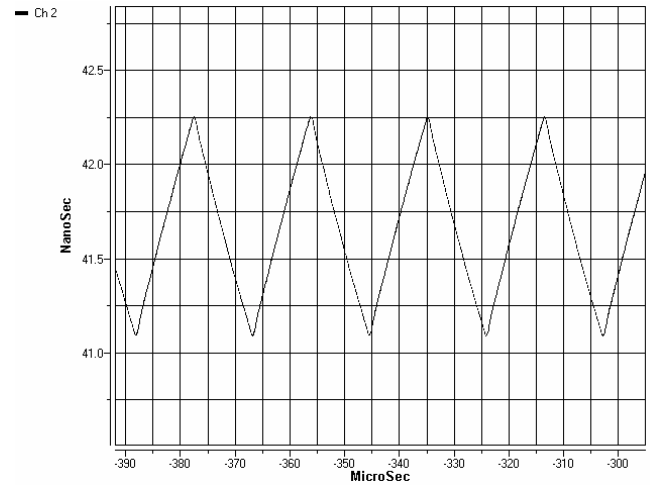
The following curves determine the characteristic behavior of the MK5811C when tested over a number of environmental and application-specific parameters. These are typical performance curves and are not meant to replace any parameter specified in DC and AC Characteristics tables.



SSCG Profiles

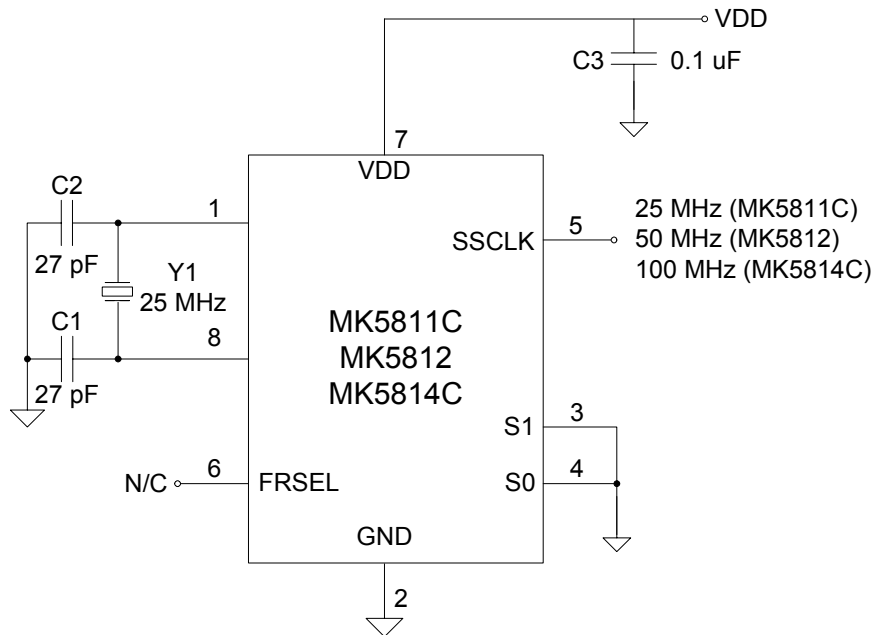


Min: 5.925 MHz Max: 6.075 MHz
 Rate: 46.88 kHz Pk-Pk: Jitter: 130 ps
 Xin = 6.0 MHz SSCLK1 = 6.0 MHz
 S1, S0 = 0
 FRSEL = 0 P/N: MK5811C



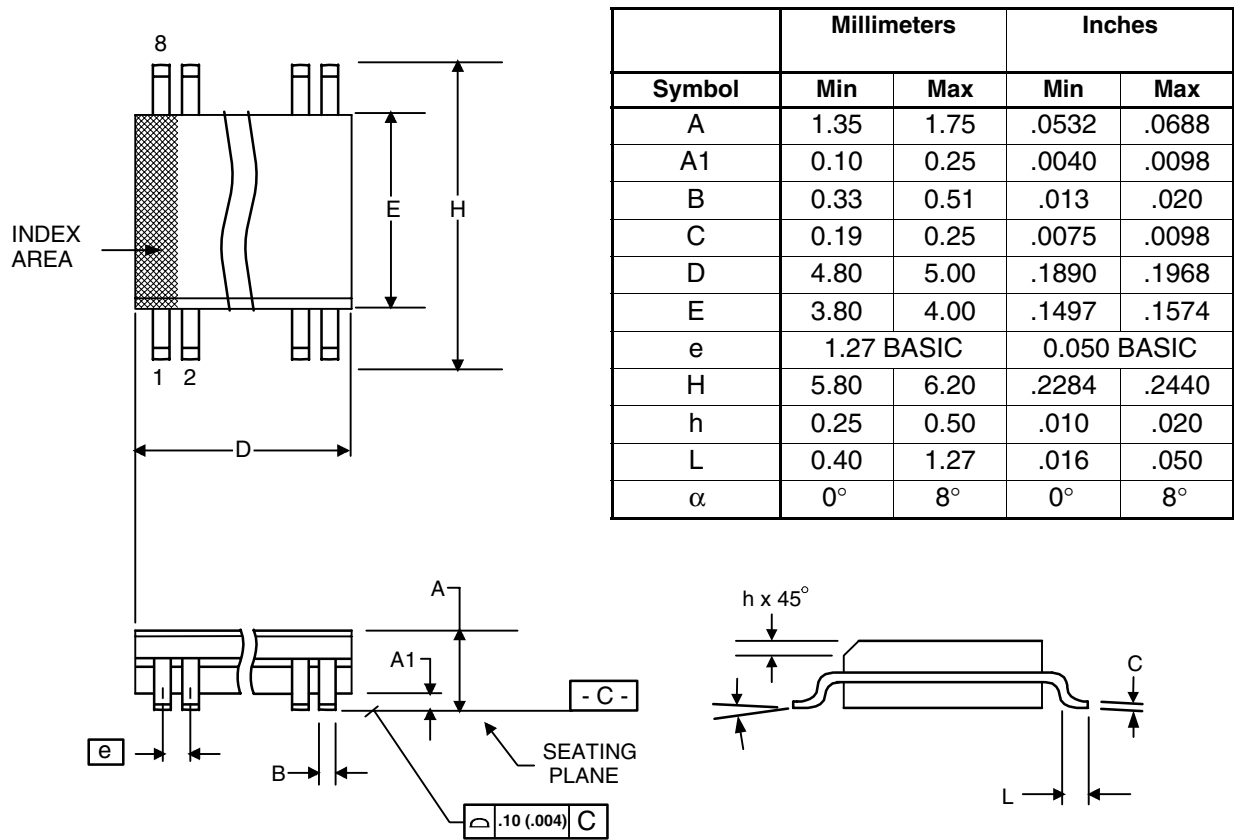
Min: 23.67 MHz Max: 24.33 MHz
 Rate: 46.89 kHz Pk-Pk: Jitter: 365 ps
 Xin = 24.0 MHz SSCLK1 = 24.0 MHz
 S1, S0 = 0
 FRSEL = M P/N: MK5811C

Application Schematic



Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---------------------|----------|--------------------|------------|---------------|
| MK5811CMLF | 5811CML | Tubes | 8-pin SOIC | 0 to +85° C |
| MK5811CMLFT | 5811CML | Tape and Reel | 8-pin SOIC | 0 to +85° C |
| MK5811CMILF | 5811CMIL | Tubes | 8-pin SOIC | -40 to +85° C |
| MK5811CMILFT | 5811CMIL | Tape and Reel | 8-pin SOIC | -40 to +85° C |

“LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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