The MPC941 is a 1:27 low voltage clock distribution chip. The device features the capability to select either a differential LVPECL or an LVCMOS compatible input. The 27 outputs are LVCMOS compatible and feature the drive strength to drive 50 Ω series or parallel terminated transmission lines. With output-to-output skews of 250 ps, the MPC941 is ideal as a clock distribution chip for the most demanding of synchronous systems. For a similar product with a smaller number of outputs, please consult the MPC940 data sheet.

- LVPECL or LVCMOS Clock Input
- 250 ps Maximum Output-to-Output Skew
- Drives Up to 54 Independent Clock Lines
- Maximum Output Frequency of 250 MHz
- High Impedance Output Enable
- Extended Temperature Range: –40°C to +85°C
- 48-Lead LQFP Packaging, Pb-free
- 3.3 V or 2.5 V V_{CC} Supply Voltage

LOW VOLTAGE 3.3 V/2.5 V
1:27 CLOCK
DISTRIBUTION CHIP

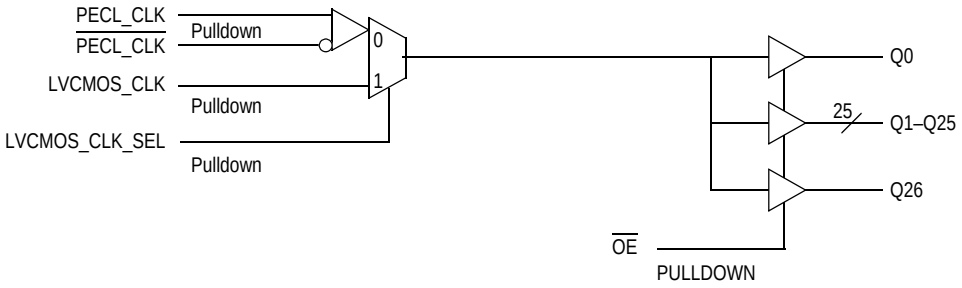
AE SUFFIX
48-LEAD LQFP PACKAGE
Pb-FREE PACKAGE
CASE 932-03

With a low output impedance, in both the HIGH and LOW logic states, the output buffers of the MPC941 are ideal for driving series terminated transmission lines. More specifically, each of the 27 MPC941 outputs can drive two series terminated 50 Ω transmission lines. With this capability, the MPC941 has an effective fanout of 1:54. With this level of fanout, the MPC941 provides enough copies of low skew clocks for most high performance synchronous systems.

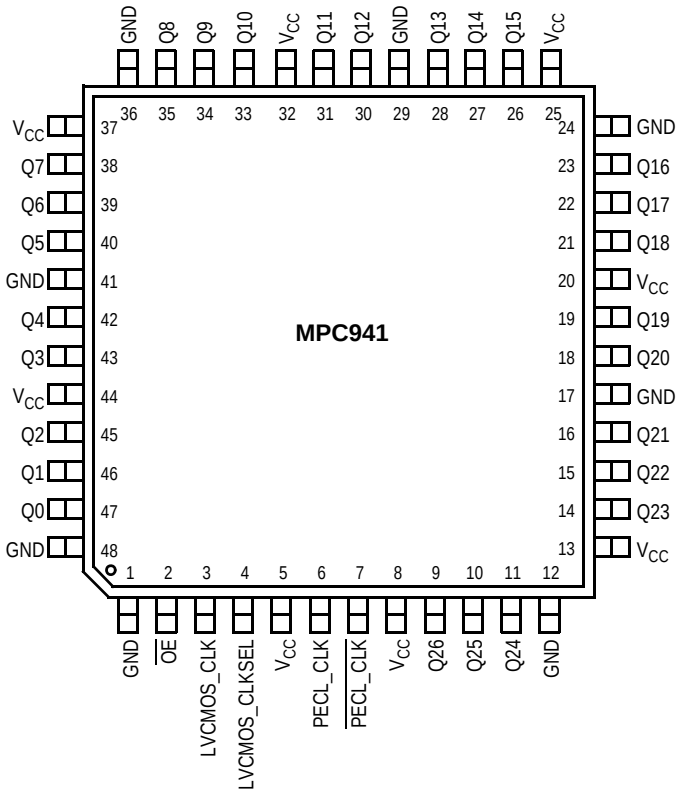
The differential LVPECL inputs of the MPC941 allow the device to interface directly with an LVPECL fanout buffer like the MC100EP111 to build very wide clock fanout trees or to couple to a high frequency clock source. The LVCMOS input provides a more standard interface for applications requiring only a single clock distribution chip at relatively low frequencies. In addition, the two clock sources can be used as a test clock interface as well as the primary system clock. A logic HIGH on the LVCMOS_CLK_Sel pin will select the LVCMOS level clock input.

The MPC941 is fully 3.3 V and 2.5 V compatible. The 48-lead LQFP package was chosen to optimize performance, board space and cost of the device. The 48-lead LQFP has a 7x7 mm body size.

LOGIC DIAGRAM



Pinout: 48-Lead TQFP (Top View)



FUNCTION TABLE

LVCMOS_CLK_SEL	Input
0	PECL_CLK
1	LVCMOS_CLK

Table 1. Pin Configuration

Pin	I/O	Type	Function
PECL_CLK, PECL_CLK	Input	LVPECL	LVPECL differential reference clock inputs
LVCMOS_CLK	Input	LVCMOS	Alternative reference clock input
LVCMOS_CLK_SEL	Input	LVCMOS	Input reference clock select
OE	Input	LVCMOS	Output tristate control
GND		Supply	Negative voltage supply output bank (GND)
V_{CC}		Supply	Positive voltage supply
Q0–Q26	Output	LVCMOS	Clock outputs

Table 2. Absolute Maximum Ratings(1)

Symbol	Characteristics	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	3.6	V
V_{IN}	DC Input Voltage	–0.3	V_{CC}+0.3	V
V_{OUT}	DC Output Voltage	–0.3	V_{CC}+0.3	V
I_{IN}	DC Input Current		±20	mA
I_{OUT}	DC Output Current		±50	mA
T_S	Storage Temperature	–40	125	°C

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 3. DC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = –40 to +85°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	LVCMOS_CLK	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage	LVCMOS_CLK	–0.3		0.8	V	LVCMOS
I_{IN}	Input Current				±120(1)	µA	
V_{PP}	Peak-to-Peak Input Voltage	PECL_CLK, $\overline{\text{PECL\_CLK}}$	500			mV	LVPECL
V_{CMR}	Common Mode Range	PECL_CLK, $\overline{\text{PECL\_CLK}}$	1.2		V_{CC} –0.8	V	LVPECL
V_{OH}	Output High Voltage		2.4			V	I_{OH} = –24 mA(2)
V_{OL}	Output Low Voltage				0.55 0.40	V V	I_{OL} = 24 mA(2) I_{OL} = 12 mA
I_{OZ}	Output Tristate Leakage Current				100	µA	
Z_{OUT}	Output Impedance			14 – 17		Ω	
C_{PD}	Power Dissipation Capacitance			7-8	10	pF	Per Output
C_{IN}	Input Capacitance			4.0		pF	
I_{CCQ}	Maximum Quiescent Supply Current				5	mA	All V_{CC} Pins
V_{TT}	Output Termination Voltage			V_{CC} ÷ 2		V	

1. Input pull-up / pull-down resistors influence input current.
2. The MPC941 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50 Ω series terminated transmission lines.

Table 4. AC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = –40 to +85°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{MAX}	Maximum Output Frequency		0		250[2]	MHz	
t_r, t_f	LVCMOS_CLK Input Rise/Fall Time				1.0[3]	ns	0.8 to 2.0 V
t_{PLH} t_{PHL}	Propagation Delay	PECL_CLK to any Q LVCMOS_CLK to any Q	1.2 0.9	1.8 1.5	2.6 2.3	ns ns	
$t_{PLZ, HZ}$	Output Disable Time					ns	
$t_{PZL, LZ}$	Output Enable Time					ns	
$t_{sk(O)}$	Output-to-Output Skew	PECL_CLK to any Q LVCMOS_CLK to any Q		125 125	250 250	ps	
$t_{sk(PP)}$	Device-to-Device Skew	PECL_CLK to any Q LVCMOS_CLK to any Q			1000 1000	ps ps	For a given T_A and V_{CC}, any Q
$t_{sk(PP)}$	Device-to-Device Skew	PECL_CLK to any Q LVCMOS_CLK to any Q			1400 1400	ps ps	For any T_A, V_{CC} and Q
DC_Q	Output Duty Cycle	PECL_CLK to any Q LVCMOS_CLK to any Q	45 45	50 50	60 55	% %	DC_{REF} = 50% DC_{REF} = 50%
t_r, t_f	Output Rise/Fall Time		0.2		1.0	ns	0.55 to 2.4 V

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. AC characteristics are guaranteed up to fmax. Please refer to applications section for information on power consumption versus operating frequency and thermal management.
3. Fast input signal transition times are required to maintain part-to-part skew specification. If part-to-part skew is not critical to the application, signal transition times smaller than 3 ns can be applied to the MPC941.

Table 5. DC Characteristics (V_{CC} = 2.5 V ± 5%, T_A = –40 to +85°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	LVCMOS_CLK	1.7		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage	LVCMOS_CLK	–0.3		0.7	V	LVCMOS
I_{IN}	Input Current				±120[1]	µA	
V_{PP}	Peak-to-Peak Input Voltage	PECL_CLK, $\overline{\text{PECL\_CLK}}$	500			mV	LVPECL
V_{CMR}	Common Mode Range	PECL_CLK, $\overline{\text{PECL\_CLK}}$	1.1		V_{CC} – 0.7	V	LVPECL
V_{OH}	Output High Voltage		1.8			V	I_{OH} = –15 mA[2]
V_{OL}	Output Low Voltage				0.6	V	I_{OL} = 15 mA[2]
I_{OZ}	Output Tristate Leakage Current				100	µA	
Z_{OUT}	Output Impedance			18 – 20		Ω	
C_{PD}	Power Dissipation Capacitance			7 – 8	10	pF	Per Output
C_{IN}	Input Capacitance			4.0		pF	
I_{CCQ}	Maximum Quiescent Supply Current				5	mA	All V_{CC} Pins
V_{TT}	Output Termination Voltage			V_{CC} ÷ 2		V	

1. Input pull-up / pull-down resistors influence input current.
2. The MPC941 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50 Ω series terminated transmission lines.

Table 6. AC Characteristics (V_{CC} = 2.5 V ± 5%, T_A = –40 to +85°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{MAX}	Maximum Output Frequency		0		250[2]	MHz	
t_r, t_f	LVCMOS_CLK Input Rise/Fall Time				1.0[3]	ns	0.7 to 1.7 V
t_{PLH} t_{PHL}	Propagation Delay	PECL_CLK to any Q LVCMOS_CLK to any Q	1.3 1.0	2.1 1.8	2.9 2.6	ns ns	
$t_{PLZ, HZ}$	Output Disable Time					ns	
$t_{PZL, LZ}$	Output Enable Time					ns	
$t_{sk(O)}$	Output-to-Output Skew	PECL_CLK to any Q LVCMOS_CLK to any Q		125 125	250 250	ps	
$t_{sk(PP)}$	Device-to-Device Skew	PECL_CLK to any Q LVCMOS_CLK to any Q			1200 1200	ps ps	For a given T_A and V_{CC}, any Q
$t_{sk(PP)}$	Device-to-Device Skew	PECL_CLK to any Q LVCMOS_CLK to any Q			1600 1600	ps ps	For any T_A, V_{CC} and Q
DC_Q	Output Duty Cycle	PECL_CLK to any Q LVCMOS_CLK to any Q	45 45	50 50	60 55	% %	DC_{REF} = 50% DC_{REF} = 50%
t_r, t_f	Output Rise/Fall Time		0.2		1.0	ns	0.6 to 1.6 V

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. AC characteristics are guaranteed up to f_{MAX}. Please refer to the applications section for information on power consumption versus operating frequency and thermal management.
3. Fast input signal transition times are required to maintain part-to-part skew specification. If part-to-part skew is not critical to the application, signal transition times smaller than 3 ns can be applied to the MPC941.

APPLICATIONS INFORMATION

Driving Transmission Lines

The MPC941 clock driver was designed to drive high-speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user, the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20 Ω, the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines, the reader is referred to Freescale application note AN1091 in the Timing Solutions data book (DL207/D).

In most high performance clock networks, point-to-point distribution of signals is the method of choice. In a point-to-point scheme, either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to V_{CC}/2. This technique draws a fairly high level of DC current, and thus, only a single terminated line can be driven by each output of the MPC941 clock driver. For the series terminated case, however, there is no DC current draw; thus, the outputs can drive multiple series terminated lines. Figure 1 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme, the fanout of the MPC941 clock driver is effectively doubled due to its capability to drive multiple lines.

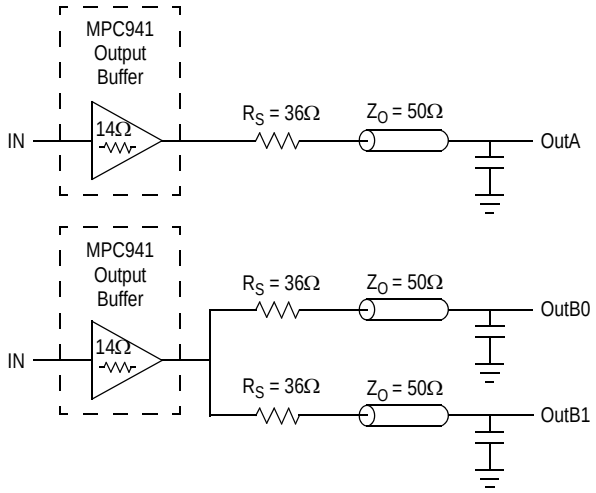


Figure 1. Single versus Dual Transmission Lines

The waveform plots of Figure 2 show the simulation results of an output driving a single line vs two lines. In both cases, the drive capability of the MPC941 output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations, a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC941. The output waveform in Figure 2 shows a step in the waveform. This step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_O / (R_S + R_O + Z_O))$$
$$Z_O = 50\ \Omega \,||\, 50\ \Omega$$
$$R_S = 36\ \Omega \,||\, 36\ \Omega$$
$$R_O = 14\ \Omega$$
$$V_L = 3.0\ (25 / (18 + 14 + 25) = 3.0\ (25 / 57)$$
$$= 1.31\ V$$

At the load end, the voltage will double, due to the near unity reflection coefficient, to 2.5 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case, 4.0 ns).

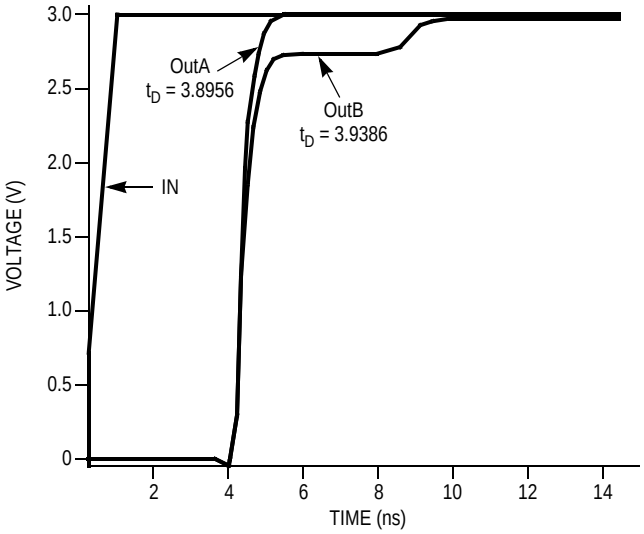
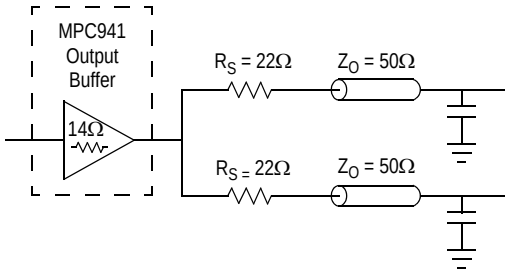


Figure 2. Single versus Dual Waveforms

Since this step is well above the threshold region, it will not cause any false clock triggering; however, designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines, the situation in Figure 3 should be used. In this case, the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance, the line impedance is perfectly matched.



14Ω + 22Ω || 22Ω = 50Ω ||50Ω
25Ω = 25Ω

Figure 3. Optimized Dual Line Termination

Power Consumption of the MPC941 and Thermal Management

The MPC941 AC specification is guaranteed for the entire operating frequency range up to 250 MHz. The MPC941 power consumption and the associated long-term reliability may decrease the maximum frequency limit, depending on operating conditions such as clock frequency, supply voltage, output loading, ambient temperture, vertical convection and thermal conductivity of package and board. This section describes the impact of these parameters on the junction temperature and gives a guideline to estimate the MPC941 die junction temperature and the associated device reliability. For a complete analysis of power consumption as a function of operating conditions and associated long term device reliability, please refer to the Freescale application note AN1545. According the AN1545, the long-term device reliability is a function of the die junction temperature:

Table 7. Die Junction Temperature and MTBF

Junction Temperature (°C)	MTBF (Years)
100	20.4
110	9.1
120	4.2
130	2.0

Increased power consumption will increase the die junction temperature and impact the device reliability (MTBF). According to the system-defined tolerable MTBF, the die junction temperature of the MPC941 needs to be controlled, and the thermal impedance of the board/package should be optimized. The power dissipated in the MPC941 is represented in equation 1.

Where I_{CCQ} is the static current consumption of the MPC941, C_{PD} is the power dissipation capacitance per output. $(M)\Sigma C_L$ represents the external capacitive output load, and N is the number of active outputs (N is always 27 in case of the MPC941). The MPC941 supports driving transmission lines to maintain high signal integrity and tight timing parameters. Any transmission line will hide the lumped capacitive load at the end of the board trace, therefore, ΣC_L is zero for controlled transmission line systems and can be eliminated from equation 1. Using parallel termination output termination results in equation 2 for power dissipation.

In equation 2, P stands for the number of outputs with a parallel or thevenin termination. V_{OL}, I_{OL}, V_{OH} and I_{OH} are a function of the output termination technique, and DC_Q is the clock signal duty cyle. If transmission lines are used, ΣC_L is zero in equation 2 and can be eliminated. In general, the use of controlled transmission line techniques eliminates the impact of the lumped capacitive loads at the end lines and greatly reduces the power dissipation of the device. Equation 3 describes the die junction temperature T_J as a function of the power consumption.

Where R_{thja} is the thermal impedance of the package (junction to ambient), and T_A is the ambient temperature, according to Table 7, the junction temperature can be used to estimate the long-term device reliability. Further, combining equation 1 and equation 2 results in a maximum operating frequency for the MPC941 in a series terminated transmission line system.

$T_{J,MAX}$ should be selected according to the MTBF system requirements, and Table 7, R_{thja} can be derived from Table 8. The R_{thja} represent data based on 1S2P boards. Using 2S2P boards will result in a lower thermal impedance than indicated below.

Table 8. Thermal Package Impedance of the 48ld LQFP

Convection, LFPM	R_{thja} (1P2S board), K/W
Still air	78
100 lfpm	68
200 lfpm	59
300 lfpm	56
400 lfpm	54
500 lfpm	53

If the calculated maximum frequency is below 250 MHz, it becomes the upper clock speed limit for the given application conditions. The following eight derating charts describe the safe frequency operation range for the MPC941. The charts were calculated for a maximum tolerable die junction temperature of 110°C (120°C), corresponding to a estimated MTBF of 9.1 years (4 years), a supply voltage of either 3.3 V or 2.5 V, and series terminated transmission line or capacitive loading. Depending on a given set of these operating conditions and the available device convection, a decision on the maximum operating frequency can be made.

$$P_{TOT} = \left[I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left(N \cdot C_{PD} + \sum_{M} C_L \right) \right] \cdot V_{CC} \qquad \text{Equation 1}$$

$$P_{TOT} = V_{CC} \cdot \left[I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left(N \cdot C_{PD} + \sum_{M} C_L \right) \right] + \sum_{P} \left[DC_Q \cdot I_{OH} \cdot (V_{CC} - V_{OH}) + (1 - DC_Q) \cdot I_{OL} \cdot V_{OL} \right] \qquad \text{Equation 2}$$

$$T_J = T_A + P_{TOT} \cdot R_{thja} \qquad \text{Equation 3}$$

$$f_{CLOCK,MAX} = \frac{1}{C_{PD} \cdot N \cdot V_{CC}^2} \cdot \left[\frac{T_{j,MAX} - T_A}{R_{thja}} - (I_{CCQ} \cdot V_{CC}) \right] \qquad \text{Equation 4}$$

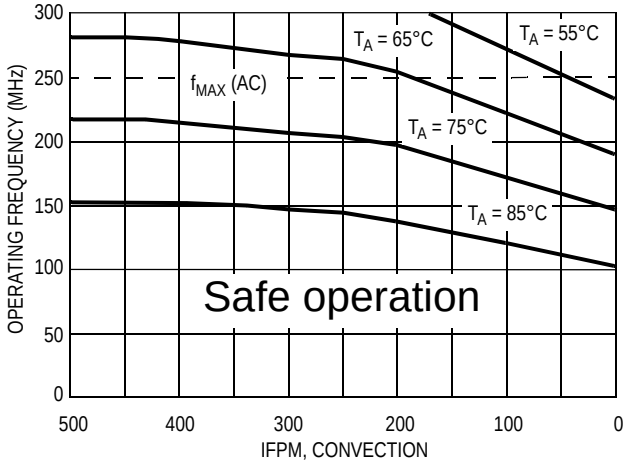


Figure 4. Maximum MPC941 frequency, V_{CC} = 3.3 V, MTBF 9.1 years, driving series terminated transmission lines

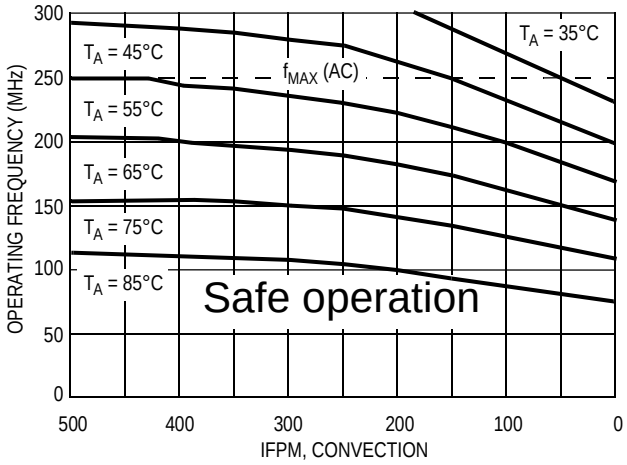


Figure 5. Maximum MPC941 frequency, V_{CC} = 3.3 V, MTBF 9.1 years, 4 pF load per line

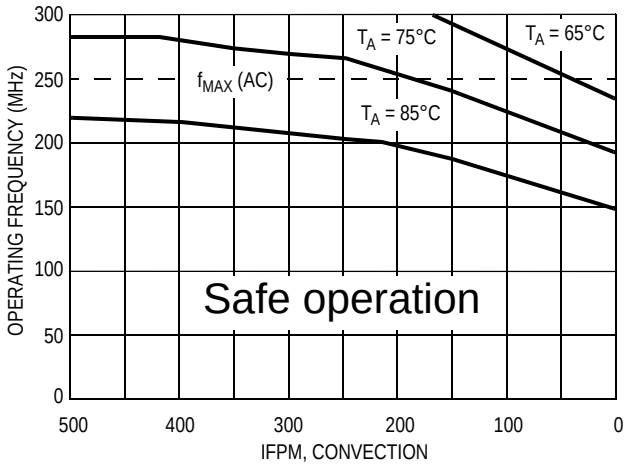


Figure 6. Maximum MPC941 frequency, V_{CC} = 3.3 V, MTBF 4 years, driving series terminated transmission lines

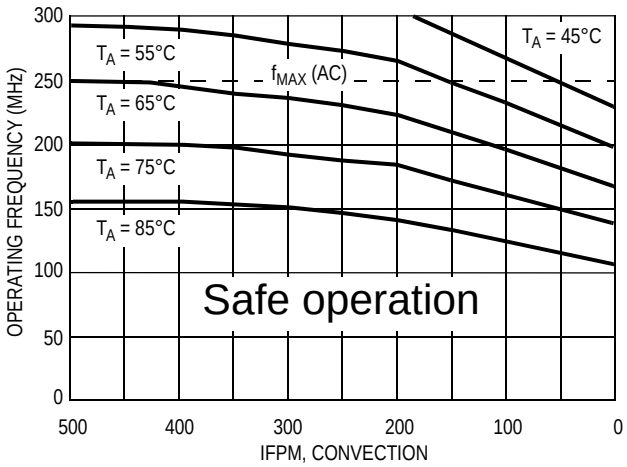


Figure 7. Maximum MPC941 frequency, V_{CC} = 3.3 V, MTBF 4 years, 4 pF load per line

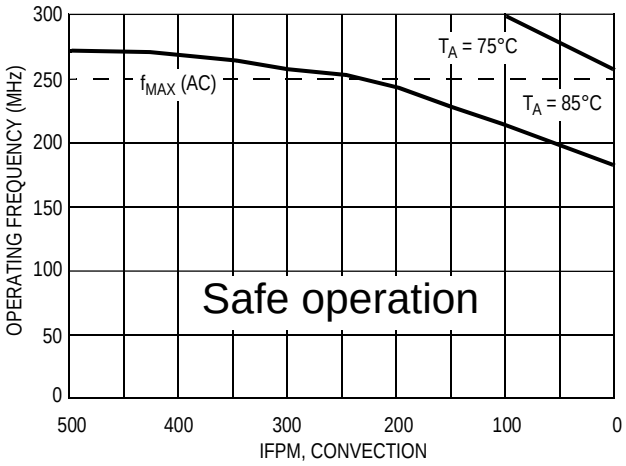


Figure 8. Maximum MPC941 frequency, V_{CC} = 2.5 V, MTBF 9.1 years, driving series terminated transmission lines

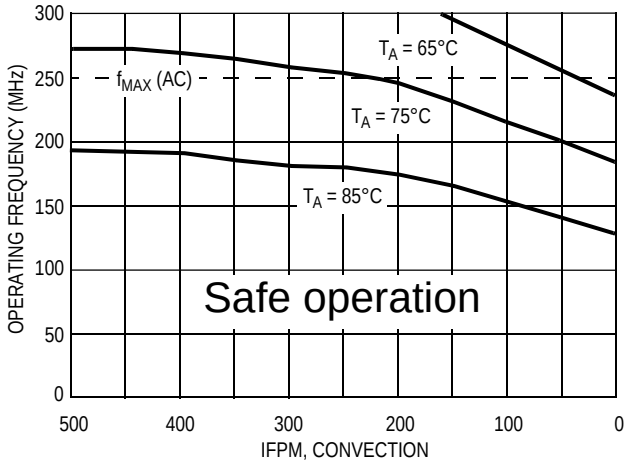


Figure 9. Maximum MPC941 frequency, V_{CC} = 2.5 V, MTBF 9.1 years, 4 pF load per line

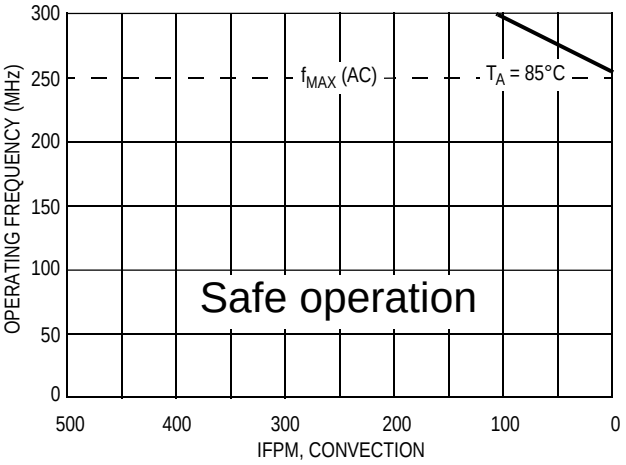


Figure 10. Maximum MPC941 frequency, V_{CC} = 2.5 V, MTBF 4 years, driving series terminated transmission lines

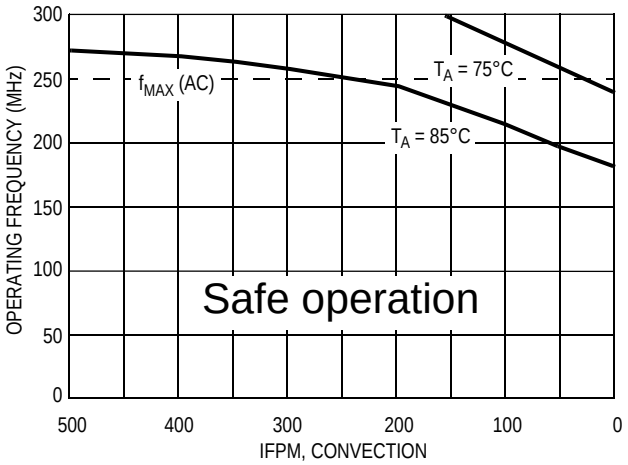


Figure 11. Maximum MPC941 frequency, V_{CC} = 2.5 V, MTBF 4 years, 4 pF load per line

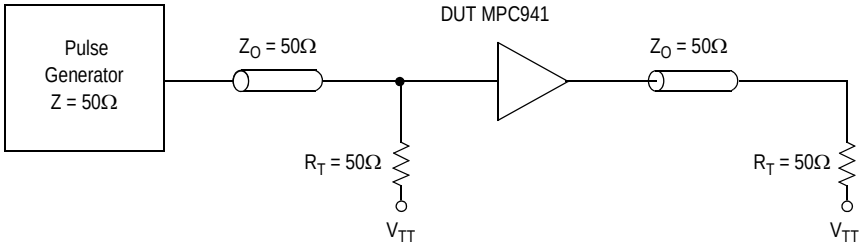


Figure 12. LVCMOS_CLK MPC941 AC Test Reference for V_{CC} = 3.3 V and V_{CC} = 2.5 V

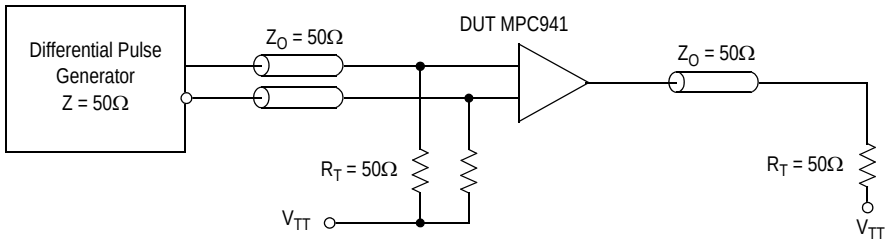


Figure 13. PECL_CLK MPC941 AC Test Reference for V_{CC} = 3.3 V and V_{CC} = 2.5 V

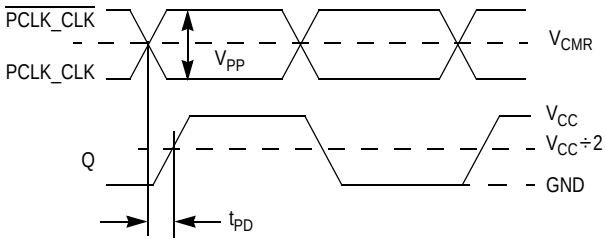


Figure 14. LVPECL Propagation Delay (t_{PD}) Test Reference

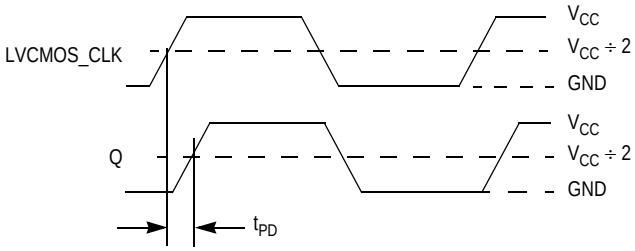
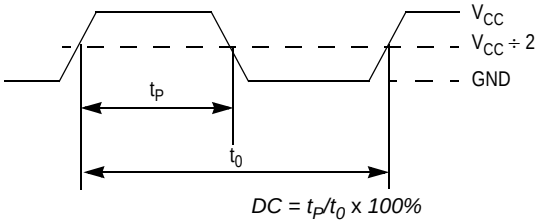
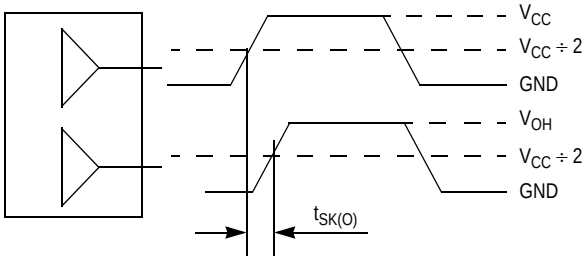


Figure 15. LVCMOS Propagation Delay (t_{PD}) Test Reference



The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 16. Output Duty Cycle (DC)



The pin-to-pin skew is defined as the worst case difference in propagation delay between any two similar delay path within a single device

Figure 17. Output-to-Output Skew $t_{SK(O)}$

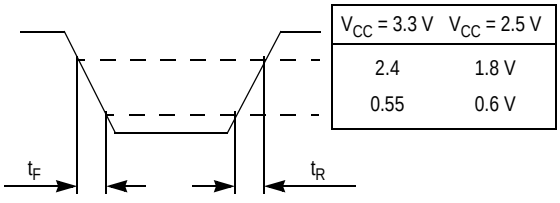


Figure 18. Output Transition Time Test Reference

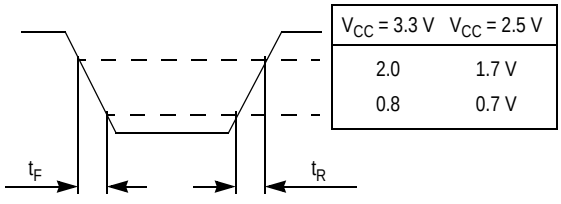
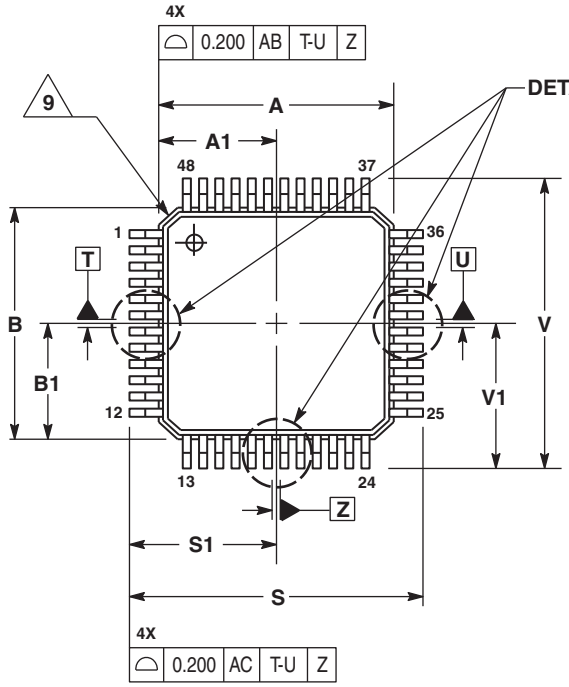
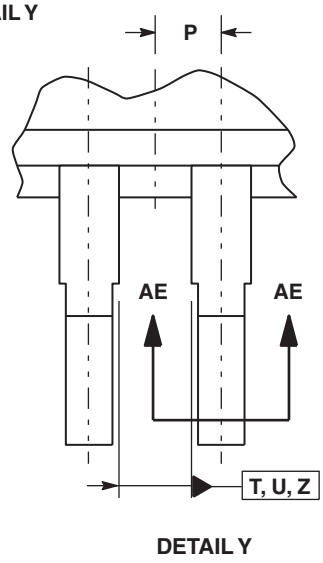


Figure 19. Input Transition Time Test Reference

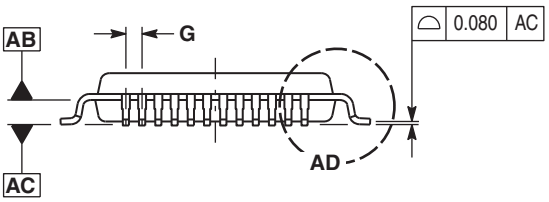
PACKAGE DIMENSIONS

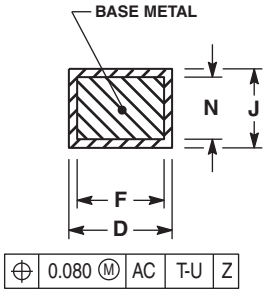




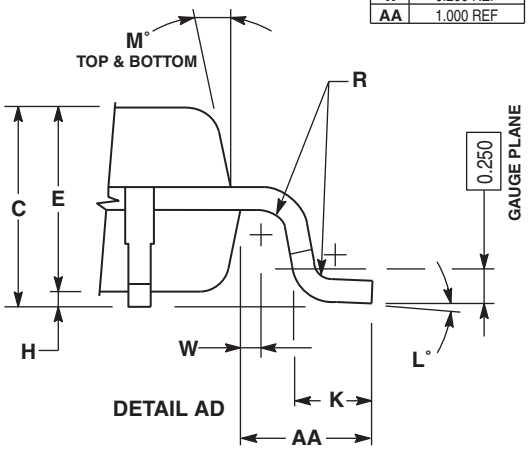
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5m, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLAN AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS T, U, AND Z TO BE DETERMINED AT DATAUM PLANE AB.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE AC.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

	MILLIMETERS	
DIM	MIN	MAX
A	7.000 BSC	
A1	3.500 BSC	
B	7.000 BSC	
B1	3.500 BSC	
C	1.400	1.600
D	0.170	0.270
E	1.350	1.450
F	0.170	0.230
G	0.500 BSC	
H	0.050	0.150
J	0.090	0.200
K	0.500	0.700
L	0°	7°
M	12° REF	
N	0.090	0.160
P	0.250 BSC	
R	0.150	0.250
S	9.000 BSC	
S1	4.500 BSC	
V	9.000 BSC	
V1	4.500 BSC	
W	0.200 REF	
AA	1.000 REF	





SECTION AE-AE



CASE 932-03
ISSUE F
48-LEAD LQFP PACKAGE

Revision History Sheet

Rev	Table	Page	Description of Change	Date
9		1	NRND – Not Recommend for New Designs	1/7/13
10		1	Removed NRND and updated the format of the data sheet	3/18/15

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