

## Description

The XU devices are low phase noise quartz-based PLL oscillators supporting a large range of frequencies and output interface types. These devices are designed to operate at three different power supplies and are available in multiple package sizes as well as temperature grades.

With a patented one-time program (OTP) allowing for infinite memory shelf life, the XU devices can be programmed to generate an output frequency from 16kHz to 1500MHz with a resolution as low as 1Hz accuracy. The configuration capability of this family of devices allows for fast delivery times for both sample and large production orders.

## Features

- Frequency range: 0.016MHz to 1500MHz<sup>[1]</sup>
- Output types: LVDS, LVPECL, HCSL, LVCMOS
- Supply voltage options: 1.8V, 2.5V, or 3.3V
- Phase jitter (1.875MHz to 20MHz): 100fs typical
- Phase jitter (12kHz to 20MHz): 300fs typical
- Package options:
  - 5.0 × 3.2 × 1.2 mm
  - 7.0 × 5.0 × 1.3 mm
- Operating temperature: -20°C to +70°C
  - Frequency stability options: ±20, ±25, ±50, or ±100 ppm
- Operating temperature: -40°C to +85°C
  - Frequency stability options: ±25, ±50, or ±100 ppm
- Operating temperature: -40°C to +105°C
  - Frequency stability options: ±50 or ±100 ppm

[1] There is a dead zone between 1037.5MHz to 1300MHz. Contact [www.idt.com/support](http://www.idt.com/support) for frequencies above 1300MHz.

## Pin Assignments

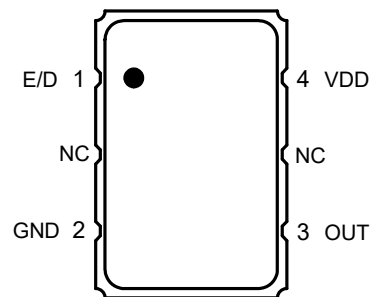
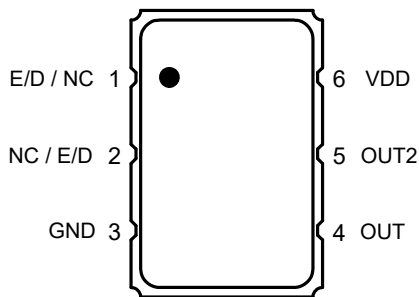


Table 1. 6-pin Package

Pin #	Pin Name	Description
1	E/D NC	Enable/Disable <sup>[a,b]</sup> No connect
2	NC E/D	No connect Enable/Disable <sup>[a,b]</sup>
3	GND	Connect to ground
4	OUT	Output
5	OUT2	Complementary output
6	V <sub>DD</sub>	Supply voltage

Table 2. 4-pin Package

Pin #	Pin Name	Description
1	E/D	Enable/Disable <sup>[a,b]</sup>
2	GND	Connect to ground
3	OUT	Output
4	V <sub>DD</sub>	Supply voltage

[a] Pulled high internally = output enabled.

[b] Low = output disabled.

See [Ordering Information](#) for more details.

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the device. The ratings, which are standard values for Renesas commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Table 3. Absolute Maximum Ratings

Item	Rating			
V <sub>DD</sub>	-0.5 to +5.0V			
E/D	-0.5V to V <sub>DD</sub> + 0.5V			
OUT	-0.5V to V <sub>DD</sub> + 0.5V			
Storage Temperature	-55°C to 125°C			
Maximum Junction Temperature	125°C			
Core Current	65mA maximum			
Theta J <sub>A</sub>	JU6	75.9 °C/W	JS6	89.6 °C/W
Theta J <sub>B</sub>		48.6°C/W		54.3 °C/W

## ESD Compliance

Table 4. ESD Compliance

Human Body Model (HBM)	1000V
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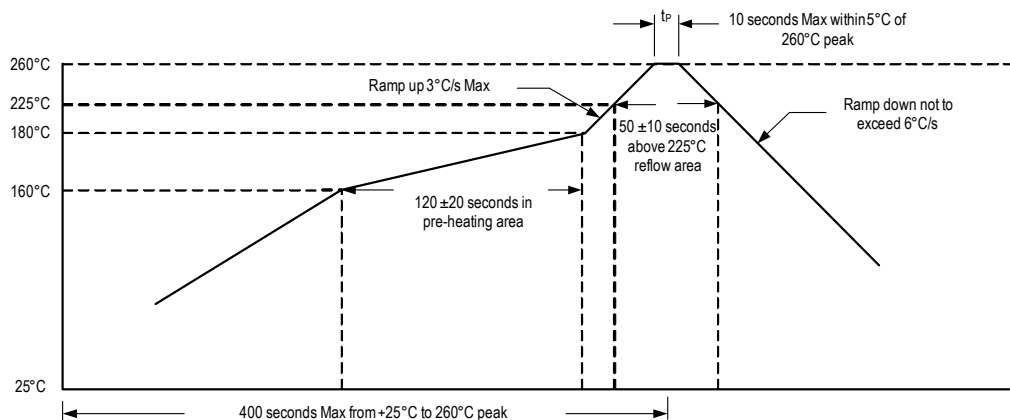
## Mechanical Testing

Table 5. Mechanical Testing \*

Parameter	Test Method
Mechanical Shock	Half-sine wave with 0.3ms 3000G. X, Y, Z each direction 1 time.
Mechanical Vibration	Frequency: 10 to 55MHz amplitude: 1.5mm. Frequency: 55–2000Hz peak value: 20G. Duration time: 4H for each X,Y,Z axis; total 12hours.
High Temp Operating Life (HTOL)	2000 hours at 125°C (under power).
Hermetic Seal	Gross leak (air leak test). Fine leak (Helium leak test) He-pressure: 6kgf/cm <sup>2</sup> 2 hours.

\* MSL level does not apply.

## Solder Reflow Profile



## DC Electrical Characteristics

Note for all DC Electrical Characteristics tables: A pull-up resistor from  $V_{DD}$  to E/D enables output when pin 1 is left open.

Table 6. 3.3V  $I_{DD}$  DC Electrical Characteristics

$V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -20^\circ C$  to  $+70^\circ C$ ;  $-40^\circ C$  to  $+85^\circ C$ ,  $-40^\circ C$  to  $+105^\circ C$ .

Symbol	Parameter	Output Type	Conditions	Minimum	Typical	Maximum	Units
$I_{DD}$	Current Consumption	LVDS	0.016MHz to 400MHz.			97	mA
			400.000+MHz to 1.5GHz.			122	
		LVPECL	0.016MHz to 212.5MHz.			115	
			212.5+MHz to 400MHz.			128	
			400+MHz to 670MHz.			142	
		HCSL	0.016MHz to 670MHz.			145	
		LVCMOS	0.016MHz to 62.5MHz.			98	
			62.5+MHz to 167MHz.			108	

Table 7. 2.5V  $I_{DD}$  DC Electrical Characteristics

$V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -20^\circ C$  to  $+70^\circ C$ ;  $-40^\circ C$  to  $+85^\circ C$ ,  $-40^\circ C$  to  $+105^\circ C$ .

Symbol	Parameter	Output Type	Conditions	Minimum	Typical	Maximum	Units
$I_{DD}$	Current Consumption	LVDS	0.016MHz to 400MHz.			90	mA
			400.000+MHz to 1.35GHz.			103	
		LVPECL	0.016MHz to 156.25MHz.			102	
			156.25+MHz to 400MHz.			112	
			400+MHz to 670MHz.			118	
		HCSL	0.016MHz to 400MHz.			102	
			400.000+MHz to 670MHz.			112	
		LVCMOS	0.016MHz to 62.5MHz.			80	
			62.5+MHz to 125MHz.			85	
			125+MHz to 167MHz.			92	

Table 8. 1.8V IDD DC Electrical Characteristics

$V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -20^\circ C$  to  $+70^\circ C$ ;  $-40^\circ C$  to  $+85^\circ C$ ,  $-40^\circ C$  to  $+105^\circ C$ .

Symbol	Parameter	Output Type	Conditions	Minimum	Typical	Maximum	Units
$I_{DD}$	Current Consumption	LVDS	0.016MHz to 400MHz.			65	mA
			400.000+MHz to 1.0GHz.			72	
		LVPECL	0.016MHz to 250MHz.			75	
			250.000+MHz to 670MHz.			97	
		HCSL	0.016MHz to 400MHz.			68	
			400.000+MHz to 670MHz.			77	
LVC MOS	0.016MHz to 125MHz.			58			

Table 9. LVDS DC Electrical Characteristics

$V_{DD} = 3.3V, 2.5V, 1.8V \pm 5\%$ ,  $T_A = -20^\circ C$  to  $+70^\circ C$ ;  $-40^\circ C$  to  $+85^\circ C$ ,  $-40^\circ C$  to  $+105^\circ C$ . Below are guaranteed for listed standard frequencies.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$V_{OD}$	Differential Output Voltage		0.25	0.4	0.5	V
$V_{OS}$	Output Offset Voltage		1	1.17	1.375	
$V_{IH}$	Enable/Disable Input High Voltage		$70\%V_{DD}$			
$V_{IL}$	Enable/Disable Input Low Voltage				$30\%V_{DD}$	

Table 10. LVPECL DC Electrical Characteristics

$V_{DD} = 3.3V, 2.5V, 1.8V \pm 5\%$ ,  $T_A = -20^\circ C$  to  $+70^\circ C$ ;  $-40^\circ C$  to  $+85^\circ C$ ,  $-40^\circ C$  to  $+105^\circ C$ . Below are guaranteed for listed standard frequencies.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage	$V_{DD} = 3.3V \pm 5\%$ .	1.85		2.3	V
		$V_{DD} = 2.5V \pm 5\%$ .	1.1		1.45	
		$V_{DD} = 1.8V \pm 5\%$ .	0.5		0.8	
$V_{OL}$	Output Low Voltage	$V_{DD} = 3.3V \pm 5\%$ .	1.1		1.65	
		$V_{DD} = 2.5V \pm 5\%$ .	0.35		0.85	
		$V_{DD} = 1.8V \pm 5\%$ .	0		0.25	
$V_{IH}$	Enable/Disable Input High Voltage		$70\%V_{DD}$			
$V_{IL}$	Enable/Disable Input Low Voltage				$30\%V_{DD}$	

Table 11. HCSL DC Electrical Characteristics

$V_{DD} = 3.3V, 2.5V, 1.8V \pm 5\%$ ,  $T_A = -20^\circ C$  to  $+70^\circ C$ ;  $-40^\circ C$  to  $+85^\circ C$ ,  $-40^\circ C$  to  $+105^\circ C$ . Below are guaranteed for listed standard frequencies.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage	$V_{DD} = 3.3V \pm 5\%$ .	0.6		1.1	V
		$V_{DD} = 2.5V \pm 5\%$ .	0.55		0.95	
		$V_{DD} = 1.8V \pm 5\%$ .	0.45		0.7	
$V_{OL}$	Output Low Voltage		0		0.2	
$V_{IH}$	Enable/Disable Input High Voltage		$70\%V_{DD}$			
$V_{IL}$	Enable/Disable Input Low Voltage				$30\%V_{DD}$	

Table 12. LVCMOS DC Electrical Characteristics

$V_{DD} = 3.3V, 2.5V, 1.8V \pm 5\%$ ,  $T_A = -20^\circ C$  to  $+70^\circ C$ ;  $-40^\circ C$  to  $+85^\circ C$ ,  $-40^\circ C$  to  $+105^\circ C$ . Below are guaranteed for listed standard frequencies.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Differential Output Voltage		$90\%V_{DD}$			V
$V_{OL}$	Output Offset Voltage				$10\%V_{DD}$	
$V_{IH}$	Enable/Disable Input High Voltage		$70\%V_{DD}$			
$V_{IL}$	Enable/Disable Input Low Voltage				$30\%V_{DD}$	

## AC Electrical Characteristics

Table 13. 3.3V AC Electrical Characteristics

$V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -20^\circ C$  to  $+70^\circ C$ ;  $-40^\circ C$  to  $+85^\circ C$ ,  $-40^\circ C$  to  $+105^\circ C$ .

Symbol	Parameter	Test Condition		Minimum	Typical	Maximum	Units
F	Output Frequency Range	LVDS.		0.016		1500	MHz
		LVPECL, HCSL.		0.016		670	
		LVCMOS.		0.016		167	
	Frequency Stability	Temperature = $-20^\circ C$ to $+70^\circ C$ .		$\pm 20$		$\pm 100$	ppm
		Temperature = $-40^\circ C$ to $+85^\circ C$ .		$\pm 25$		$\pm 100$	ppm
		Temperature = $-40^\circ C$ to $+105^\circ C$ .		$\pm 50$		$\pm 100$	ppm
	Aging (1st year)	$T_A = 25^\circ C$ .				$\pm 3$	
	Aging (10 years)	$T_A = 25^\circ C$ .				$\pm 10$	
	Output Load	LVDS.	Differential.		100		$\Omega$
		LVPECL.	$V_{DD} - 2.0V$ .		50		
		HCSL.	To GND.		50		
		LVCMOS.	To GND.		15		pF
$T_{ST}$	Start-up Time	Output valid time after $V_{DD}$ meets minimum specified level.				10	ms
$t_R$	Output Rise Time	LVDS.	20% to 80% Vpk-pk.		275	380	ps
		LVPECL.				400	
		HCSL.				330	
		LVCMOS.	10% to 90% $V_{DD}$ .			3	ns
$t_F$	Output Fall Time	LVDS.	80% to 20% Vpk-pk.		275	380	ps
		LVPECL.				400	
		HCSL.				330	
		LVCMOS.	90% to 10% $V_{DD}$ .			3	ns
$O_{DC}$	Output Clock Duty Cycle	LVDS.		45		55	%
		LVPECL.	$F_{OUT} \leq 312.5MHz$ .	45		55	
			$F_{OUT} > 312.5MHz$ .	40		60	
		HCSL.		45		55	
		LVCMOS.	$F_{OUT} \leq 62.5MHz$ .	45		55	
			$F_{OUT} > 62.5MHz$ .	40		60	
$T_{OE}$	Output Enable/ Disable Time					100	ns
$f_{JITTER}$	Phase Jitter (12kHz–20MHz)	LVDS.			300	400	fsec
		LVPECL.			300	400	
		HCSL.			300	400	
		LVCMOS.	$F_{OUT} = 100MHz$ .		300	400	

Table 14. 2.5V AC Electrical Characteristics

$V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -20^\circ C$  to  $+70^\circ C$ ;  $-40^\circ C$  to  $+85^\circ C$ ,  $-40^\circ C$  to  $+105^\circ C$ .

Symbol	Parameter	Test Condition		Minimum	Typical	Maximum	Units
F	Output Frequency Range	LVDS.		0.016		1350	MHz
		LVPECL.		0.75		670	
		HCSL.		0.016		670	
		LVCMOS.		0.016		167	
	Frequency Stability	Temperature = $-20^\circ C$ to $+70^\circ C$ .		$\pm 20$		$\pm 100$	ppm
		Temperature = $-40^\circ C$ to $+85^\circ C$ .		$\pm 25$		$\pm 100$	ppm
		Temperature = $-40^\circ C$ to $+105^\circ C$ .		$\pm 50$		$\pm 100$	ppm
	Aging (1st year)	$T_A = 25^\circ C$ .				$\pm 3$	
	Aging (10 years)	$T_A = 25^\circ C$ .				$\pm 10$	
	Output Load	LVDS.	Differential.		100		$\Omega$
		LVPECL.	$V_{DD} - 2.0V$ .		50		
		HCSL.	To GND.		50		
		LVCMOS.	To GND.		15		$\mu F$
$T_{ST}$	Start-up Time	Output valid time after $V_{DD}$ meets minimum specified level.				10	ms
$t_R$	Output Rise Time	LVDS.	20% to 80% Vpk-pk.		300	400	ps
		LVPECL.			250	630	
		HCSL.				315	
		LVCMOS.	10% to 90% $V_{DD}$ .			3	ns
$t_F$	Output Fall Time	LVDS.	80% to 20% Vpk-pk.		300	400	ps
		LVPECL.			360	630	
		HCSL.				315	
		LVCMOS.	90% to 10% $V_{DD}$ .			3	ns
$O_{DC}$	Output Clock Duty Cycle	LVDS.		45		55	%
		LVPECL.	$F_{OUT} \leq 156.25MHz$ .	45		55	
			$F_{OUT} \leq 156.25MHz$ .	40		60	
		HCSL.		45		55	
		LVCMOS.	$F_{OUT} \leq 62.5MHz$ .	45		55	
			$F_{OUT} > 62.5MHz$ .	40		60	
$T_{OE}$	Output Enable/ Disable Time					100	ns
$f_{JITTER}$	Phase Jitter (12kHz–20MHz)	LVDS.			400	500	fsec
		LVPECL.			350	500	
		HCSL.			350	500	
		LVCMOS.	$F_{OUT} = 100MHz$ .		350	500	

Table 15. 1.8V AC Electrical Characteristics

$V_{DD} = 1.8V \pm 5\%$ ,  $T_A = -20^\circ C$  to  $+70^\circ C$ ;  $-40^\circ C$  to  $+85^\circ C$ ,  $-40^\circ C$  to  $+105^\circ C$ .

Symbol	Parameter	Test Condition		Minimum	Typical	Maximum	Units	
F	Output Frequency Range	LVDS.		0.016		1000	MHz	
		LVPECL, HCSL.		0.016		670		
		LVCMOS.		0.016		125		
	Frequency Stability	Temperature = $-20^\circ C$ to $+70^\circ C$ .		$\pm 20$		$\pm 100$	ppm	
		Temperature = $-40^\circ C$ to $+85^\circ C$ .		$\pm 25$		$\pm 100$	ppm	
		Temperature = $-40^\circ C$ to $+105^\circ C$ .		$\pm 50$		$\pm 100$	ppm	
	Aging (1st year)	$T_A = 25^\circ C$ .				$\pm 3$		
	Aging (10 years)	$T_A = 25^\circ C$ .				$\pm 10$		
	Output Load	LVDS.	Differential.		100		$\Omega$	
		LVPECL, HCSL.	To GND.		50			
		LVCMOS.	To GND.		10		pF	
$T_{ST}$	Start-up Time	Output valid time after $V_{DD}$ meets minimum specified level.				10	ms	
$t_R$	Output Rise Time	LVDS.	20% to 80% Vpk-pk.		250	315	ps	
		LVPECL.			250	350		
		HCSL.				320		
		LVCMOS.	10% to 90% $V_{DD}$ .		5		ns	
$t_F$	Output Fall Time	LVDS.	80% to 20% Vpk-pk.		250	315	ps	
		LVPECL.			250	350		
		HCSL.				320		
		LVCMOS.	90% to 10% $V_{DD}$ .		5		ns	
$O_{DC}$	Output Clock Duty Cycle	LVDS.	$F_{OUT} \leq 156.25MHz$ .	45		55	%	
			$F_{OUT} \leq 156.25MHz$ .	40		60		
		LVPECL.	$F_{OUT} \leq 312.5MHz$ .	45		55		
			$F_{OUT} > 312.5MHz$ .	40		60		
		HCSL.			40			60
		LVCMOS.	$F_{OUT} \leq 62.5MHz$ .	45		55		
$F_{OUT} > 62.5MHz$ .	40			60				
$T_{OE}$	Output Enable/ Disable Time					100	ns	
$f_{JITTER}$	Phase Jitter (12kHz–20MHz)	LVDS.			800	1200	fsec	
		LVPECL.			750	1200		
		HCSL.			100	1200		
		LVCMOS.	$F_{OUT} = 100MHz$ .		800	1200		



Notes for all AC Electrical Characteristics tables:

- <sup>1</sup> A pull-up resistor from  $V_{DD}$  to E/D enables output when pin 1 is left open.
- <sup>2</sup> Installation should include a 0.01 $\mu$ F bypass capacitor placed between VDD and GND to minimize power supply line noise.
- <sup>3</sup> Stability is inclusive of 25°C tolerance, operating temperature range, input voltage change, load change, aging, shock and vibration.
- <sup>4</sup> Standard LVCMOS frequencies include 10MHz, 12MHz, 12.288MHz, 16MHz, 20MHz, 24MHz, 24.576MHz, 25MHz, 33.333MHz, 40MHz, 48MHz, 50MHz, 100MHz, 125MHz and 156.25MHz.
- <sup>5</sup> Standard differential frequencies include 100MHz, 106.25MHz, 125MHz, 150MHz, 155.52MHz, 156.25MHz, 200MHz, 212.5MHz, 250MHz, 300MHz, 312.5MHz and 400MHz.

## I2C Bus Characteristics

Table 16. I2C Bus DC Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Level		$0.7 \times V_{DD33}$			V
$V_{IL}$	Input Low Level				$0.3 \times V_{DD33}$	V

Table 17. I2C Bus AC Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$F_{SCLK}$	Serial Clock Frequency (SCL)			100	400	kHz
$t_{BUF}$	Bus Free Time between STOP and START		1.3			$\mu$ s
$t_{SU:START}$	Setup Time, START		0.6			$\mu$ s
$t_{HD:START}$	Hold Time, START		0.6			$\mu$ s
$t_{SU:DATA}$	Setup Time, Data Input (SDA)		100			$\mu$ s
$t_{HD:DATA}$	Hold Time, Data Input (SDA) <sup>1</sup>		0			$\mu$ s
$t_R$	Rise Time, Data and Clock (SDA, SCL)				300	ns
$t_F$	Fall Time, Data and Clock (SDA, SCL)				300	ns
$t_{HIGH}$	High Time, Clock (SCL)		0.6			$\mu$ s
$t_{LOW}$	Low Time, Clock (SCL)		1.3			$\mu$ s
$t_{SU:STOP}$	Setup Time, STOP		0.6			$\mu$ s

<sup>1</sup> A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the  $V_{IH(MIN)}$  of the SCL signal) to bridge the undefined region of the falling edge of SCL.

# Output Waveforms

Figure 1. LVDS Output Waveforms

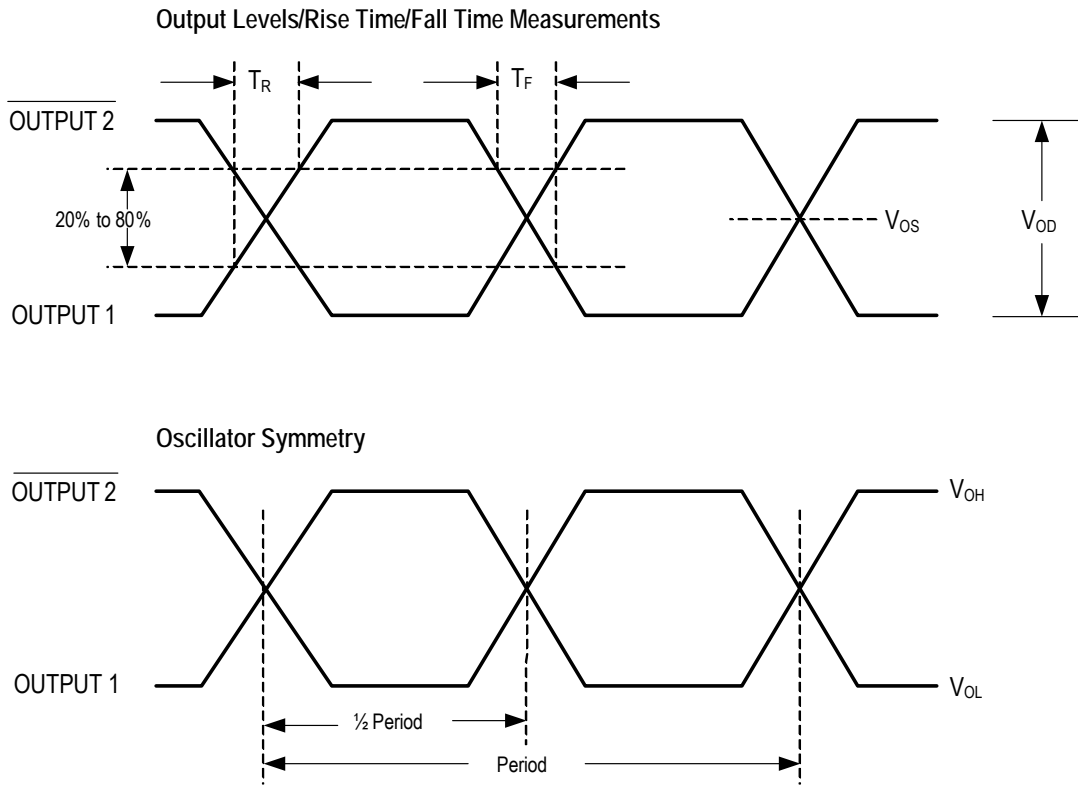


Figure 2. LVPECL Output Waveforms

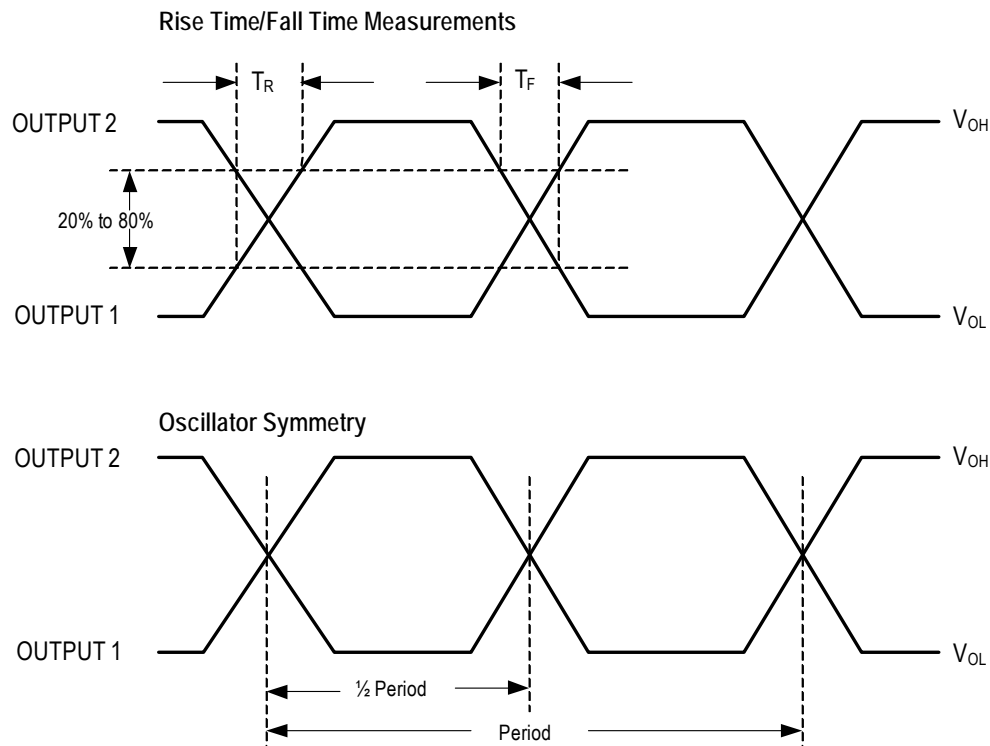


Figure 3. HCSL Output Waveforms

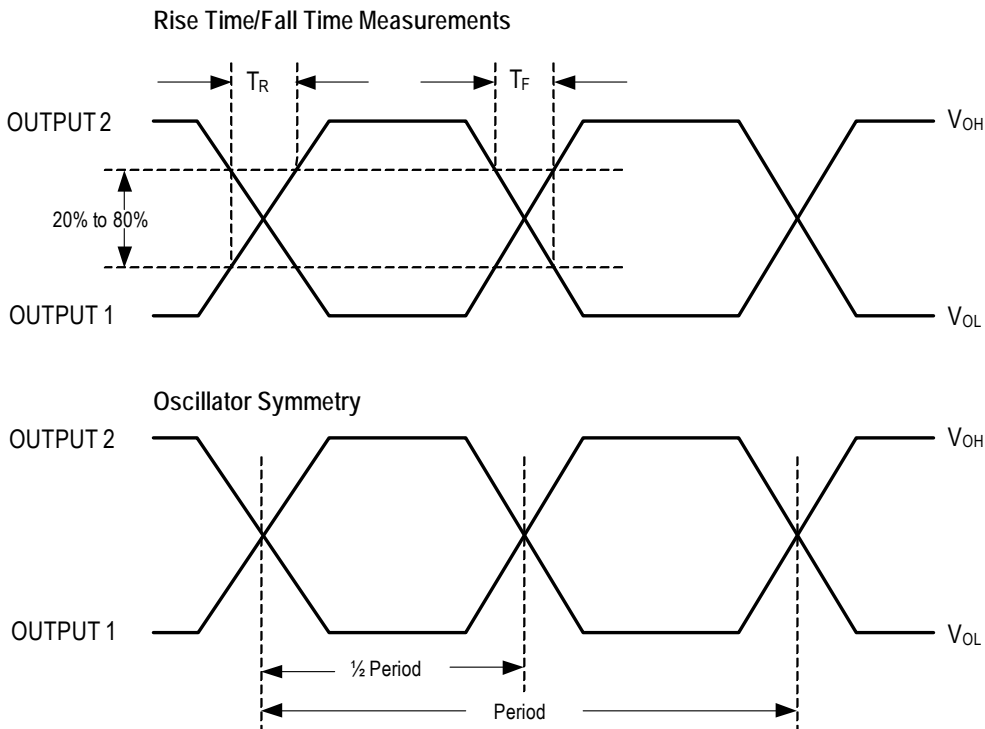
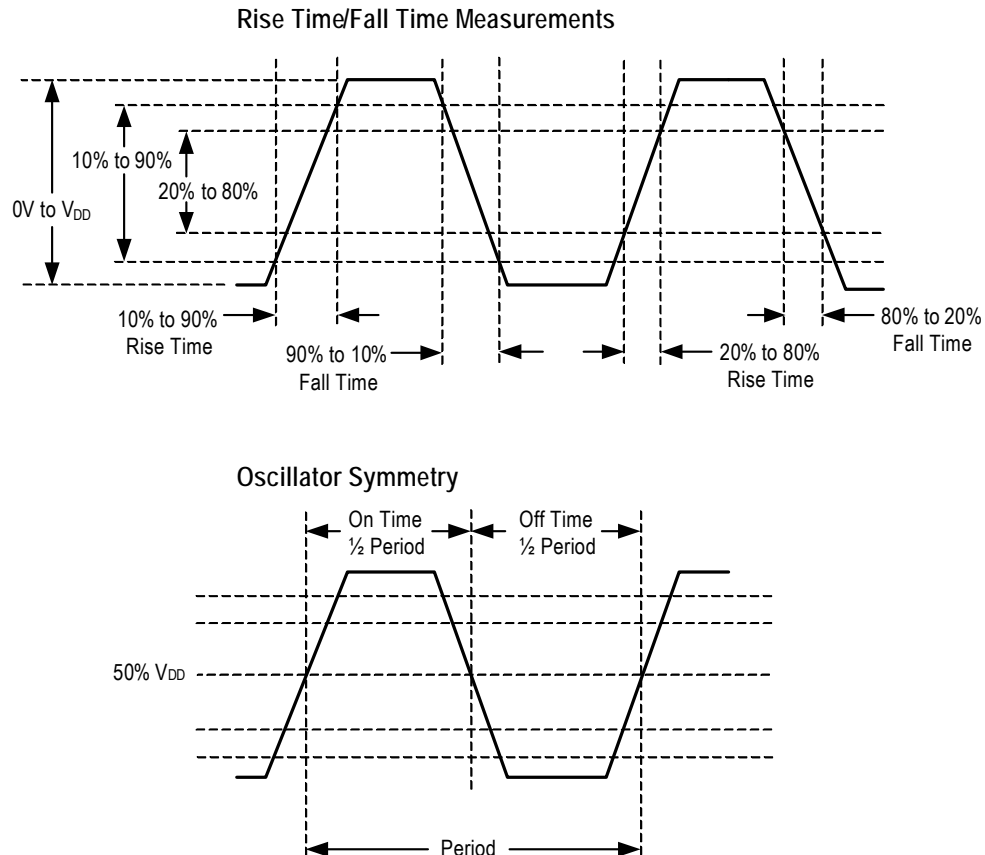


Figure 4. LVCMOS Output Waveforms



## Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the links below. The package information is the most current data available.

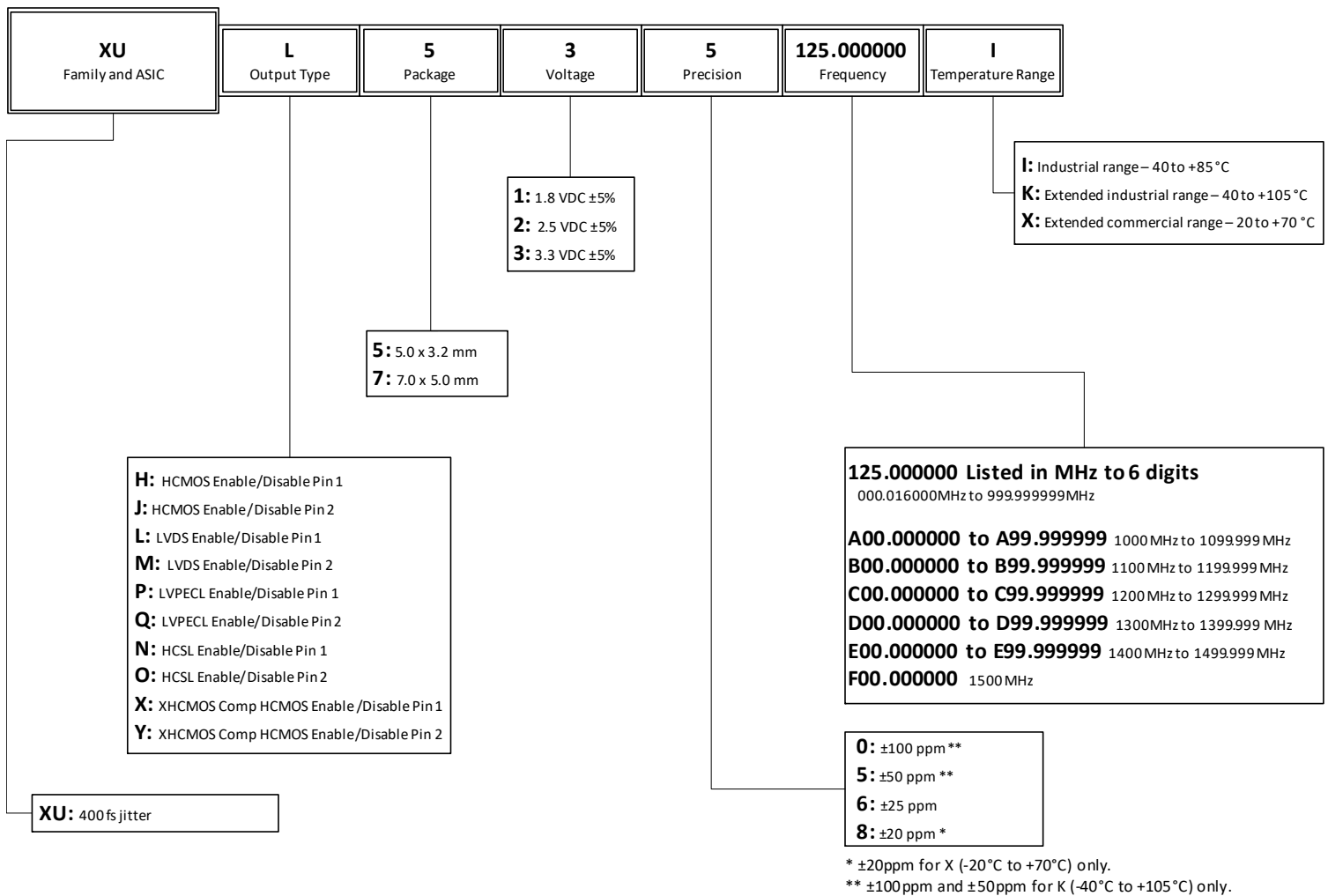
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[www.idt.com/document/psc/ju6-package-outline-70-x-50-mm-body-13-mm-thick](http://www.idt.com/document/psc/ju6-package-outline-70-x-50-mm-body-13-mm-thick)

[www.idt.com/document/psc/js4-package-outline-50-x-32-mm-body-11-mm-thick](http://www.idt.com/document/psc/js4-package-outline-50-x-32-mm-body-11-mm-thick)

[www.idt.com/document/psc/ju4-package-outline-70-x-50-mm-body-13-mm-thick](http://www.idt.com/document/psc/ju4-package-outline-70-x-50-mm-body-13-mm-thick)

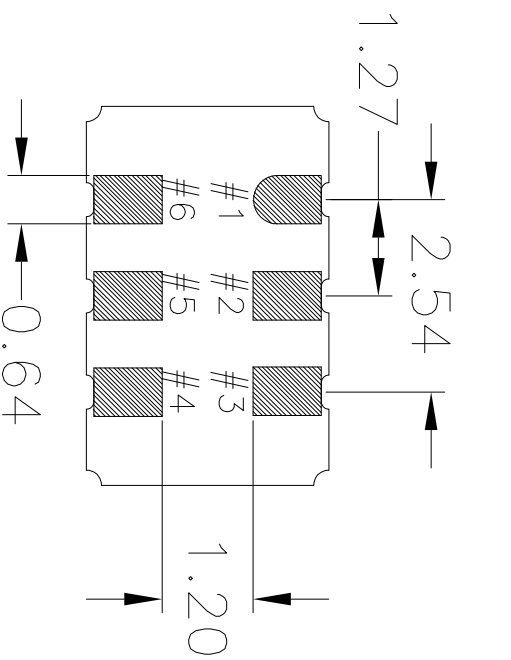
## Ordering Information



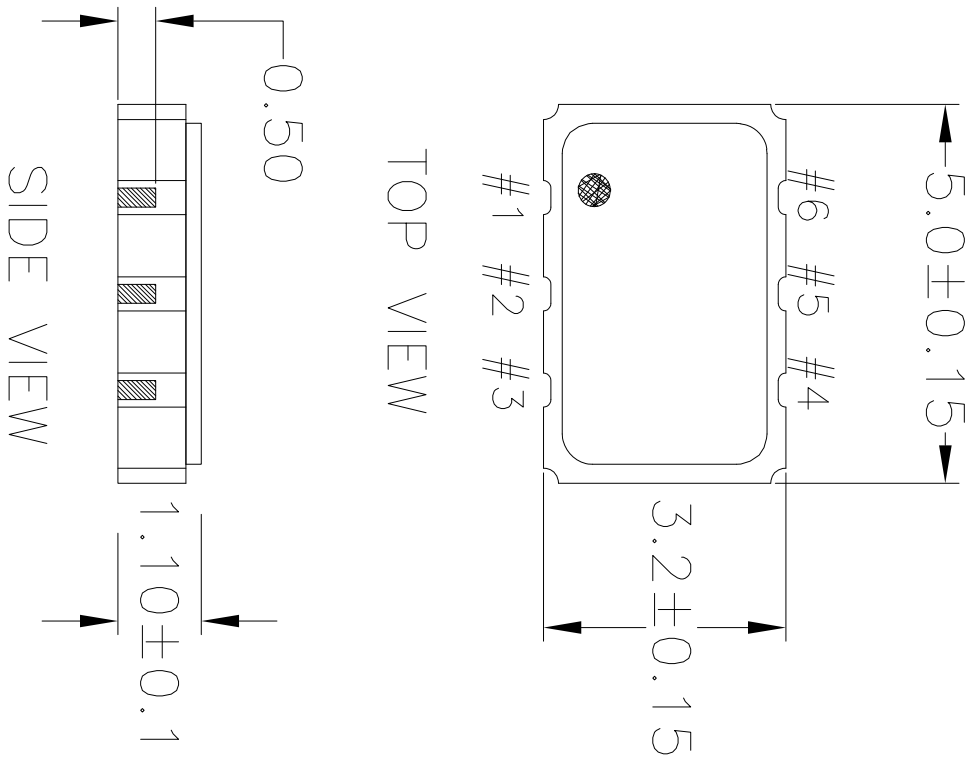
## Revision History

Revision Date	Description of Change
February 11, 2020	Added I2C Bus Characteristics tables.
June 28, 2019	<ul style="list-style-type: none"> <li>▪ Added footnote to frequency range bullet under front page Features.</li> </ul>
June 25, 2018	<ul style="list-style-type: none"> <li>▪ Updated Package Outline Drawings section.</li> </ul>
November 22, 2017	<ul style="list-style-type: none"> <li>▪ Updated Theta JA and JB in Absolute Maximum Ratings table.</li> <li>▪ Added MSL statement under Mechanical Testing table.</li> <li>▪ Updated ordering information.</li> </ul>
October 19, 2017	<ul style="list-style-type: none"> <li>▪ Updated document title.</li> <li>▪ Updated Features bullets.</li> <li>▪ Updated Absolute Maximum Ratings and ESD Compliance tables.</li> <li>▪ Added -40°C to +105°C rating to all electrical tables.</li> <li>▪ Removed phase noise charts.</li> <li>▪ Updated Ordering Information table.</li> </ul>
May 12, 2017	<ul style="list-style-type: none"> <li>▪ Reformatted embedded tables.</li> <li>▪ Removed “Jitter Performance” tables and moved the “Phase Jitter (12kHz–20MHz)” parameter to its respective AC Electrical Characteristics table.</li> <li>▪ Updated all Output Waveform drawings.</li> </ul>
December 1, 2016	Initial release.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	04/2/12	DP
01	ADDED LID IN TOP VIEW	07/12/12	KS
02	UPDATED LID TOLERANCES	12/03/12	KS
03	UPDATE PACKAGE DRAWING	8/8/14	JHUA



BOTTOM VIEW



TOP VIEW

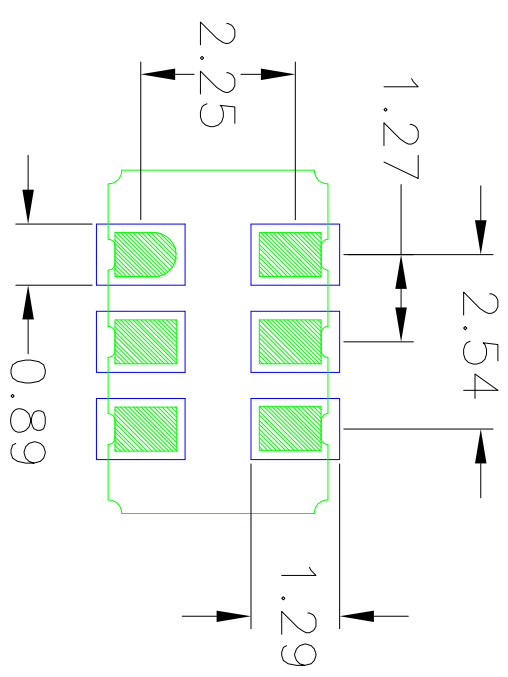
SIDE VIEW

NOTES:  
1. ALL DIMENSIONS IN MM.

TOLERANCES UNLESS SPECIFIED		6024 Silver Creek Valley Rd	
DECIMAL	ANGULAR	Son Jose, CA 95138	
XXX±	±	PHONE: (408) 727-6116	
XXXX±		FAX: (408) 492-8874	
XXXX±			
APPROVALS	DATE	TITLE	SIZE
DRAWN <i>QAC</i>	04/2/12	JS6 PACKAGE OUTLINE	DRAWING No.
CHECKED		5.0 x 3.2 mm BODY	PSC-4411
		1.1 mm Thick	
			REV
			03
DO NOT SCALE DRAWING			SHEET 1 OF 2



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	04/2/12	DP
01	ADDED LID IN TOP VIEW	07/12/12	KS
02	UPDATED LID TOLERANCES	12/03/12	KS
03	UPDATE PACKAGE DRAWING	8/8/14	JHUUA

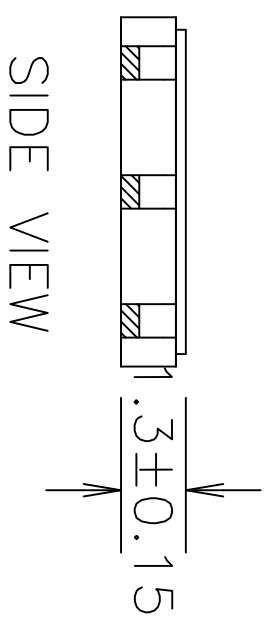
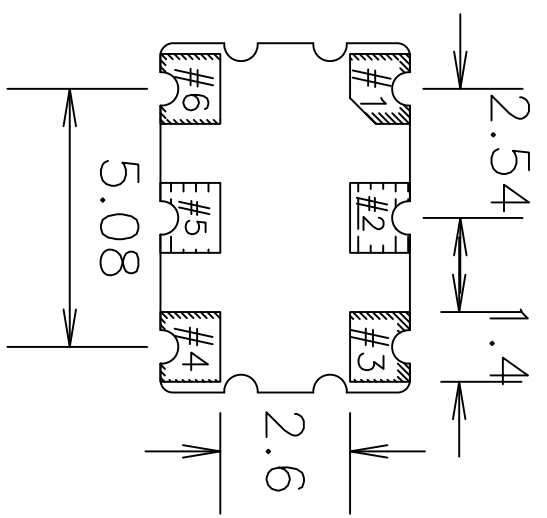
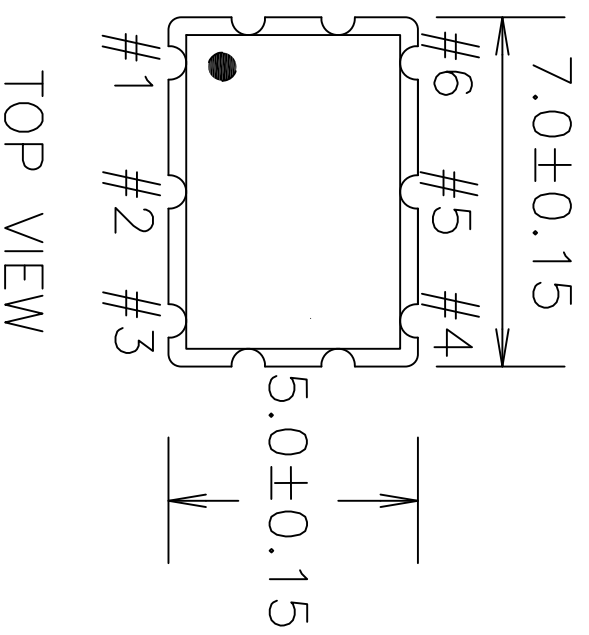


RECOMMENDED LAND PATTERN


- NOTES:
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
  2. TOP DOWN VIEW. AS VIEWED ON PCB.
  3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
  4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
  5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED		6024 Silver Creek Valley Rd	
DECIMAL	ANGULAR	San Jose, CA 95138	
XXX±	±	PHONE: (408) 727-6176	
XXXX±		FAX: (408) 492-8674	
APPROVALS		www.IDT.com	
DRAWN	DATE	TITLE	
04/2/12		J56 PACKAGE OUTLINE	
CHECKED		5.0 x 3.2 mm BODY	
		1.1 mm Thick	
SIZE	DRAWING No.	REV	
C	PSC-4411	03	
DO NOT SCALE DRAWING			SHEET 2 OF 2

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	10/5/12	KS
01	UPDATE PACKAGE DRWING	8/12/14	JHUA

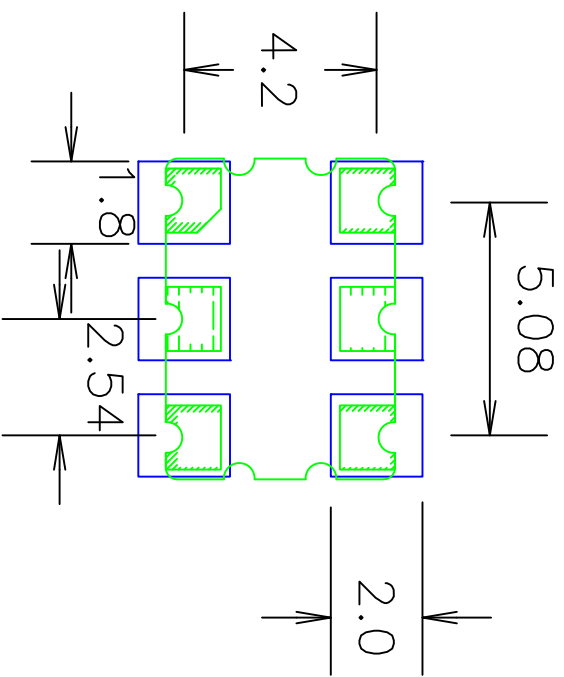


NOTES:  
1. ALL DIMENSIONS IN MM.

TOLERANCES UNLESS SPECIFIED		www.IDT.com	
DECIMAL	ANGULAR	 <b>IDT</b> <sup>TM</sup> 6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-6116 FAX: (408) 482-9874	
XXX±	±		
XXXX±		DATE	
APPROVALS		10/03/12	
DRAWN XJS		TITLE	
CHECKED		JUG PACKAGE OUTLINE	
		SIZE	7.0 x 5.0 mm BODY
		DRAWING No.	1.3 mm Thick
		PSC-4430	
		REV	01
DO NOT SCALE DRAWING			SHEET 1 OF 2




REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	10/5/12	KS
01	UPDATE PACKAGE DRAWING	8/12/14	JLHUA

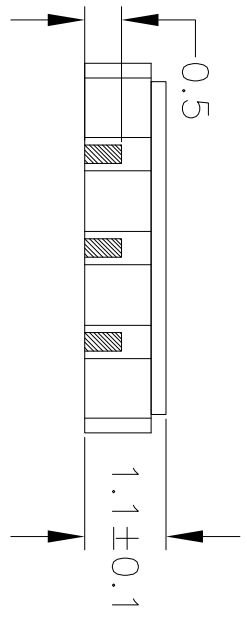
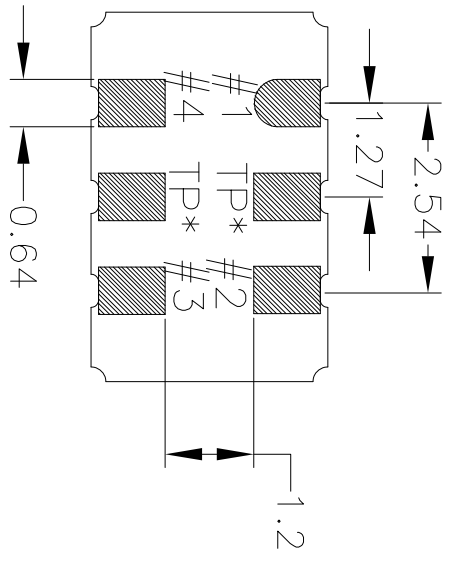
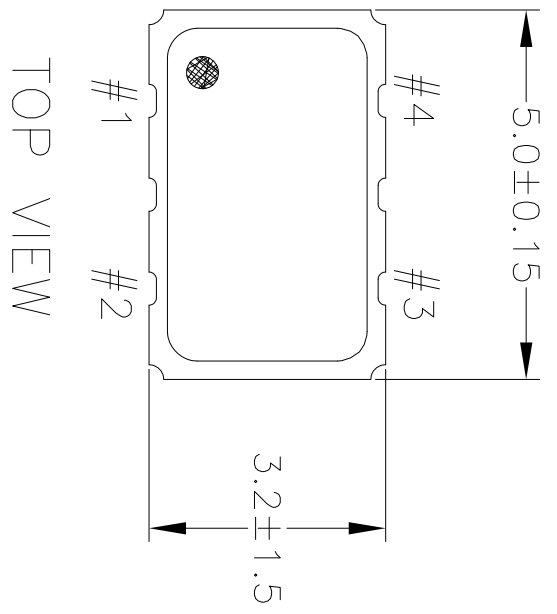


RECOMMENDED LAND PATTERN

- NOTES:
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
  2. TOP DOWN VIEW. AS VIEWED ON PCB.
  3. COMPONENT OUTLINE SHOW FOR REFERENCE IN PCB.
  4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
  5. LAND PATTERN RECOMMENDATION PER IPC-7351B. GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED		 <b>IDT</b> 6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 757-6116 FAX: (408) 492-8874 <a href="http://www.idt.com">www.idt.com</a>	
DECIMAL	ANGULAR		
X.XX	±		
X.XXX			
APPROVALS	DATE	TITLE	
DRAWN <b>KS</b>	10/05/12	J06 PACKAGE OUTLINE	
CHECKED		7.0 x 5.0 mm BODY	
		1.3 mm Thick	
SIZE	DRAWING No.	REV	
<b>C</b>	FSC-4430	<b>01</b>	
DO NOT SCALE DRAWING			SHEET 2 OF 2

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	08/21/12	K. Stahn
01	UPDATED IJD TOLERANCES	12/03/12	K. Stahn
02	UPDATE PACKAGE DRAWING	8/8/14	JHUA



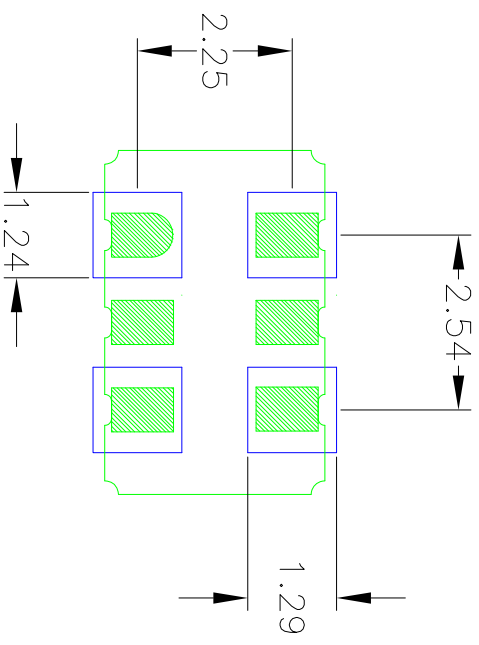
SIDE VIEW

BOTTOM VIEW

NOTES:  
1. ALL DIMENSIONS IN MM.


TOLERANCES UNLESS SPECIFIED		6024 Silver Creek Valley Rd	
DECIMAL	ANGULAR	San Jose, CA 95138	
±	F	PHONE: (408) 727-8116	
XXX	XXXX	FAX: (408) 492-8574	
WWW.IDT.COM		IDT™	
APPROVALS		TITLE JS4 PACKAGE OUTLINE	
DATE	07/18/12	5.0 x 3.2 mm BODY	
DRAWN BY		1.1 mm Thick	
CHECKED		SIZE C	
DRAWING No. PSC-4429		REV 02	
DO NOT SCALE DRAWING		SHEET 1 OF 2	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	08/21/12	K. Stahn
01	UPDATED LID TOLERANCES	12/03/12	K. Stahn
02	UPDATE PACKAGE DRAWING	8/8/14	JHUA

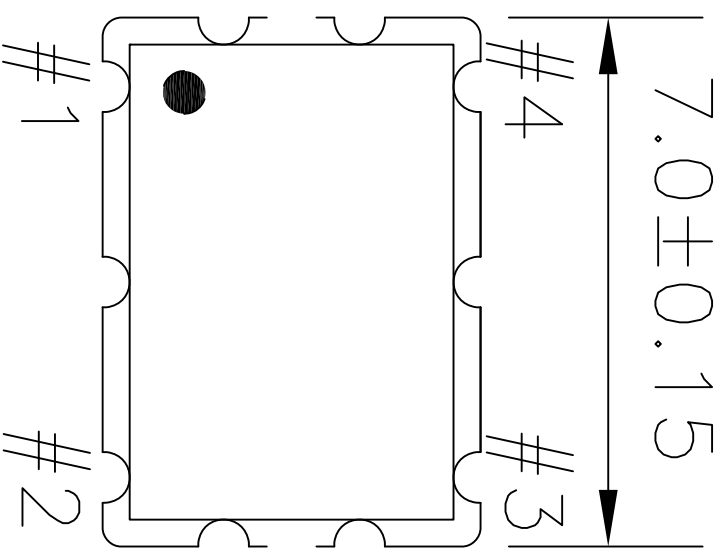


RECOMMENDED LAND PATTERN

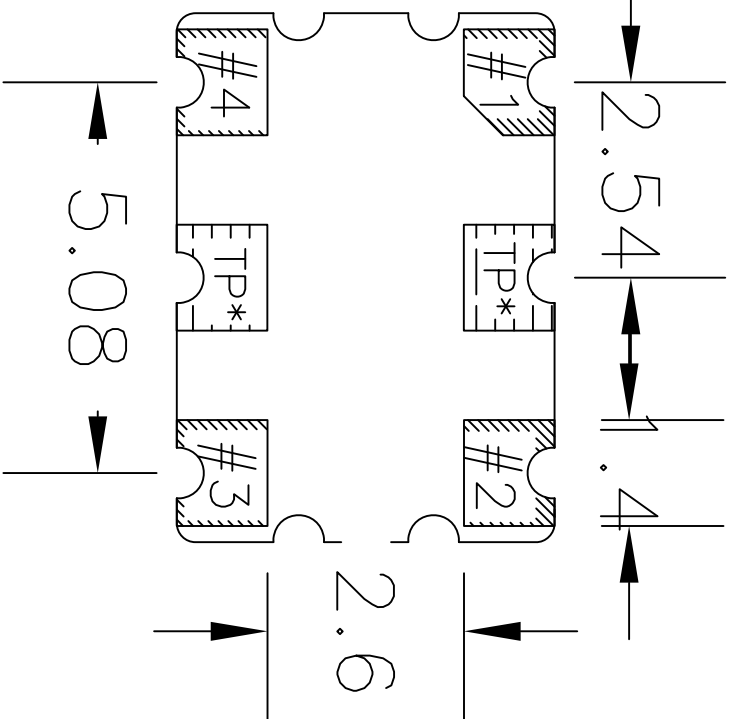
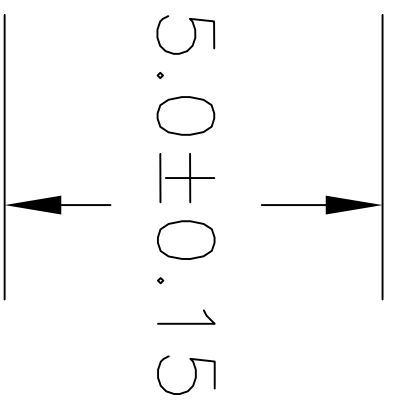
- NOTES:
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
  2. TOP DOWN VIEW. AS VIEWED ON PCB.
  3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
  4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
  5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED		 <b>IDT™</b> 6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-6118 FAX: (408) 492-8674 <a href="http://www.idt.com">www.idt.com</a>	
DECIMAL	±	ANGULAR	
DATE	07/16/12	TITLE	JS4 PACKAGE OUTLINE
DRAWN BY	XXXXX	SIZE	5.0 x 3.2 mm BODY
CHECKED		DRAWING No	1.1 mm Thick
		FSC-4429	
		REV	02
DO NOT SCALE DRAWING			SHEET 2 OF 2

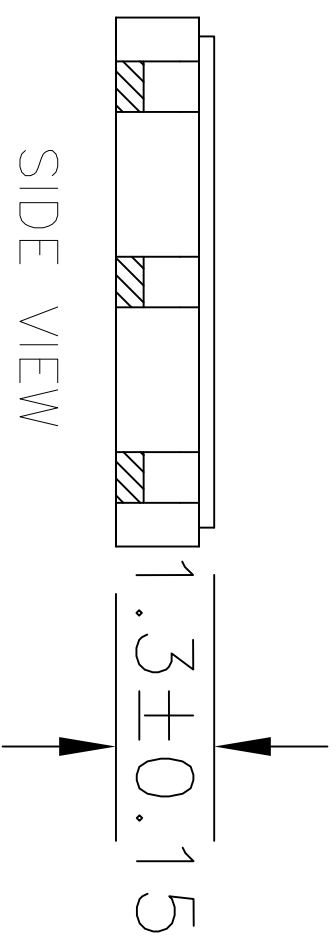
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	10/09/12	KS
01	UPDATE PACKAGE DRAWING	8/11/14	JHUA



TOP VIEW



BOTTOM VIEW

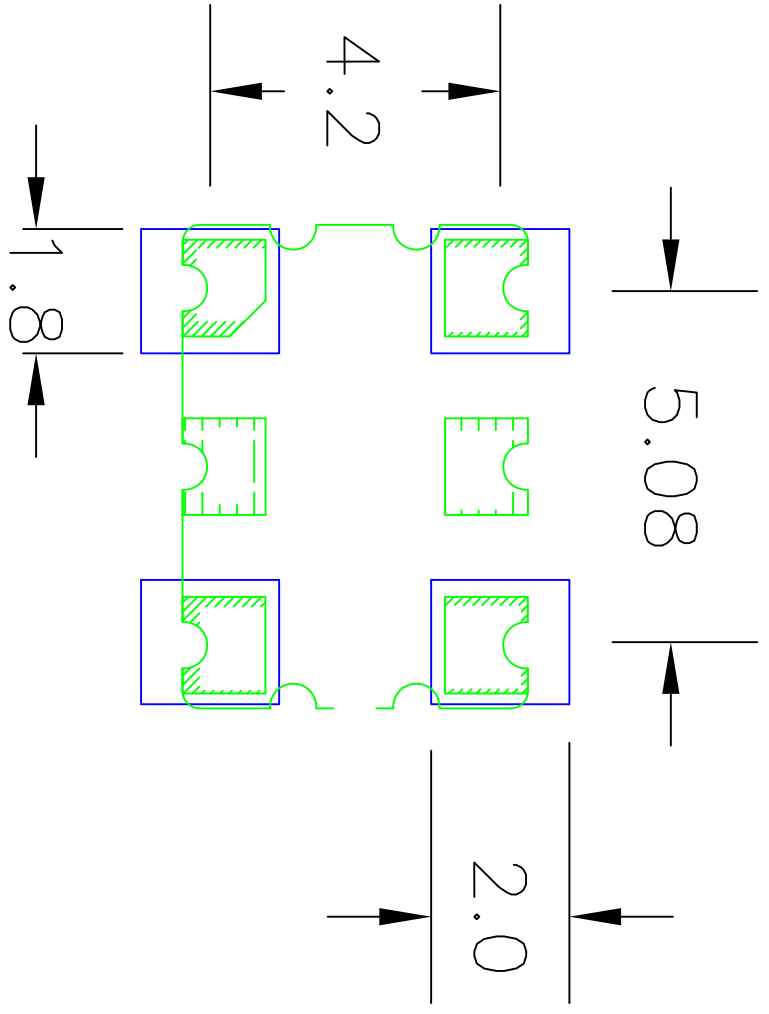


SIDE VIEW

NOTES:  
1. ALL DIMENSIONS IN MM.

TOLERANCES UNLESS SPECIFIED		6024 Silver Creek Valley Rd San Jose, CA 95138	
DECIMAL	±	PHONE: (408) 727-6116	
ANGULAR	±	FAX: (408) 492-8674	
XXX			
XXXX			
XXXXX			
APPROVALS	DATE	TITLE	7024 Silver Creek Valley Rd
DRAWN JCS	10/09/12	JU4 PACKAGE OUTLINE	San Jose, CA 95138
CHECKED		7.0 x 5.0 mm BODY	PHONE: (408) 727-6116
		1.3 mm Thick	FAX: (408) 492-8674
SIZE	DRAWING NO.	REV	
C	PSC-4431	01	
DO NOT SCALE DRAWING			SHEET 1 OF 2

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	10/09/12	KS
01	UPDATE PACKAGE DRAWING	8/11/14	JHUA



RECOMMENDED LAND PATTERN

- NOTES:
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
  2. TOP DOWN VIEW. AS VIEWED ON PCB.
  3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
  4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
  5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED		6024 Silver Creek Valley Rd	
DECIMAL	ANGULAR	San Jose, CA 95128	
XXX±	±	PHONE: (408) 727-6116	
XXXX±		FAX: (408) 492-8674	
XXXX±		www.IDT.com	
APPROVALS	DATE	TITLE	JU4 PACKAGE OUTLINE
DRAWN %28	10/05/12	7.0 x 5.0 mm BODY	
CHECKED		1.3 mm Thick	
		SIZE DRAWING No.	REV
		C PSC-4431	01
DO NOT SCALE DRAWING			SHEET 2 OF 2

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(Rev.1.0 Mar 2020)

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Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

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