# RC32438 Document Errata

## Notes

## Supplemental Information

This document errata reflects changes to the "RC32438 Integrated Communications Processor User Reference Manual" dated March 7, 2003.

### Revision History

**March 21, 2003**: Initial publication, with item #1.

**March 28, 2003**: Added items #2 and #3.

**April 8, 2003**: Added item #4.

**April 11, 2003**: Added items #5 and #6.

**May 28, 2003**: Added items #7 through #9.

**July 28, 2003**: Added item #10.

**October 6, 2003**: Added item #11.

**November 21, 2003**: Added item #12.

## Errata Items

#### Item #1 - PCI Serial EEPROM Interface

**Issue:** In Chapter 10, PCI Bus Interface, section PCI Serial EEPROM Interface, first paragraph, the last sentence should read as follows: "Only EEPROMs which are 2048 bits or greater in size should be used."

#### Item #2 - PCI Serial EEPROM Interface

**Issue:** In Chapter 10, PCI Bus Interface, section PCI Serial EEPROM Interface, first paragraph: changed configuration register address from 0x80 to 0x40 and added the following sentence, "The interface only supports 93C46-compatible serial EEPROMs." In the second paragraph, the following sentence was deleted, "EEPROM addresses which are greater than or equal to 0x40 in EEPROMs whose size is greater than 1024 bits may be used to store application specific information."

#### Item #3 - PCI Disabled Mode

**Issue:** In Chapter 10, PCI Bus Interface, section Disabled Mode, the first sentence of the second paragraph should read as follows: "When the PCI bus interface is disabled, all of the PCI pins are tri-stated, except PCIGNTN[3:1], and thus should be held at a valid logic level on the board." Also added that PCIGNTN[3:1] signals are driven high.

#### Item #4 - TLB Behavior

**Issue:** In Chapter 2, Index Register (CP0 Register 0, Select 0) section on page 2-56, the first paragraph should read as follows: "The Index register is a 32-bit read/write register that contains the index used to access the TLB for TLBP, TLBR, and TLBWI instructions. The width of the index field is 4-bits wide in order to address the 16 entries in the TLB. The operation of the processor is UNDEFINED if a value greater than or equal to the number of TLB entries is written to the Index register. This register is only valid with the TLB."

Also in Chapter 2, TLB section on page 2-80, first sentence should read as follows: "Because of the hidden bit indicating initialization, the 4Kc processor core does not require TLB initialization upon Cold-Reset. This is a feature of the 4Kc core."

**Item #5 - Register Address for DDR Read Data Capture Register**

**Issue:** The address for the DDRRDC register, 0x01_8024, was added to Table 7.1 in Chapter 7 and to Table 1.4 in Chapter 1.

**Item #6 - DDR Program Example**

**Issue:** Revised the DDR Program Example at the end of Chapter 7.

**Item #7 - RC32438 or SDRAM Mapping**

**Issue:** Added the following footnote to page 1-20 in Chapter 1 and to page 4-4 in Chapter 4:

"If a device or SDRAM is mapped such that it overlaps the internal system address space (0x1800_000 through 0x181F_FFFF), the internal system controller address space will take precedence. Any subsequent CPU or PCI access to this redundantly mapped space will result in the system controller being accessed."

**Item #8 - PCIREQN[3:0] Signals**

**Issue:** In Chapter 1, Table 1.2, the description for PCIREQN[3:0] signals refers to unused signals being driven low. In fact, the signals are driven high.

**Item #9 - Ethernet Station Addresses**

**Issue:** In Chapter 11, Address Recognition Logic section, the 4th and 5th paragraphs were changed to read as follows:

The Ethernet interface contains four station address registers. A station address is a 48-bit MAC address stored in a station address low and high register pair. There are four station address register pairs:

ETHSAL[0|1|2|3]

ETHSAH[0|1|2|3]

> **Note:** To ensure proper operation, all four Ethernet station address registers MUST be programmed with the same value.

The MAC address used for control frames is contained in the ETHCFSA[0|1|2] registers.

**Item #10 - Multiple Changes**

**Issue:** Removed references to IPBus Monitor feature. In Chapter 5, deleted Enable Eager Prefetching bit from IPBus Arbiter Control Register in the IPBus Registers section. In Chapter 10, revised description for EN bit in PCI Control Register, Changed Byte Swapping bit in PCI Local Address Control register to Force Endianess, added "byte and halfword target IO transactions are not supported" to Target I/O Read and Target I/O Write sections, and changed DMA limitations to "32KB minus 8 bytes" for channels 8 and 9. In Chapter 11, removed table associated with MII Management Command Register, changed the First Descriptor bit in Figure 11.10 to Reserved, and deleted information about FD in 2 sections: Ethernet Input DMA Operations and Ethernet Output DMA Operations. In Chapter 16, added information in the Functional Overview section. In Chapter 17, revised first 4 paragraphs of Theory of Operation section.

**Item #11 - PCI Serial EEPROM Done bit**

**Issue:** On page 10-7 of the User Manual, the last sentence of the description for the EED bit should read "This bit is always cleared in the other PCI modes."

**Item #12 - PCI Bus Interface**

**Issue:** On page 10-6, the description of the IGM bit should read as follows: This bit controls the operation of the internal arbiter when the PCI interface is configured to operate in a PCI host mode with internal arbiter. When the internal arbiter is used and this bit is cleared, the arbiter operates in a static idle grant mode. This means that once a grant is asserted to a given master, the grant will remain asserted until the requested transaction completes and 16 PCI clock cycles have elapsed. When the internal arbiter is used and this bit is set, the arbiter operates in a dynamic idle grant mode. This means that while the PCI bus is idle, the arbiter may take away a grant from one master and pass it to another. For optimal PCI throughput, this bit should be set to one.

On page 10-8, the description of the CWE bit should read as follows: This bit is set if a CPU PCI write transaction experienced an error and the IPBus Error Enable (IEN) bit is set in the PCIC register.

On page 10-52, the description of the CLS bit should read as follows: This field specifies the size of a cache line in 32-bit words. This field may only be initialized to the following values: 0, 1, 2, 4, 8, 16, 32, 64, 128. Initializing this field to any other value results in the same behavior as initializing this field to zero. **Note**: The PCI master and PCI target transactions use these values differently. For PCI master transactions where the processor is the master initiating a read from another device on the PCI bus, initializing this field to 4 or less results in a 4 word prefetch on the PCI bus while initializing this field to 8 or greater results in an 8 word prefetch (see “Master Memory Read Line” on page 10-21). For PCI target read transactions where the processor is the target device, this field directly controls the number of bytes prefetched. A setting of zero results in a one byte prefetch, otherwise the prefetch matches the setting, e.g., 1 if setting is 1, 2 if setting is 2 ..... 64 if setting is 64, and 128 if setting is 128.