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RENESAS TECHNICAL UPDATE

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Product Category	IIBU/ClockMatrix		Document No.		Rev.	1.10
Title	8A3xxxx Firmware Version v4.8.7 - Errata Notice		Information Category	Technical Notification		
Applicable Product	8A3xxxx, ClockMatrix	Lot No.	Reference Document			

Devices Affected

8A3xxxx devices running firmware version 4.8.7 loaded from internal ROM, or loaded into RAM from an EEPROM or by a host processor.

Issue BRMBXR-3256 Description

A DPLL configured as a GPIO_Slave will use hitless reference switching when it is triggered by GPIO to switch from Master to Slave. This behavior can cause a phase difference between the output of the master and the slave timing devices.

Work-Around

There are two options:

1. After a DPLL is triggered to switch from Master mode to Slave mode by a GPIO, use the DPLL_HS_TIE_RESET control bit to reset the hitless switching time interval error and align the DPLL output with its input reference.

2. Change from Master mode to Slave mode using the DPLL_REF_MODE control register.

Issue BRMBXR-3293 Description

The DPLL_TRANS_CTRL control register is marked as reserved in the Programming Guide, but the register is available. The DPLL_TRANS_CTRL description information is provided below.

Offset Address (Hex)	Register Module Address: C3B0h	
	Individual Register Name	Register Description
022h	DPLL_TRANS_CTRL	Phase transient configuration

DPLL_TRANS_CTRL

DPLL phase transient (phase build-out) configuration.

Offset Address (Hex)	DPLL_TRANS_CTRL Bit Field Locations							
	D7	D6	D5	D4	D3	D2	D1	D0
022h	RESERVED[7:2]						TRANS_SUPPRESS_EN[1]	TRANS_DETECT_EN[0]

DPLL_TRANS_CTRL Bit Field Descriptions			
Bit Field Name	Field Type	Default Value	Description
RESERVED[7:2]	N/A	-	This field must not be modified from its read value
TRANS_SUPPRESS_EN[1]	R/W	0	0 = disabled 1 = enabled
TRANS_DETECT_EN[0]	R/W	0	0 = disabled 1 = enabled

Issue BRMBXR-3301 Description

PWM receivers configured for an external channel cannot receive all 128 bytes of payload if the carrier frequency is lower than 50kHz.

Work-Around

Ensure the carrier frequency is ≥ 50kHz.

Issue BRMBXR-3302 Description

If the OTP or EEPROM configuration has OUT_SYNC_DISABLE bit set to “1” then the output clock might not become active for a random interval of up to 8 seconds after power on reset. This issue does not happen after a warm reset.

Work-Around

Set the OUT_SYNC_DISABLE bit to “0” in OTP and EEPROM configurations.