Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA - 95054
Phone #: (408) 727-6116 Fax #: (408) 727-2328

Errata Notification

EN #: **FEN-01-02** Errata Revision #: 0

Issue Date: August 29, 2001 Effective Date: August 29, 2001

Product Affected: 72V01/02/03/04/05/06, 15ns speed grade.

ERRATA DETAILS: **ATTACHMENT** ■ Yes ☐ No

- ■ Data Sheet Errata
- ☐ Device Manual Errata
- ☐ Application Notes Errata
- ☐ Other (Please Specify)

Datasheet update to reflect correct AC ELECTRICAL CHARACTERISTICS for the 15ns option.

Devices affected:

72V01L15J, 72V02L15J, 72V03L15J, 72V04L15J, 72V05L15J, 72V06L15J

IDT Web Site Location: http://www.idt.com/products/pages/FIFOs_DS_t.html

CUSTOMER NOTIFICATION:

As a result of Errata listed above, IDT has decided to notify you through this Errata Notification.
We recommend you to review this notification in details prior to the use of affected product in your application.
Please use acknowledgement below or E-Mail to request additional information.

If you have any questions, please feel free to contact your local IDT distributor or sales representative.

Customer: _____ E-Mail Address: _____

Name/Date: _____ Phone #: _____

Title: _____ Fax # : _____

CUSTOMER COMMENTS: _____

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C)

		New Datasheet Spec		Previous Data Sheet Spec		
		IDT72V01L15 IDT72V02L15 IDT72V03L15 IDT72V04L15 IDT72V05L15 IDT72V06L15		IDT72V01L15 IDT72V02L15 IDT72V03L15 IDT72V04L15 IDT72V05L15 IDT72V06L15		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
f_S	Shift Frequency	—	**40**	—	50	MHz
t_{RC}	Read Cycle Time	**25**	—	20	—	ns
t_A	Access Time	—	**15**	—	12	ns
t_{RR}	Read Recovery Time	**10**	—	8	—	ns
t_{RPW}	Read Pulse Width[3]	**15**	—	12	—	ns
t_{RLZ}	Read Pulse Low to Data Bus at Low Z[4]	3	—	3	—	ns
t_{WLZ}	Write Pulse High to Data Bus at Low Z[4,5]	5	—	5	—	ns
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	ns
t_{RHZ}	Read Pulse High to Data Bus at High Z[4]	—	**15**	—	12	ns
t_{WC}	Write Cycle Time	**25**	—	20	—	ns
t_{WPW}	Write Pulse Width[3]	**15**	—	12	—	ns
t_{WR}	Write Recovery Time	**10**	—	8	—	ns
t_{DS}	Data Setup Time	**11**	—	9	—	ns
t_{DH}	Data Hold Time	0	—	0	—	ns
t_{RSC}	Reset Cycle Time	**25**	—	20	—	ns
t_{RS}	Reset Pulse Width[3]	**15**	—	12	—	ns
t_{RSS}	Reset Setup Time[4]	**15**	—	12	—	ns
t_{RSR}	Reset Recovery Time	**10**	—	8	—	ns
t_{RTC}	Retransmit Cycle Time	**25**	—	20	—	ns
t_{RT}	Retransmit Pulse Width[3]	**15**	—	12	—	ns
t_{RTS}	Retransmit Setup Time[4]	**15**	—	12	—	ns
t_{RTR}	Retransmit Recovery Time	**10**	—	8	—	ns
t_{EFL}	Reset to Empty Flag Low	—	**25**	—	12	ns
$t_{HFH,FFH}$	Reset to Half-Full and Full Flag High	—	**25**	—	17	ns
t_{RTF}	Retransmit Low to Flags Valid	—	**25**	—	20	ns
t_{REF}	Read Low to Empty Flag Low	—	**15**	—	12	ns
t_{RFF}	Read High to Full Flag High	—	**15**	—	14	ns
t_{RPE}	Read Pulse Width after EF High	**15**	—	12	—	ns
t_{WEF}	Write High to Empty Flag High	—	**15**	—	12	ns
t_{WFF}	Write Low to Full Flag Low	—	**15**	—	14	ns
t_{WHF}	Write Low to Half-Full Flag Low	—	**25**	—	17	ns
t_{RHF}	Read High to Half-Full Flag High	—	**25**	—	17	ns
t_{WPF}	Write Pulse Width after FF High	**15**	—	12	—	ns
t_{XOL}	Read/Write to XO Low	—	**15**	—	12	ns
t_{XOH}	Read/Write to XO High	—	**15**	—	12	ns
t_{XI}	XI Pulse Width[3]	**15**	—	12	—	ns
t_{XIR}	XI Recovery Time	**10**	—	8	—	ns
t_{XIS}	XI Setup Time	**10**	—	8	—	ns