Description
The 8V97003 evaluation board is designed to enable customers to evaluate the functionality and performance of the 8V97003 RF/Microwave Wideband Synthesizer. The 8V97003 device on the evaluation board can be programmed and configured via a PC-based GUI, called Timing Commander, to generate output frequency from 187.5MHz to 18GHz with very low phase noise and RMS phase jitter.

This document discusses the setup of the EVB, and the programming of the 8V97003 using Timing Commander.

Kit Contents
- 8V97003 Evaluation Board
- Micro USB Cable

8V97003 Evaluation Board

Required Software
- IDT Timing Commander Software Installer (available at www.idt.com/timingcommander)
- Network access during installation if the .NET framework is not currently installed on the system
- 8V97003 GUI (available at www.idt.com/8V97003)
- USB 2.0 or USB 3.0 interface
Important Notes

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(i) delivered hardware or software
(ii) non-observance of instructions contained in this manual and in any other documentation provided to user, or
(iii) Misuse, abuse, use under abnormal conditions, or alteration by anyone other than IDT.

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Important Equipment Warning: Ensure the correct connection of all cables. Supplying the board using the wrong polarity could result in damage to the board and/or the equipment. Check that all jumpers have been removed from the board before applying power.
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1. Hardware Setup

This section provides an overview of the different components on the evaluation board. In addition, it discusses the necessary bench equipment, the hardware connection, and the power-up sequence.

1.1 Evaluation Board Overview

The following diagram identifies various components of the board: power supply jacks, input and output SMA connectors, USB interface port, and lock indicator LED.

Figure 1. Evaluation Board Overview

- Power supply (Banana) jacks: +5V DC at J10, GND at J11
- PCB layout revision: For RF Transmission Line Loss information
- Reference clock input SMA connectors: Use J6 and J8 for differential reference clock input; use J6 for single-ended reference clock input
  - Maximum Vpp = 3.3V
  - f_max = 1000MHz when input reference doubler is disabled
  - f_max = 250MHz when input reference doubler is enabled
- Lock detect LED: LED indicator of PLL Lock status
- RF_OUTB/nRF_OUTB output SMA connectors: differential RF/Microwave outputs at J3, J4
- RF_OUTA/nRF_OUTA output SMA connectors: differential RF/Microwave outputs at J1, J2
- SYNC input: J16

Detailed descriptions of these components are as follows (clock-wise from upper left):

- Power supply (Banana) jacks: +5V DC at J10, GND at J11
- PCB layout revision: For RF Transmission Line Loss information
- Reference clock input SMA connectors: Use J6 and J8 for differential reference clock input; use J6 for single-ended reference clock input
  - Maximum Vpp = 3.3V
  - f_max = 1000MHz when input reference doubler is disabled
  - f_max = 250MHz when input reference doubler is enabled
- Lock detect LED: LED indicator of PLL Lock status
- RF_OUTB/nRF_OUTB output SMA connectors: differential RF/Microwave outputs at J3, J4
- RF_OUTA/nRF_OUTA output SMA connectors: differential RF/Microwave outputs at J1, J2
- SYNC input: J16

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1.2 Required Equipment

Several pieces of bench equipment are required for the evaluation of the 8V97003. This section describes the functions of the required equipment.

1.2.1 Power Supply

The evaluation board uses a single +5V DC supply for its power supply. When running the board, set the bench power supply at 5V/1A. The +5V terminal is connected to J10, and the Ground terminal is connected to J11. Multiple LDOs on board are used to generate 3.3V to the 8V97003.

1.2.2 Signal Generator

A signal generator is necessary to generate the reference clock to the 8V97003. A single-ended reference clock is connected to J6, while J8 can be left unconnected. When a differential reference clock is available, connect them to J6 and J8.

Oscillators such as Oven Controlled Oscillators (OCXO) from Wenzel Associates, Inc. can also be used to generate a reference clock to the 8V97003. Some examples of these Wenzel Oscillators are the VHF ULN OCXO (for frequencies from 15MHz to 160MHz) or MXO-FR OCXO (for frequencies greater than 200MHz). However, a signal generator is recommended for the flexibility to experiment with different reference clock frequencies.

1.2.3 Phase Noise Analyzer/Spectrum Analyzer

A phase noise analyzer is necessary to evaluate phase noise performance of the 8V97003. A spectrum analyzer is required to evaluate harmonic performance. Both of these pieces of equipment have (output) power measurement capability.

1.2.4 Balun

Balun is optional. A balun can be used to convert single-ended output of a signal generator to differential output which is used to provide a reference clock to the 8V97003. Another balun can be used to combine the differential outputs of the 8V97003 to a single-ended signal for measurement with a phase noise analyzer/spectrum analyzer.

1.2.5 PC

A PC is required to run the IDT Timing Commander GUI.
1.3 Hardware Connection

Complete the following procedures to set up the evaluation board:

1. Without connecting the bench power supply to the EVB, turn on the bench power supply to make sure the output voltage and current clamp are set to +5V/1A respectively. Then turn off the bench power supply.
2. Connect the bench power supply to the EVB: +5V to J10, GND to J11.
3. Connect the Signal Generator’s output to J6 if single-ended reference input clock configuration is desired. If differential reference input clock configuration is desired, connect the Signal Generator’s output to a balun’s unbalanced port, then connect the balun’s balanced ports to J6 and J8.
4. Connect the RF outputs to measurement equipment.
5. Terminate unused outputs.
6. Connect micro-USB cable: micro-B end of the cable is connected to J12, A-plug is connected to PC.

Table 1. Evaluation Board Connection Descriptions

<table>
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<tr>
<th>Equipment Type</th>
<th>Connection on EVB</th>
<th>Description</th>
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<tr>
<td>(DC) Power Supply</td>
<td>+5V at J10 / GND at J11</td>
<td>5V/1A power supply</td>
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<tr>
<td>Signal Generator</td>
<td>J6 for single-ended) /</td>
<td>Reference clock input to 8V97003</td>
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<td>balun for differential)</td>
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<td>Phase Noise Analyzer</td>
<td>J1, J2, J3, J4</td>
<td>Measure phase noise at RF outputs</td>
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<tr>
<td>Spectrum Analyzer</td>
<td>J1, J2, J3, J4</td>
<td>Measure output power or harmonic performance at RF outputs</td>
</tr>
<tr>
<td>Balun (Macom H-183-4)</td>
<td>J6, J8</td>
<td>Differential reference clock input to 8V97003</td>
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<tr>
<td>Balun (Marki BAL 0026)</td>
<td>J1, J2, J3, J4</td>
<td>Convert differential outputs to single-ended signal for measurements</td>
</tr>
<tr>
<td>Micro-USB</td>
<td>J12</td>
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</table>

1.4 Power-up Procedures

Complete the following steps to power up the evaluation board once the “Hardware Connection” have been completed:

1. Turn the bench power supply on. Initial current consumption of the whole EVB should be around 500mA.
2. Set the reference clock input frequency and amplitude on the Signal Generator – enable Signal Generator output.
3. Program the 8V97003 using IDT’s Timing Commander GUI.
2. Working with Timing Commander™ for Programming/Configuration

2.1 Opening an Existing Configuration

When a customer’s user case information is provided to IDT prior to when the EVB is sampled, an optimized configuration is usually provided to the customer for the evaluation. Complete the following procedure to open a setting file:

1. Power up the evaluation board.
2. Start the Timing Commander software. You will see options of “New Setting File” and “Open Setting File”. Select “Open Setting File”.

3. At the “Open Settings File” dialog box, browse to select the setting file (*.tcs) and the personality file (*.tcp), then click “Open.”

Figure 2. Starting Up Timing Commander GUI

Figure 3. Open Settings File Dialog Box
4. The GUI window with the 8V97003 block diagram will open to show the existing configuration; all configured values will be displayed. In order to connect the board with Timing Commander (PC) and to set up the communication interface, click the “Connect” button (chip symbol) at the upper right corner of the GUI.

The connection will be established if a valid 8V97003 is detected, and a green band appears at the upper right corner of the GUI window.

**Figure 4. Connect to the 8V97003**

5. Click “Write All” to program the 8V97003.

**Figure 5. Program the 8V97003**

6. The 8V97003 is now configured. If the lock detection function is properly configured, the Lock Detect LED should lit once PLL locked status is achieved. The output frequency displayed in the Desired REF_OUTA/B box should also be available for measurements.
2.2 Making Changes to an Existing Configuration

When changes to an existing configuration are necessary, make sure none of the settings in the affected signal path is locked as to allow the GUI to make appropriate calculation for optimal settings. A locked setting is indicated by a white lock symbol in a red box ( ). Complete steps 1 to 3 in “Opening an Existing Configuration” before making changes to the existing configuration.

For example, when changing the input reference frequency, make sure the input doubler enable and the input reference divider settings are unlocked, as shown in Figure 6.

Figure 6. Input Configuration Settings

Another example is when changing the desired output frequency, make sure the Feedback Divider settings are unlocked, as shown in Figure 7.

Figure 7. Feedback Divider Settings

A quick way to view all “Locked” settings in an existing configuration is to select “Locked” option in “Bit Sets” tab, as shown in Figure 8.

Figure 8. “Locked” Settings View in “Bit Sets” Tab
2.3 Creating a New Configuration

Complete the following procedure to create a new setting file:

1. Power up the evaluation board.
2. Start the Timing Commander software. You will see options of “New Setting File” and “Open Setting File”. Select “New Setting File”.
3. In the “New Settings File” dialog box, select “8V97003” and click OK.
4. The GUI window with the 8V97003 block diagram will open with no setting on any of the blocks.

Figure 9. New Settings GUI

5. Click on each functional block of the block diagram to enter the desired settings/configuration or to check automatically calculated settings/configuration. An invalid setting/configuration will result in an “Error”. Settings/configurations that are not invalid but not optimum will result in “Warning”. Errors must be resolved before proceeding.

6. Once all settings have valid values, click the Connect button (chip symbol) at the upper right corner of the GUI to set up the communication interface.

The connection will be established if a valid 8V97003 is detected, and a green band appears at the upper right corner of the GUI window.

7. Click “Write All” to program the 8V97003.

For examples of creating New Configurations for 8V97003, see Appendix A.
3. Performance Evaluation with the 8V97003 EVB

Because the 8V97003 supports a very wide range of output frequencies, careful consideration must be given to component selection and termination to ensure signal integrity, especially at high output frequencies. In addition, because impedance is a function of frequency, (amplitude) loss of transmission line should also be characterized over frequency to ensure accurate de-embed of trace loss.

This section discusses the following topics when evaluating performance of the 8V97003:

- Output matching
- AC-coupling (series) capacitor
- Proper termination when making measurements on single-ended output
- Transmission line loss

3.1 Output Matching

The 8V97003 provides two differential outputs of CML type. The outputs are “open collector outputs” and can be matched in different ways. By default, a simple resistive matching is used on the 8V97003 EVB. This resistive matching consists of a 50Ω resistor to VDD, with a series AC coupling capacitor. This matching scheme gives the output amplitude a “broadband” response but is not ideal to achieve maximum output power transmission, especially for high frequencies.

An inductive matching is recommended for better performance and optimal power transmission. For the inductive matching scheme, the 50Ω resistors connected to VDD are replaced by inductors. The inductor value is frequency dependent.

An inductive matching is recommended for better performance and optimal power transmission. For the inductive matching scheme, the 50Ω resistors connected to VDD are replaced by inductors. The inductor value is frequency dependent.

Figure 10. 8V97003 Output Power over Frequencies – Resistive vs. Inductive Matching

For impedance matching of 50Ω, the inductor value can be calculated as $L = \frac{50}{(2 \times \pi \times f)}$ where $f$ is the operating frequency. In the data shown in Figure 10, a 1nH would provide a 50.24Ω match at $f = 8$GHz Therefore, for the same output power setting, the measured output power with the 1nH inductive matching is 2dB higher than that with 50Ω resistive match at 8GHz.

When selecting the inductors for output matching, it is critical to select inductors whose self-resonant frequency is higher than the operating frequency.
3.2 AC-coupling Capacitor

AC-coupling capacitors are populated on the 8V97003 EVB to ensure 0V DC on the output signals when they are connected to the input of (RF) measurement equipment. The part number of the (series) AC-coupling capacitor used on the 8V97003 EVB is 520L103KT16T, which is specified for operation up to 16GHz. The same consideration regarding self-resonant frequency also applies when selecting this capacitor.

For output frequencies above 16GHz, IDT recommends these AC-coupling capacitors be replaced with 0Ω resistors, and a high-performance external DC block be used to ensure 0V DC input to (RF) measurement equipment.

3.3 Termination

As mentioned in “Output Matching”, the outputs of the 8V97003 are “open collector outputs.” Therefore, when making single-ended measurements on one branch of the differential pair, it is critical to properly terminate the unused port to minimize distortion (due to reflection) of the output signal.

Because the built-in load of most (RF) measurement equipment is 50Ω, when making single-ended measurements on one branch of the differential pair, terminate the unused port with a 50Ω load. At high frequencies, the mismatch in electrical length at which each branch of the differential pair is terminated could result in reflection that would distort the output signal. IDT recommends that at high frequencies, each branch of the differential pair be terminated at the same electrical length. This means when making single-ended measurements on one branch of the differential pair at high frequency, connect the unused port to a cable of the same length with the cable connecting the port being measured, and terminate that cable with 50Ω load.

3.4 Transmission Line Loss

To accurately characterize the output power of the 8V97003 RF/Microwave Synthesizer, insertion loss of all components in the measurement path should be accurately accounted. Besides the insertion loss of the RF cables, and balun (if applicable), loss across frequencies due to transmission line on the EVB must also be characterized.

To assist customers with the measurement of trace loss on the 8V97003 EVB, a test “coupon” is included in the same PCB manufacturing panel with the main EVB. This test coupon consists of the exact copy of the transmission lines on the board and the SMA connectors.

The insertion loss of the transmission lines on EVB Revision D is displayed in Figure 11. The measurement was taken on the test coupon using a network analyzer, with \( Z_{\text{source}} = Z_{\text{load}} = 50\Omega \). On the actual EVB with the 8V97003 as device-under-test (DUT), the source impedance (including output buffer, bond wire, package, and external matching components) is probably not a perfect 50Ω. Therefore, the mismatch between the source impedance and the transmission line could cause reflection that would likely present more loss to the output signal. The insertion loss measured on the test structure shown above should be used as the minimum loss the output signal will suffer.
Figure 11. Transmission Line Loss – 8V97003 EVB Revision D

The insertion loss of the transmission lines on EVB Revision C is displayed in Figure 12. The high insertion loss is caused by reflection along the transmission line which was due to larger-than-expected tolerance of the designed characteristic impedance of 50Ω. This issue causes performance degradation in output power, harmonic, and phase noise. This trace loss should be considered if you are evaluating the 8V97003 RF/Microwave Synthesizer on IDT’s EVB Revision C.

Figure 12. Transmission Line Loss – 8V97003 EVB Revision C
4. Schematics

Figure 13. Evaluation Board Schematic – Page 1

TCED Layout Notes:
1. Overlapping Q0 and U1 footprint
2. U1 uses 4 pads, U3 can use 6 pads (skipping 4 and 5)
3. Keeping branching traces short
4. U50/41 and U52/42 unless U5 or U13 is used
5. RX1/45 and RX5/46 are used only when U7 is used
6. Place RXA/Q47 close to the branching point meeting with RX1 traces of the same net as U5
Figure 14. Evaluation Board Schematic – Page 2
5. Bill of Materials (BOM)

Table 2. Evaluation Board BOM

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6. Board Layout

Figure 16. Evaluation Board – Top Layer

Figure 17. Evaluation Board – Second Layer

Figure 18. Evaluation Board – Third Layer

Figure 19. Evaluation Board – Bottom Layer

7. Ordering Information

Contact Renesas Sales at https://www.idt.com/buy-sample/locations.
Appendix A – New Configuration Examples

Example 1 – New Configuration for Integer Mode of Operation

In this example, the Timing Commander GUI's is used to create a new configuration for the 8V97003 with the following operating parameters:

- Input Reference Frequency: 245.76MHz; Input signal type: Differential
- Desired Output Frequency: 8110.08MHz; Desired output power: +2dBm

Follow instructions in steps 1-4 of "Creating a New Configuration” to bring up the GUI for a new configuration, then enter the operating parameters as follows:

1. Enter input reference frequency 245.76 in the "REF_IN (MHz)" box.
2. Click on the Input Buffer icon to open the Input Buffer configuration. Check the “Differential” box to specify differential input signal.
3. Click on the "Input Config" box to open the input path configuration to check the PFD frequency. The PFD frequency is automatically calculated based on the REF_IN input and the Desired Output Frequency. Because the Desired Output Frequency is not yet entered, this PFD frequency may change.
4. Enter the Desired Output Frequency 8110.08 in the “Desired REF_OUTA (MHz)” box.
   • With REF_IN frequency, input path configuration, and desired output frequency information, the GUI will automatically calculate the feedback divider.
   • In this case, with REF_IN = 245.76, PFD Frequency = 245.76, RF_OUT = 8110.08, the feedback divider is calculated to be 33.
5. Click on the Output driver icon to open RF_OUTA configuration.
   a. Select +2dBm from the Power pull-down menu.
   b. Make sure Power Down = “Regulator Enabled” and Enabled box is checked.
6. Click on the Lock Detect icon to open Lock Detect Configuration
   a. Set Pin Mode = “Digital Lock Detect” (already set by default)
   b. Precision = 6.4ns
7. Set the operating Charge Pump current.
   • By default, the charge pump current is set to 5mA.
   • The charge pump current can be used to vary the loop bandwidth, therefore, to optimize phase noise and/or integrated RMS jitter. Set Pmos = 8.5mA and Nmos = 8.5mA to get the performance in the phase noise plot displayed in Figure 21.
Figure 20. Timing Commander GUI for Creating New Integer Mode Configuration
Figure 21. Expected Performance of 8110.08MHz Output from Example 1
Example 2 – New Configuration for Fractional Mode of Operation

In this example, the Timing Commander GUI is used to create a new configuration for the 8V97003 with the following operating parameters:

- Input reference frequency: 245.76MHz; Input signal type: Differential
- Desired output frequency: 8200MHz; Desired output power: +2dBm

Complete the instructions in steps 1-4 in “Creating a New Configuration” to bring up the GUI for a new configuration, then enter the operating parameters as follows:

1. Enter the input reference frequency 245.76 in the “REF_IN (MHz)” box.
2. Click on the Input Buffer icon to open the Input Buffer configuration. Check the “Differential” box to specify differential input signal.
3. Click on the “Input Config” box to open input path configuration to check the PFD frequency. The PFD frequency is automatically calculated based on the REF_IN input and the Desired Output Frequency. Because the Desired Output Frequency is not yet entered, this PFD frequency may change.
4. Enter the Desired Output Frequency 8200 in the “Desired REF_OUTA (MHz)” box.
   - With REF_IN frequency, input path configuration, and desired output frequency information, the GUI will automatically calculate the feedback divider.
   - In this case, with REF_IN = 245.76, PFD Frequency = 245.76, RF_OUT = 8200, the feedback divider is calculated to be $\frac{33.36588}{1571465805} = 1571465805$.
5. Click on the Output driver icon to open RF_OUTA configuration.
   a. Select +2dBm from the Power pull-down menu.
   b. Make sure Power Down = “Regulator Enabled” and Enabled box is checked.
6. Click on the Lock Detect icon to open Lock Detect Configuration.
   a. Set Pin Mode = “Digital Lock Detect” (already set by default).
   b. Precision = 6.4ns.
7. Set the operating charge pump current.
   a. By default, charge pump current is set to 5mA.
   b. The charge pump current can be used to vary the loop bandwidth, therefore, optimize phase noise and/or integrated RMS jitter. Set Pmos = 8.5mA, Nmos = 8.5mA, Bleeder = OFF. With the Bleeder off, the noise from the modulator will degrade phase noise performance as shown in Figure 23.
   c. Set Pmos = 8.5mA, Nmos = 8.5mA, Bleeder = 1100µA to improve phase noise performance as shown in Figure 24.
Figure 22. Timing Commander GUI for Creating New Fractional Mode Configuration
Figure 23. Expected Performance of 8200MHz Output without Bleeder Current from Example 2
Figure 24. Expected Performance of 8200MHz Output with 1.1mA of Bleeder Current from Example 2
Appendix B – Input Reference Phase Noise Performance

Phase noise measurement results shown in Figure 21, Figure 23, and Figure 24 were obtained with the input reference clock from a bench signal generator. Because the in-band phase noise performance of the 8V97003 is dictated by the phase noise performance of the input reference, the input reference’s phase noise performance is provided below.

Figure 25. Phase Noise Performance of 245.76MHz Input Reference Clock
## Revision History

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<td>December 2, 2019</td>
<td>- Updated Figure 1 and added additional bullet (second bullet) to the board descriptions</td>
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<td>- Updated Transmission Line Loss</td>
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<td>- Updated Figure 13 and Figure 14</td>
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<td>September 5, 2019</td>
<td>- Updated the document to corporate standards</td>
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<td>- Completed minor changes throughout</td>
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<tr>
<td>July 24, 2019</td>
<td>- Add Appendix A: New Configurations Examples</td>
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<td>- Add Appendix B: Input Reference Phase Noise Performance</td>
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<td>- Initial Release</td>
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