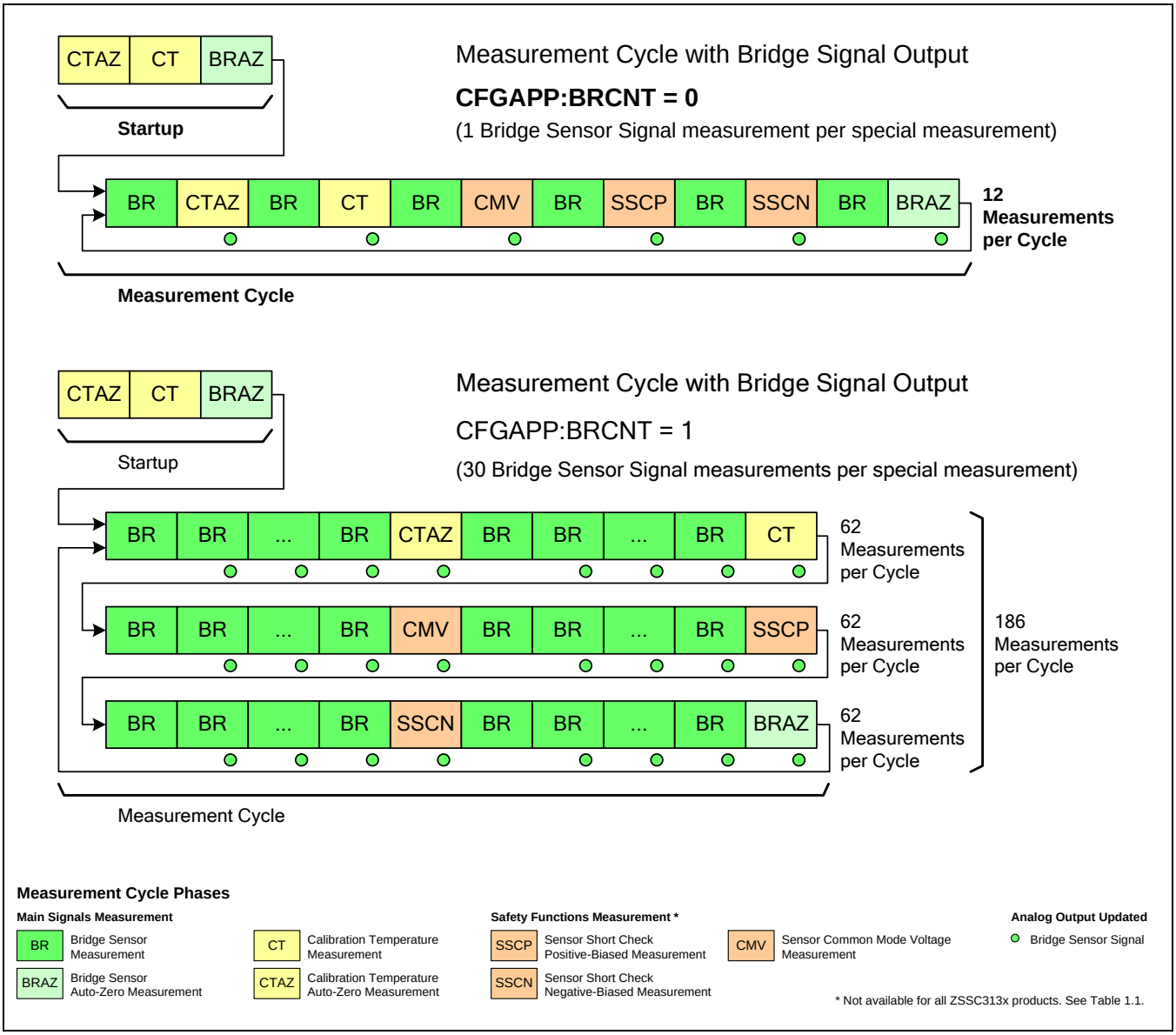
Contents

Figure 1.1 Measurement Cycle



1.3.2 Command Mode (CM)

The Command Mode (CM) is the working mode that is used for calibration data acquisition and access to the internal RAM and EEPROM of the ZSSC313x. The CM start command START_CM aborts the running NOM, so the measurement cycle stops. The ZSSC313x changes to CM only after receiving the START_CM command by digital serial communication (I^2C™ or OWI). This protects the ZSSC313x against interruption of processing the NOM (continuous signal conditioning mode) and/or unintentional changes of configuration. In CM, the full set of commands is supported (see section 4.1).

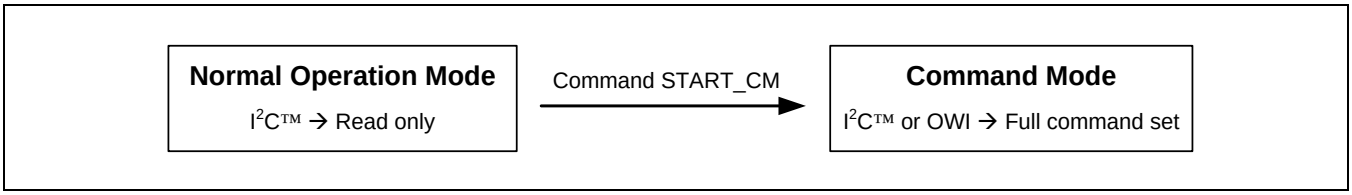
Starting CM via I²C™ communication (SCL and SDA pins) is possible at any time. If starting CM via one-wire communication (AOUT pin), the START_CM command must be transmitted when OWI is enabled, i.e. during the OWI startup window or during permanent OWI output mode (see section 3.4.2 for OWI configuration).

If the ZSSC313x receives a command other than START_CM in NOM, it is not valid. It is ignored and no interrupt to the continuous measurement cycle is generated. Refer to section 4.4.1 for a detailed description of the START_CM command.

In CM, the full command set is enabled for processing. During processing of a received command, the digital serial interfaces are disabled; no further commands are recognized. After finishing the processing, the CMC waits for further commands or processes requested measurement loops continuously.

EEPROM programming is only enabled after receiving the EEP_WRITE_EN command.

Figure 1.2 Modes of Digital Serial Communication



1.3.3 Diagnostic Mode (DM)

The ZSSC313x detects various failures. When a failure is detected, Diagnostic Mode (DM) is activated. DM is indicated by setting the output pin AOUT to the Lower Diagnostic Range (LDR). When using digital serial communication protocols (I²C™ or OWI) to read out conditioning results data, the error status is indicated by a specific error code.

OWI communication is enabled during DM. Because the analog output pin AOUT is driven to the diagnostic range, the AOUT pin must be overwritten when starting OWI communication. The communication master must provide driving capability (AOUT current limitation: <20mA).

Note that many of the error detection features can be enabled or disabled by configuration words CFGAPP and CFGSF (see section 5.3).

There are three possible conditions for Diagnostic Mode determined by the type of error (see Table 1.1):

- **Steady Diagnostic Mode**
  In steady DM, the measurement cycle is stopped and failure notification is activated.
  If enabled by the configuration bit ADJREF:DMRES, a reset after the time-out of a watchdog is executed.
- **Temporary Diagnostic Mode**
  There is a failure counting sequence that can result in a temporary DM. DM is activated after two consecutively detected failure events and is deactivated after a failure counter counts down if the failure condition is no longer detected. The measurement cycle is continuously processed during temporary DM.
- **Power and Ground Loss**
  Power and ground loss cases are signaled by setting the analog output pins to high-impedance states. The output levels are determined by the external loads.

1.3.4 Failsafe Tasks and Error Codes

Table 1.1 Error Detection Functionality and Error Codes

Failsafe Task		Description	Messaging Time	Error Code[1)]	Activation	Action
Oscillator Fail Detection		Oscillator is observed generating clock pulses by an asynchronous timing logic	< 200µs	-	-	Temporary DM
Watchdog		Watchdog time-out during initialization or measurement cycle	Startup, two measurement times	$C008_{HEX}$	-	Steady DM or reset after watchdog time-out (if enabled by ADJREF: DMRES)
Register Parity		Hard-wired parity check of configuration registers	Immediately	$C002_{HEX}$	-	
RAM Parity		Parity check at every RAM access	Immediately	$C001_{HEX}$	-	
EEPROM Multiple-Bit Error		Detection of non-correctable multiple-bit error per 16-bit word	Startup	$C004_{HEX}$	-	Steady DM
EEPROM Signature		Checks signature of RAM mirror against signature stored in EEPROM	Startup	$C0AA_{HEX}$	-	
ZSSC3136 only	**ROM Signature**	Checks CMC ROM signature Note that this check increases startup time by 10ms.	Startup	$C0CC_{HEX}$	CFGAPP: CHKROM	
	Arithmetic Check	Functional check of arithmetic unit	Two measurement cycles	$C010_{HEX}$	-	Temporary DM
	Data Bus Check	Functional check of internal peripheral data bus			-	
	MCCH	Main channel check – High: Detection of positive overdriving the analog front-end during bridge measurement			CFGSF: CHKMCCH	
	MCCL	Main channel check – Low: Detection of negative overdriving the analog front-end during bridge measurement			CFGSF: CHKMCCL	
	SAC	Bridge sensor aging check			CMVMIN / CMVMAX	
ZSSC3135/36/38	**TSC**	Temperature sensor check			CFGAPP: CHKTS	
	SCC	Bridge sensor connection check			CFGAPP: CHKSENS	
	SSC	Bridge sensor short check			CFGAPP: CHKSENS, CFGSF: SSCDIS	
Power & Ground Loss		Power and ground loss detection	< 5ms	-	-	Reset

1) Error codes can be bitwise OR-combined. Note that the reset after the watchdog time-out clears any error codes that were previously generated.

1.3.4.1 Main Channel Check (MCCH / MCCL) available in ZSSC3136

The main channel check detects whether the ADC dynamic range has been exceeded during the bridge measurement. The bridge signal raw value is checked if it is less than 128 or greater than ($2^{r_{ADC}}$ - 128) where r_{ADC} is the selected ADC resolution. 16/15-bit values are shifted to 14/13-bit before the check.

This can result from various causes: the bridge sensor is disconnected; the main input channel is defective or not sufficiently calibrated; or the bridge signal is out of targeted range.

The main channel check distinguishes between positive (MCCH) and negative (MCCL) overdrive to allow tailored overdrive handling at the bridge channel.

1.3.4.2 Bridge Sensor Aging Check (SAC) available in ZSSC3136

The sensor aging check detects long-term altering of the bridge sensor resistors that would result in a shift of the calibrated output characteristics. The SAC evaluates the common mode voltage of the sensor bridge once per measurement cycle if enabled. The measurement result is checked for compliance with programmed limits (CMVMIN / CMVMAX).

1.3.4.3 Temperature Sensor Check (TSC) available in ZSSC3135, ZSSC3136 and ZSSC3138

The temperature sensor check detects whether the ADC dynamic range has been exceeded during the temperature measurement. The temperature signal raw value is checked if it is less than 128 or greater than ($2^{r_{ADC}}$ - 128) where r_{ADC} is the selected ADC resolution. 16/15-bit values are shifted to 14/13-bit before check.

This can result from various causes: the external temperature sensor is disconnected; the analog temperature input channel is not sufficiently calibrated or defective; or the temperature signal is out of targeted range.

1.3.4.4 Bridge Sensor Connection Check (SCC) available in the ZSSC3135, ZSSC3136 and ZSSC3138

The sensor-connection check monitors the connection of the bridge sensor at the VBP and VBN pins. An internally determined current is applied to the sensor, and the resulting differential input signal is evaluated once per measurement cycle if enabled. The following failures are detected by SCC:

- High-resistive sensor bridge elements (e.g., a diaphragm rapture)
- Connection loss at the pins VBP, VBN, VBR_T, or VBR_B
- Short between pins VBP or VBN and pins VBR_T or VBR_B

1.3.4.5 Bridge Sensor Short Check (SSC) available in ZSSC3135, ZSSC3136 and ZSSC3138

The sensor-short check detects a short between the bridge sensor input pins VBP and VBN (connections less than 50Ω nominal). An internally determined current is applied to the sensor in both directions, resulting in differential input signals that are evaluated once per measurement cycle if enabled. If a short occurs, the input signal difference of both is less than an internally determined limit.

Increasing the sensor-short check limit via CFGAPP:CHKSSCL is recommended in the case of a sensor bridge with low impedance (less than 2kΩ).

1.3.4.6 Power and Ground Loss

Detection of a power or ground loss is indicated by pulling the analog output AOUT to the diagnostic range. The level of the diagnostic output depends on the lost node and load connection to ground or supply. In such cases, the ZSSC313x is inactive and the specified leakage current in combination with the load resistor guarantees reaching the Upper Dignostic Range (UDR) or the Lower Diagnostic Range (LDR).

2 Signal Conditioning

2.1 A/D Conversion

During NOM, the analog preconditioned sensor signal is continuously converted from analog to digital. The analog-to-digital (A/D) conversion is performed with the selected resolution r_{ADC}, which is equal for all measurements in the measurement cycle (e.g., bridge sensor signal, calibration temperature, auto-zero, etc.). The A/D conversion is configurable regarding the inherent range shift rs_{ADC} for the bridge sensor signal measurement. One or two step A/D conversion mode is selectable; the two-step mode is faster, the one-step mode is more accurate because of its longer integration time. All resulting digital raw values are determined by the following equations:

Analog differential input voltage to A/D conversion

$$V_{ADC\_DIFF} = a_{IN} \cdot V_{IN\_DIFF} + a_{XZC} \cdot V_{XZC} \quad (1)$$

Where

V_{ADC_DIFF} Differential input voltage to ADC

a_{IN} Gain of analog front-end for differential input voltage

V_{IN_DIFF} Differential input voltage to analog front-end.

Extended Zero Compensation (ZSSC3138 only):

a_{XZC} Gain of extended zero compensation voltage

V_{XZC} Extended zero compensation voltage = $-(-1^{BRXZCPOL}) * V_{ADC\_REF} * BRXZC / 48$
using CFGAFE:BRXZC and CFGAFE:BRXZCPOL (see section 5.3); see below for V_{ADC_REF}.

Digital raw A/D conversion result Z_{ADC}

$$Z_{ADC} = 2^{r_{ADC}} \cdot \left(\frac{V_{ADC\_DIFF} + V_{OFF}}{V_{ADC\_REF}} + rs_{ADC} \right) \quad (2)$$

Where

r_{ADC} Resolution of A/D conversion (ZSSC3131/35/36: 13, 14 bit; ZSSC3138: 13, 14, 15, 16 bit)

V_{OFF} Residual offset voltage of analog front-end (which is eliminated by auto-zero compensation)

V_{ADC_REF} ADC reference voltage (ratiometric reference for measurement)

rs_{ADC} Range shift of A/D conversion (bridge sensor: ½, ¼, $^1/_8$, $^1/_{16}$; Temperature: ½)

Auto-zero value Z_{AZ}

$$Z_{AZ} = 2^{r_{ADC}} \cdot \left(\frac{V_{OFF}}{V_{ADC\_REF}} + rs_{ADC} \right) \quad (3)$$

Auto-zero corrected raw A/D conversion result Z_{CORR}

$$Z_{CORR} = Z_{ADC} - Z_{AZ} = 2^{r_{ADC}} \cdot \frac{V_{ADC\_DIFF}}{V_{ADC\_REF}} \quad (4)$$

2.2 Digital Value Range Zooming (ZSSC3138 only)

The digital zooming feature is available for the ZSSC3138 only. The result of the A/D conversion Z_{CORR}, which is the input value for the signal conditioning formula, depends on the resolution setting r_{ADC} ranging from 13 to 16 bit resolution. Raw values acquired with resolutions of 15 and 16 bits must be mapped to the 13 **or** 14 bit resolution range for further calculations. This is done by different methods depending on the data to be measured:

- SSC+ and SSC- measurements for diagnostic checks are always shifted to 13 bits.
- The temperature measurement value (Z_{CORR_T}) is divided by 4.
- The bridge sensor (BR) measurement auto-zero corrected data (Z_{CORR}) must be moved in the +/- 2^{15} range (see Table 2.1) by subtraction of the offset determined in configuration register CFGAPP:BROFFS (see Table 5.4). Minimum and maximum input data (span of Z_{CORR} raw data) should have 14-bit **or** slightly higher resolution (16384 ADC counts) for proper calibration coefficients calculation.

AD conversion result segmentation calculation (only if r_{ADC} = 15 or 16 bit)

$$Z_{CORR\_OUT} = Z_{CORR} - BROFFS * 2^{13} \qquad \text{with BROFFS} \in [0; 7] \quad (5)$$

Where

Z_{CORR} Raw input main channel A/D result for measured value (auto-zero compensated; $D8_{HEX}$ and $D9_{HEX}$ commands)

Z_{CORR_OUT} Raw main channel A/D result for measured value (auto-zero compensated), mapped in range given in Table 2.1

$$Z_{CORR\_TOUT} = \frac{Z_{CORR\_T}}{4} \quad (6)$$

Where

Z_{CORR_T} Raw temperature input A/D result for measured value (auto-zero compensated)

Z_{CORR_TOUT} Raw temperature A/D result for measured value (auto-zero compensated), mapped in range [-2^{14}; 2^{14})

Note: All raw data acquiring commands (Dx commands listed in Table 4.1) do not process the shifting procedure, and therefore 15 and 16 bit results are read out. Therefore, the acquired data must be processed according to the Z_{CORR_OUT} and Z_{CORR_TOUT} formulas above in the following sequence before calculation of the calibration coefficients:

1. Raw calibration data acquisition
2. Z_{CORR_OUT} calculation for the main channel data and the Z_{CORR_T} calculation for temperature data
3. Calibration coefficients calculation using calculated corrected raw data

Important: Results of the ADC conversion Z_{CORR_OUT} greater than +32767 counts (15 bits) will result in negative read-out values and a wrong analog output voltage for AOUT. In this case, a greater offset BROFFS, adjusted ADC Range Shift, or lower gain should be used.

Table 2.1 Valid Data Ranges for 15-bit and 16-bit ADC Resolution

ADC Resolution	Data	ADC Range Shift							
		1/2		3/4		7/8		15/16	
		Min	Max	Min	Max	Min	Max	Min	Max
16 bits	Z_{CORR} ($D8_{HEX}$ and $D9_{HEX}$ commands)	-32768	32767	-16384	49151	-8192	57343	-4096	61439
15 bits		-16384	16383	-8192	24575	-4096	28671	-2048	30719
16 bits	Z_{CORR_OUT}	-32768	32767	-16384	32767	-8192	32767	-4096	32767
15 bits		-16384	16383	-8192	24575	-4096	28671	-2048	30719

Recommendation: To avoid possible ADC saturation, perform a check on the ADC raw data ($D0_{HEX}$ and $D1_{HEX}$ commands). For results close to the limits [$0\text{-}2^{res}$), a lower gain or adjusted ADC Range Shift should be used.

2.3 Signal Conditioning Formula

The digital raw value Z_{CORR} for the measured bridge sensor signal is processed with a conditioning formula to remove offset and temperature dependency and to compensate nonlinearity up to the 3rd order. The signal conditioning equation is processed by the CMC and is defined as follows:

⇒ Range definition of inputs

$$Z_{CORR} \in \left[-2^{r_{ADC}} ; 2^{r_{ADC}} \right) \tag{7}$$

$$Z_{CORR\_T} \in \left[-2^{r_{ADC}-1} ; 2^{r_{ADC}-1} \right) \tag{8}$$

Where

Z_{CORR} Raw A/D conversion result for bridge sensor signal (auto-zero compensated)

r_{ADC} Resolution of A/D conversion (13 or 14 bit)

Z_{CORR_T} Raw A/D conversion result for calibration temperature (auto-zero compensated)

⇒ Conditioning Equations

$$Y = \frac{Z_{CORR} + c_0 + 2^{-(r_{ADC}-1)} c_4 Z_{CORR\_T} + 2^{-2(r_{ADC}-1)} c_5 Z_{CORR\_T}^2}{c_1 + 2^{-(r_{ADC}-1)} c_6 Z_{CORR\_T} + 2^{-2(r_{ADC}-1)} c_7 Z_{CORR\_T}^2} \quad Y \in [0;1) \tag{9}$$

$$S = Y \cdot \left(1 - 2^{-15} c_2 - 2^{-15} c_3\right) + 2^{-15} c_2 Y^2 + 2^{-15} c_3 Y^3 \quad S \in [0;1) \tag{10}$$

Where

Conditioning coefficients stored in EEPROM registers 0 to 7: $c_i \in [-2^{15}; 2^{15})$, two's complement.

c_0 Bridge offset

c_1 Bridge gain

c_2 Non-linearity correction 2nd order

c_3 Non-linearity correction 3rd order

c_4 Temperature coefficient for bridge offset 1st order

c_5 Temperature coefficient for bridge offset 2nd order

c_6 Temperature coefficient for gain 1st order

c_7 Temperature coefficient for gain 2nd order

The first equation compensates the offset and fits the gain including its temperature dependence. The nonlinearity is then corrected for the intermediate result Y. The result of these equations is a non-negative value S for measured bridge sensor signal in the range [0; 1). Note that the conditioning coefficients c_i are positive or negative values in two's complement.

2.4 Fitting Conditioning Result to Analog or Digital Output

The analog output is generated by a 5632-step D/A converter. This guarantees 12-bit analog output resolution for a typical output range of 10-to-90% V_{DDA} or larger. For the calibration of the conditioning coefficients, the target output values must be fitted to that DAC resolution.

The ***fitting factor is 0.6875*** = $\left(5632/2^{13}\right)$ and is ***applied to the normalized target values S*** $\in$ ***[0; 1)***.

Note that this fitting is supported by the ZSSC313x calibration software, but ***fitting is not included in RBIC1.DLL***. Refer to *ZSSC313x Technical Note – Calibration DLL Description* for stand-alone usage of the DLL.

The conditioned 15-bit value S is continuously written to the output register of the digital serial interface during the measurement cycle and can be readout via I²C™ or OWI communication. Note, if only digital ouput via I²C™ or OWI is used, fitting S to the DAC range is not advisable. Instead the full 15-bit resolution/accuracy should be used.

2.5 Digital Filter Function

The ZSSC313x offers a digital (averaging) low-pass filter for the analog output signal at the AOUT pin. The output value is filtered with the integrating coefficient LPFAVRG and the differential coefficient LPFDIFF (refer to section 5.2). Note that setting the coefficients LPFAVRG and LPFDIFF to 0 disables the filter function.

The filter function is implemented as follows:

⇒ **Digital Filter Function**

$$S_{OUT,0} = S_0 \tag{11}$$

$$S_{OUT,i} = S_{OUT,i-1} + \left(S_i - S_{OUT,i-1}\right) \cdot \frac{LPFDIFF + 1}{2^{LPFAVRG}} \qquad i>0; \qquad S_{OUT,i} \in [\,0;1) \tag{12}$$

with LPFAVRG, LPFDIFF $\in$ [0; 7]

Where

S_i	Conditioned output value (see section 2.3)
$S_{OUT,I}$	Filtered output value
LPFAVRG	Low-pass filter coefficient stored in EEPROM: averaging filter coefficient
LPFDIFF	Low-pass filter coefficient stored in EEPROM: differential filter coefficient

The result of the filter function is a non-negative value $S_{OUT,i}$ in the range [0; 1), which is used for continuously updating the analog output value during the measurement cycle.

Important: For proper function, ensure that the factor $\frac{LPFDIFF + 1}{2^{LPFAVRG}}$ never becomes larger than 1.

2.6 Analog Output Signal Range and Limitation

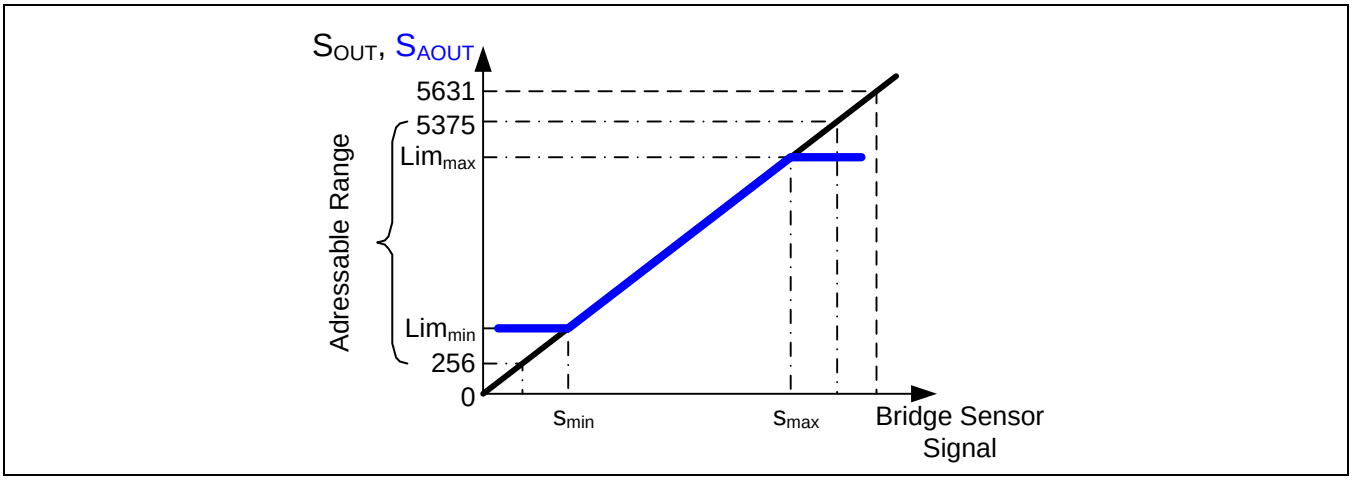
The filtered conditioning result S_{OUT} for the measured bridge signal is output at the analog output pin AOUT with a resolution greater than 12 bits. The analog output voltage is generated using a resistor-string DAC with 5632 steps, of which 5120 steps (256 to 5375) can be addressed. Consequently an adjustable range from 5% to 95% of the supply voltage is guaranteed, including all possible tolerances.

$$V_{OUT\_MIN} = (V_{VDDE} - V_{VSSE})\frac{256}{5632} \qquad V_{OUT\_MAX} = (V_{VDDE} - V_{VSSE})\frac{5375}{5632} \tag{13}$$

Setting the analog output outside the allowed range (for example via the SET_DAC command) will result in entering the diagnostic mode (DM) and setting the output to the LDR (Lower Diagnostic Range).

Note that the limit setting registers 8 and 9 are shared with the digital filter configuration (the 3 LSBs).

Figure 2.1 Accessable Output Signal Range and Limitation



3 Serial Digital Interfaces

3.1 General Description

The ZSSC313x includes a serial digital I²C™ interface and a ZACwire™ interface for one-wire communication (OWI). The digital interfaces allow programming the EEPROM to configure the application mode for the ZSSC313x and to calibrate the conditioning equations. It also provides the readout of the conditioning results as a digital value. The ZSSC313x always works as a slave.

I²C™ access to the ZSSC313x is available in all operation modes independent of the programmed configuration. The I²C™ interface is enabled after power-on and a short initialization phase. In Normal Operation Mode (NOM), the result values for the bridge sensor signal can be read out.

For OWI communication, there are four possible access modes during NOM selectable by the ADJREF:IFOWIM bits. A mode with continuous OWI access and two startup window modes are available. The startup window modes differ in the analog output behavior: with simultaneous analog output or without analog output. The fourth option is to lock OWI access; in this case, communication is only available via I²C™.

Transmitting the command START_CM enables the Command Mode (CM). In CM, either communication protocol can be used; all commands are available to process calibration. EEPROM write access via I²C™ is always available in CM. The EEPROM lock bit only affects EEPROM write access via OWI communication (see section 3.4.2).

In Diagnostic Mode (DM), both communication protocols can be used to read an error code to identify the error source. A non-configured device, identified by a non-consistent EEPROM signature, starts up in DM. Because the analog output pin AOUT is driven to the lower diagnostic range in DM, the analog output must be overwritten when starting communication using OWI communication. Starting CM from DM by transmitting the START_CM command is possible by using I²C™ or OWI communication.

In NOM, CM, and DM, an alternating use of communication protocols is permitted.

3.1.1 Command Structure

A command consists of a device address byte and a command byte. Some commands (e.g. writing data into EEPROM) also include two data bytes. The command structure is independent from the communication protocol used. Refer to section 1.3 for details of working modes and section 4 for command descriptions.

3.1.2 Addressing

Addressing is supported by I²C™ and OWI communication protocol. Every slave connected to the master responds to a defined address. After generating the start condition, the master sends the address byte containing a 7-bit address followed by a data direction bit (R/W). ”0” indicates a transmission from master to slave (WRITE); “1” indicates a data request (READ). The addressed slave answers with an acknowledge bit (I²C™ only). All other slaves connected to the master ignore this communication.

The ZSSC313x always responds to its general ZSSC313x slave address, which is 78_{HEX} (7bit). Via EEPROM programming, it is possible to allocate and activate an additional unique slave address within the range 70_{HEX} to $7F_{HEX}$ to the ZSSC313x. In this case, the device recognizes communication on both addresses, on the general one and on the additional one.

3.1.3 Read-Request

There are two general methods/requests for reading data from the ZSSC313x:

- Digital read out
  ➔ (Continuously) reading the conditioned result in NOM via I²C™ or via OWI communication

  During the measurement cycle, the ZSSC313x transfers the conditioned result for bridge sensor signal into the output registers of the digital interfaces. These data will be sent if a master generates a read-request via I²C™ or via OWI. The active measurement cycle is not interrupted by this.
- Calibration and/or configuration tasks via I²C™ or via OWI communication
  ➔ Reading internal data (e.g. EEPROM content) or acquired measurement data in CM

  To read internal and/or measurement data from the ZSSC313x in CM, usually a specific command must be sent to transfer this data into the output registers of the digital interfaces. Thereafter the data will be sent if the master generates a read-request.

3.1.4 Communication Verification

In Normal Operation Mode (NOM) and in Command Mode (CM), a read request is answered by return of the data present in the digital interface output registers (2 bytes). Next a check sum is sent (1 byte) followed by the command which is answered (see section 3.2). The check sum and the returned command allow the verification of received data by the master. For details and exceptions, also see section 4.3.

3.1.5 Communication Protocol Selection

Both available protocols, I²C™ and OWI, can be active simultaneously, but only one interface can be used at a time.

An OWI communication access is also possible if OWI communication is enabled and analog output is active at the same time (i.e., during the startup window, in Diagnostic Mode, or in Command Mode after START_CYCx commands). For this, the active output AOUT must be overwritten by the communication master, so generating a stop condition before starting the communication is recommended to guarantee a defined start of communication (refer to Figure 3.9).

3.2 Digital Output

A read request is answered by transmitting data from the digital interface output registers.

During the continuous measurement cycle (NOM), digital output via the I²C™ interface sends the 15-bit bridge sensor value. The MSB carries the diagnostic status (ERR). Data validation is available by reading an additional check sum byte. The data is updated continuously when a new conditioned value is calculated.

Figure 3.1 I²C™ Read Request during Normal Operation Mode

Byte	Device Address		Bridge Sensor Signal			Validation	
			High Byte		Low Byte	High Byte	Low Byte
	Address	R/W	ERR	Bridge sensor signal (conditioned 15-bit value)		check sum	00_{HEX}
Value	78_{HEX}	1	0	MSB	LSB	MSB LSB	MSB LSB

During Diagnostic Mode (DM, see section 1.3.3), the diagnostic status bit (ERR) is set to “1.” An error code is also transmitted to identify the failure source.

Figure 3.2 I²C™ or OWI Read Request in Diagnostic Mode

Byte	Device Address		Bridge Sensor Signal			Validation	
			High Byte		Low Byte	High Byte	Low Byte
	Address	R/W	ERR	Error Code		check sum	00_{HEX}
Value	78_{HEX}	1	1	MSB	LSB	MSB LSB	MSB LSB

In Command Mode (CM) a 2-byte answer is generated for every received command. A 1-byte check sum is added followed by the command that is being answered. The check sum and the command echo allow verification of received data by the master. For details and exceptions, see section 4.3.

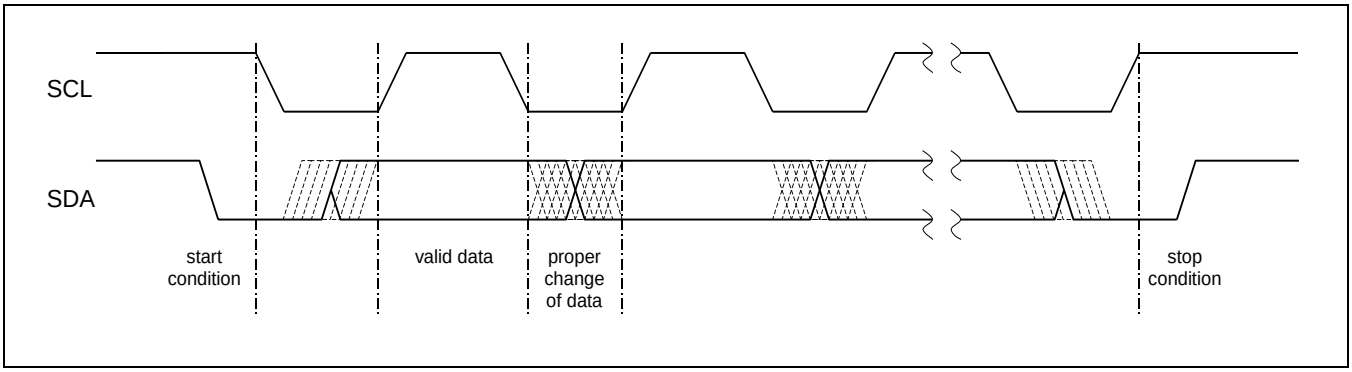
Figure 3.3 I²C™ or OWI Read Request Answering a Command (CM)

Byte	Device Address		Answer		Validation	
			High Byte	Low Byte	High Byte	Low Byte
	Address	R/W	Response (2 bytes)		check sum	Command Echo
Value	78_{HEX}	1	MSB	LSB	MSB LSB	MSB LSB

3.3 I²C™ Protocol

For I²C™ communication, a data line (SDA) and a clock line (SCL) are required.

Figure 3.4 Principles of I²C™ Protocol

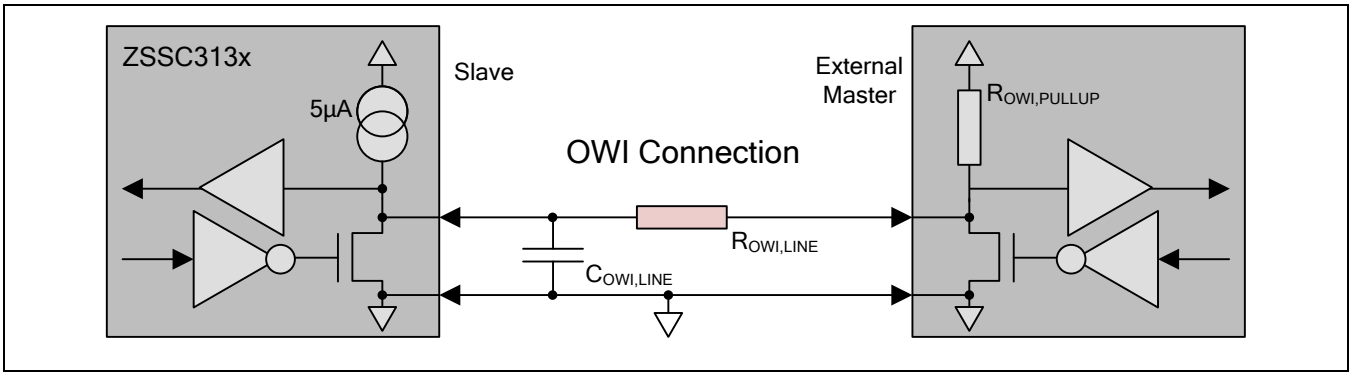


The I²C™ communication and protocol used are defined as follows:

- **Idle Period**
  When the bus is inactive, SDA and SCL are pulled-up to supply voltage V_{VDDA}.
- **Start Condition**
  A high-to-low transition on SDA while SCL is at the high level indicates a start condition. Every command must be initiated by a start condition sent by a master. A master can always generate a start condition.
- **Stop Condition**
  A low-to-high transition on SDA while SCL is at the high level indicates a stop condition. A command must be closed by a stop condition to start processing the ZSSC313x internal command routine. The ZSSC313x changes to inactive interface mode during processing.
- **Valid Data**
  Data is transmitted in bytes (8 bits) starting with the most significant bit (MSB). Each byte transmitted is followed by an acknowledge bit. Transmitted bits are valid if after a start condition, SDA maintains a constant level during a high period of SCL. The SDA level must change only when the clock signal at SCL is low.
- **Acknowledge**
  An acknowledge bit after a transmitted byte is required. The master must generate an acknowledge-related clock pulse. The receiver (slave or master) pulls-down the SDA line during the acknowledge clock pulse. If no acknowledge is generated by the receiver, a transmitting slave will remain inactive. A transmitting master can abort the transmission by generating a stop condition and can then repeat the command.

  A receiving master must signal the end of transfer to the transmitting slave by not generating an acknowledge bit and afterwards transmitting a stop condition.
- **Write Operation**
  During transmission from master to slave (WRITE), the device address byte is followed by a command byte and, depending on the transmitted command, up to 2 optional data bytes. The internal microcontroller evaluates the received command and processes the related routine.

Figure 3.8 Block Schematic of an OWI Connection



3.4.2 OWI Communication Access

OWI communication must be started when the ZSSC313x is enabled for reception. This depends on the configured OWI mode ADJREF:IFOWIM (see section 5.2). There are two OWI modes available with a startup window (nominal 52700 internal frequency clocks) after power-on and one continuous OWI communication mode. There is also a selectable mode in which OWI communication is completely disabled.

- **OWI communication continuously enabled (OWIENA)**
  OWI access remains always active at AOUT pin; the analog output is disabled. In Normal Operation Mode (NOM) the bridge sensor signal output can be readout with a cyclic read request. Command Mode (CM) can always be started by sending the command START_CM.
- **OWI startup window (OWIWIN)**
  OWI access is enabled during the startup window. The OWI master must send the START_CM command during the startup window to interrupt the start of analog output and to switch to CM.

  Analog voltage output starts if the startup window expires without receiving a valid START_CM command, and therefore OWI access is disabled. A cyclic readout of bridge sensor signal via OWI in NOM is not available.
- **OWI startup window with analog voltage output (OWIANA)**
  OWI access is enabled during the startup window. The analog voltage output starts immediately after power-on (maximum 5ms) simultaneously with the OWI startup window. For switching to CM, the OWI master must overwrite the active analog voltage output to send the START_CM command. This also ends the analog voltage output.

  OWI access is disabled if the startup window expires without receiving a valid START_CM command. A cyclic readout of the bridge sensor signal via OWI in NOM is not available.
- **OWI communication disabled (OWIDIS)**
  OWI access is not possible. In this mode, access to ZSSC313x is only available via the I^2C™ interface.

In Command Mode (CM), OWI communication is always possible. After certain commands requesting an analog output at the AOUT pin, the OWI master must overwrite the analog voltage output for further communication.

In Diagnostic Mode (DM), OWI communication is also possible. If the AOUT pin is driven to the Lower Diagnostic Range (LDR), again the OWI master must overwrite this voltage level for communication. Note that an unconfigured ZSSC313x with an invalid EEPROM signature always starts in DM.

3.4.3 OWI Protocol

OWI communication is always initiated by a master. Transmission starts with an address byte including a read/write bit to define the direction of the following byte transfer.

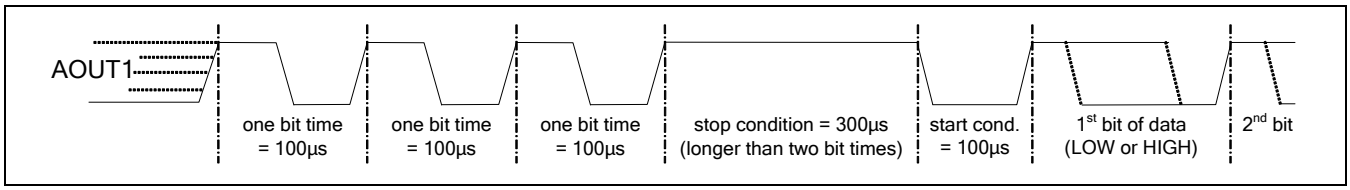
The OWI protocol is defined as follows:

- **Idle Period**
  During inactivity of the bus, the OWI communication line is pulled-up to supply voltage V_{VDDE} by an external resistor.
- **Start Condition**
  When the OWI communication line is in idle mode, a low pulse with a minimum width of 10µs* and then a return to high indicates a start condition. Every command must be initiated by a start condition sent by a master. A master can generate a start condition only when the OWI line is in idle mode.
- **Stop Condition**
  A constant level at the OWI line (no transition from low to high or from high to low) for at least twice the period of the last transmitted valid bit indicates a stop condition. Without considering the last bit-time (secure stop condition), a stop condition is generated with a constant level at the OWI line for at least 20ms.

  The master finishes a transmission by changing back to the high level (idle mode). Every command (see the subsequent “Write Operation” section) must be closed by a stop condition to start processing the command. The master must interrupt a sending slave after a data request (see the subsequent “Read Operation” section) by clamping the OWI line to the low level for generating a stop condition.

  In the case of an active analog voltage output at the AOUT pin, the output level must be overwritten by the OWI master. For example, this can occur if the OWI communication is started in the OWI startup window with a simultaneous analog voltage output. To ensure correct communication, first generate a stop condition (see Figure 3.9) before sending the first command (e.g., START_CM). After the ZSSC313x receives this first command, the analog output is disabled and OWI communication functions without sending additional sequences further on.

Figure 3.9 Example of OWI and Actively Driven AOUT – Starting OWI Communication with a Stop Condition



- **Valid Data**
  Data is transmitted in bytes (8 bits) starting with the most significant bit (MSB). Transmitted bits are recognized after a start condition at every transition from low to high at the OWI line. The value of the transmitted bit depends on the duty ratio between the high phase and high/low period (bit period $t_{OWI,BIT}$ in Figure 3.12). A duty ratio greater than 1/8 and less than 3/8 is detected as “0”; a duty ratio greater than 5/8 and less than 7/8 is detected as “1.” The bit period of consecutive bits must not change by more than a factor of 2 because the stop condition is detected in this case.

* 10µs is the minimum $t_{OWI,STA}$ that guarantees the OWI start condition in the range f_{OSC} = 2 to 4MHz.

4 Interface Commands

4.1 Command Set

All commands are available for I^2C™ and OWI communication, but only in Command Mode (CM). CM is initiated by sending the command START_CM $[72\ D1]_{HEX}$.

Every received command is answered. The answer consists of 2 bytes for the requested data or a validation code, 1-byte check sum, and 1-byte command echo. See Table 4.1 for exceptions (also refer to section 4.3).

EEPROM programming must be enabled by sending the EEP_WRITE_EN command $[6C\ F7\ 42]_{HEX}$.

During a running measurement cycle in NOM or in CM after START_CYCx and START_ADx commands, it is mandatory to abort the measurement cycle before transmitting the next command. For safe communication, it is recommended that further communication starts with a repetition of the START_CM command. This does not apply to the read operations for getting measured values.

Table 4.1 Command Set

Note: See table notes at the end of the table. See Table 4.2 for a summary of responses to commands.

Command (HEX)	Data	Command	Comments	Processing Time @ f_{OSC}=3MHz
01		START_CYC_EEPOWI	Start measurement cycle including initialization from EEPROM. OWI mode OWIENA is activated (refer to Table 5.5).	350µs
02		START_CYC_RAMOWI	Start measurement cycle including initialization from RAM. OWI mode OWIENA is activated (refer to Table 5.5).	220µs
03		START_CYC_EEPANA	Start measurement cycle including initialization from EEPROM. OWI mode OWIANA is activated (refer to Table 5.5).	350µs
04		START_CYC_RAMANA	Start measurement cycle including initialization from RAM. OWI mode OWIANA is activated (refer to Table 5.5).	220µs
05		START_CYC_EEPOWIDIS	Start measurement cycle including initialization from EEPROM. OWI mode OWIDIS is activated (refer to Table 5.5).	350µs
06		START_CYC_RAMOWIDIS	Start measurement cycle including initialization from RAM. OWI mode OWIDIS is activated (refer to Table 5.5).	220µs
07		START_CYC_EEP	Start measurement cycle including initialization from EEPROM.	350µs
08		START_CYC_RAM	Start measurement cycle including initialization from RAM.	220µs
10 to 1E		READ_RAM	Read data from RAM addresses 00_{HEX} through $0E_{HEX}$.	50µs

Command (H E X)	Data	Command	Comments	Processing Time @ f_{OSC}=3MHz
30 to 43		READ_EEP	Read data from EEPROM addresses 00_{HEX} through 13_{HEX}.	50µs
50		ADJ_OSC_ACQ	Use this command with OWI communication only! Acquire frequency ratio (f_{OSC} / f_{OWI}) where f_{OSC} is the frequency of internal oscillator f_{OWI} is the OWI communication frequency Use this for adjusting the internal oscillator frequency via ADJREF:OSCADJ (see section 4.4.3).	50µs
60	2 bytes	SET_DAC	Set analog output AOUT to value defined by data bytes. Important note: If the data byte is outside the allowed range of 0100_{HEX} to $14FF_{HEX}$, the IC will enter DM and output the LDR (Lower Diagnostic Range). See section 2.6. The AOUT pin goes into tri-state during processing of the command.	40µs
61	2 bytes	START_AD_CNT	Process <n> times A/D conversion for bridge sensor signals and for calibration temperature including auto-zero compensation (see section 4.4.2). data[15:0] is number <n> of measurements to process. Digital Low-Pass Filter averaging coefficient LPFAVRG from RAM is applied. Returns most recent two result values (Bridge, Calibration Temperature) while processing measurement. Last values remain if measurement is finished. See section 4.4.2 for details.	100µs + (4∗n) ∗ A/D conversion time
62	2 bytes	START_AD_CNT_AVRG	Process <n> times A/D conversion for bridge sensor signals and for calibration temperature including auto-zero compensation (see section 4.4.2). data[15:3] is number <n> of measurements to process. data[2:0] is digital Low-Pass Filter averaging coefficient with range [0; 7]. Note that data[2:0] changes LPFAVRG in RAM. Returns most recent two result values (Bridge, Calibration Temperature) while processing measurement. Last values remain if measurement is finished. See section 4.4.2 for details.	100µs + (4∗n) ∗ A/D conversion time
65	2 bytes	ADJ_OSC_WRI	Write to RAM and activate Oscillator Adjust value ADJREF:OSCADJ. Returns complete new configuration word ADJREF.	50µs

Command (HEX)	Data	Command	Comments	Processing Time @ f_{OSC}=3MHz
6C	2 bytes	EEP_WRITE_EN	Enable data write to EEPROM. To be sent with data $F742_{HEX}$. Other data disables EEPROM write. Returns $C36C_{HEX}$ if EEPROM programming is enabled. Returns $CF6C_{HEX}$ if EEPROM programming is disabled.	50µs
72	1 byte	START_CM	Start Command Mode (CM). To be sent with data $D1_{HEX}$. Returns $C372_{HEX}$ if CM is enabled. Returns Error code if sent during Diagnostic Mode (DM).	50µs
80 to 8E	2 bytes	WRITE_RAM	Write data to RAM addresses 00_{HEX} through $0E_{HEX}$.	50µs
A0 to B2	2 bytes	WRITE_EEP	Write data to EEPROM addresses 00_{HEX} through 12_{HEX}. Note that there is no write access to IDT word at address 13_{HEX}. Returns $CF00_{HEX}$ if EEPROM programming is disabled.	12.5ms
C0		COPY_EEP2RAM	Copy content of EEPROM address 00_{HEX} through $0E_{HEX}$ to RAM. Restores EEPROM configuration in RAM. Does not process EEPROM signature check. Returns $C3C0_{HEX}$ if command is processed.	130µs
C3		COPY_RAM2EEP	Copy content of RAM address 00_{HEX} through $0E_{HEX}$ to EEPROM. Generates EEPROM signature, writes it to address F_{HEX}. Returns $C3C3_{HEX}$ if copy is successfully processed. Returns $CFC3_{HEX}$ if copy failed. Returns $CF00_{HEX}$ if EEPROM programming is disabled.	200ms
C7		REFRESH_EEP	Refreshes content of EEPROM addresses 00_{HEX} through 13_{HEX}. Detected 1-bit errors are corrected. If multi-bit error is detected, refresh is not processed. Returns $C3C7_{HEX}$ if refresh is successfully processed. Returns $CFC7_{HEX}$ if refresh failed. Returns $CF00_{HEX}$ if EEPROM programming is disabled. Refresh must be done by user if a wafer product (not assembled tested dice) is used.	200ms
C8		GET_EEP_SIGN	Calculate and return EEPROM signature.	150µs
C9		GEN_EEP_SIGN	Calculate and return EEPROM signature and write it to EPROM address $0F_{HEX}$. Returns $CF00_{HEX}$ if EEPROM programming is disabled.	12.6ms
CA		GET_RAM_SIGN	Calculate and return RAM signature.	150µs

4.3 Digital Output Data in Command Mode

Digital output data in CM consists of two 16-bit words that can be read by an I²C™ or OWI read request. Content of data words depends on the previously received command.

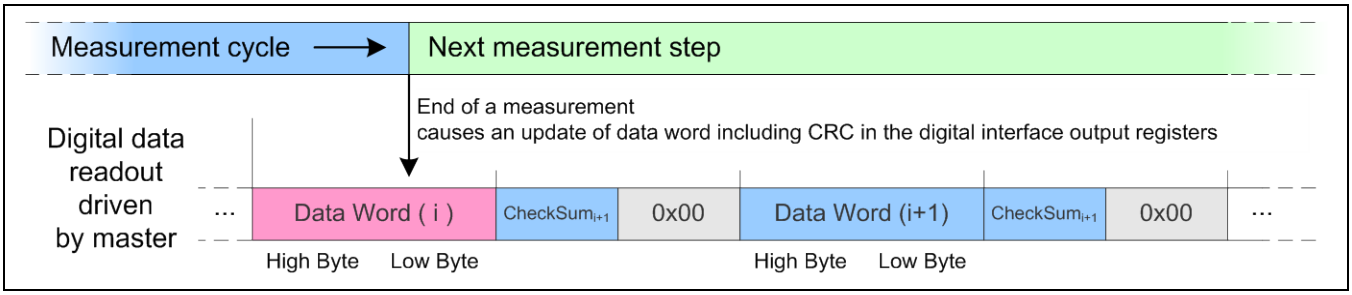
Table 4.2 Digital Output Data Resulting from Processed Commands

Mode/ Commands	Output Data Word 1		Output Data Word 2	
	High Byte	Low Byte	High Byte	Low Byte
Commands with data response	Requested data		check sum	Processed command
Commands without data response	Success code [C3 command]$_{HEX}$		check sum	Processed command
	Reject code [CF command]$_{HEX}$			
Unknown commands	Reject code [CF 00]$_{HEX}$		check sum	Received command
Command processing error	Reject code [C0 00]$_{HEX}$		check sum	Received command
START_CYC_x [01]$_{HEX}$, [02]$_{HEX}$ [03]$_{HEX}$, [04]$_{HEX}$ [05]$_{HEX}$, [06]$_{HEX}$ [07]$_{HEX}$, [08]$_{HEX}$	15-bit conditioned value, error status (NOM) *or* Error code (DM) (refer to section 3.2)		check sum	00$_{HEX}$
START_AD_CNT [61]$_{HEX}$ START_AD_CNT_AVRG [62]$_{HEX}$	Measured raw Bridge sensor value		Measured raw Calibration Temperature value	

The check sum is calculated with following formula: check sum = FF_{HEX} – ($HighByte_{1st\_word}$ + $LowByte_{1st\_word}$)$_{8LSB}$.

During running measurement cycle in NOM or in CM after START_CYC_x or START_AD_x commands, an apparent check sum mismatch can occur. The digital output data, including the check sum, are updated continuously processing these commands. If an update of data is processed during readout of a 16-bit data word, the subsequent readout delivers the new but mismatched check sum. The data word belonging to that new check sum would be read if the master proceeded to read an additional data word. This might allow a check sum protection algorithm. Nevertheless, if the measurement cycle is faster than the digital readout data rate, a check sum evaluation is not applicable.

Figure 4.1 Assignment of Check Sum for Continuously Updated Data Values

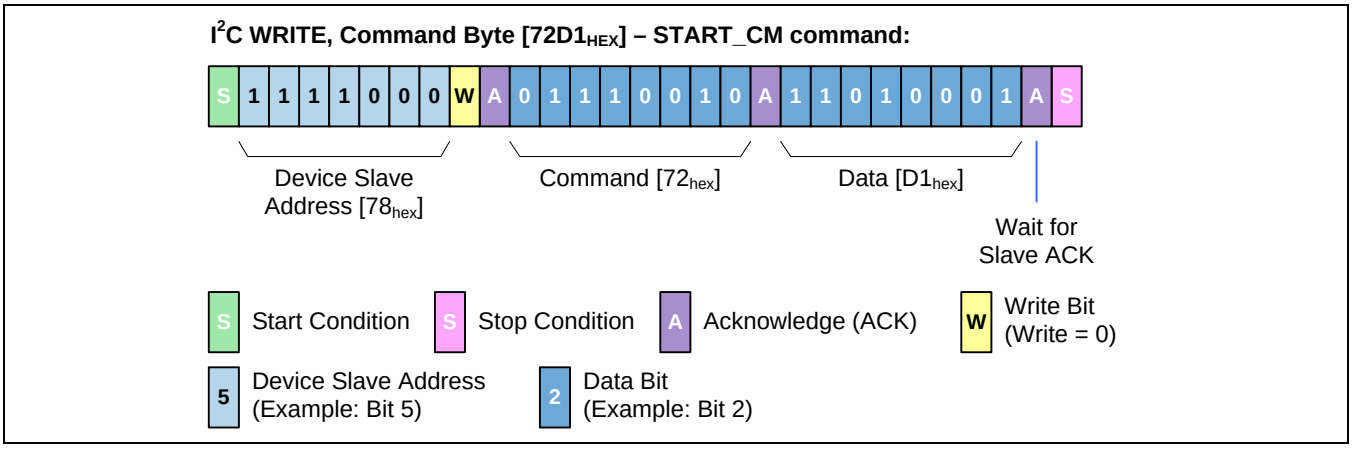


4.4 Detailed Description for Particular Commands

4.4.1 Start Command Mode with START_CM [72 D1]$_{HEX}$

Starting the Command Mode from Normal Operation Mode or Diagnostic Mode requires transmitting the START_CM command via I^{2}C™ or OWI as shown in Figure 4.2.

Figure 4.2 START_CM Command



The START_CM command should also be used to stop the measurement cycle after the START_CYC_x command [0x]$_{HEX}$ or after START_AD commands [Dx]$_{HEX}$. Recommendation: For secure operation, send the START_CM command twice and check success by reading the success code C372$_{HEX}$. Under specific ZSSC313x internal conditions, it is possible that an IC does not answer to its assigned unique slave address. In this case, use the general call address to restart communication access.

4.4.2 Acquisition of Raw Measurement Data with Commands START_AD_CNT [61]$_{HEX}$ and START_AD_CNT_AVRG [62]$_{HEX}$

The START_AD_CNT [61]$_{HEX}$ and START_AD_CNT_AVRG [62]$_{HEX}$ commands are used for synchronized raw data acquisition during the calibration process (snapshot mode). Bridge sensor signal and calibration temperature values are captured concurrently. Especially for mass calibration, it enables a raw data snapshot for all attached devices under temperature drift and pressure leakage conditions.

The START_AD_CNT command [61]$_{HEX}$ transmits two data bytes containing the A/D conversion cycle count to be processed.

The START_AD_CNT_AVRG command [62]$_{HEX}$ transmits two data bytes containing the following parameters:

data[15:3] is the A/D conversion cycle count to be processed.

data[2:0] is the digital Low-Pass Filter averaging coefficient AVRG for all measured values.
Note that this overwrites the filter coefficient LPFAVRG in RAM.

Data acquisition is low-pass filtered as shown in equation (18):

$$X_{OUT,i} = X_{OUT,i-1} + \frac{\left(X_i - X_{OUT,i-1}\right)}{2^{AVRG}} \qquad i > 0, \quad AVRG \in [0;7) \tag{18}$$

The recommended value for the requested conversion cycle count is at least (2^{AVRG} + 8).

A/D conversion is done cyclically over both input channels including auto-zero. While measuring, the most recent result values can be read out by read request. No analog output is generated. OWI communication remains enabled during the measurement cycle. When finishing the A/D conversion cycles, the read request delivers final filtered result values for the measured bridge sensor signal and calibration temperature (refer to Table 4.2).

4.4.3 Oscillator Frequency Adjustment with ADJ_OSC_ACQ [50_{HEX}] and ADJ_OSC_WRI [65 data]$_{HEX}$

ADJ_OSC_x commands are used to adjust the frequency of the internal oscillator. This frequency is adjustable in the range of 2MHz to 4MHz. It has a directly proportional effect on the A/D conversion time. The internal oscillator frequency can be adjusted by ADJREF:OSCADJ. The frequency is adjusted by steps with one step equal to approximately -125kHz (frequency is decreased if ADJREF:OSCADJ is increased).

The ADJ_OSC_ACQ command is sent first. This command is valid ONLY with one-wire communication (OWI). It returns a value that represents the ratio f_{OSC}/f_{OWI} of the internal oscillator frequency to the communication frequency. This frequency ratio can be read with an I²C™ or OWI Read Request.

The communication frequency f_{OWI} is known, so the current internal oscillator frequency f_{OSC} can be calculated. Note that the resolution of the frequency measurement is better when a lower OWI communication frequency is used.

The required adjustment of ADJREF:OSCADJ to reach the target frequency can be calculated from the ratio f_{OSC}/f_{OWI} and the adjustment increment of -125kHz/step. The ADJ_OSC_WRI command is used to write ADJREF:OSCADJ to RAM and to activate the new adjustment. The command returns the complete configuration word ADJREF (all other configuration bits retain their value).

This sequence allows an easy and accurate adjustment of the internal frequency during end-of-line calibration.

Table 4.3 Oscillator Frequency Adjust Sequence

Command [HEX]	Data [HEX]	Description	Steps
72	D1	START_CM	Start Command Mode using OWI interface
50	-	ADJ_OSC_ACQ	Acquire frequency ratio and convert to decimal
READ	-	2 bytes	Calculate the frequency: $f_{OSC} = f_{OWI} * f_{RATIO}$ [MHz] and correction steps and convert to HEX: $\text{Steps} = \frac{f_{OSC} - f_{TARGET}}{125kHz} \text{Steps} = \frac{f_{OSC} - f_{TARGET}}{125kHz} = \frac{3.838MHz - 2.6MHz}{125kHz} = 9.9 \approx 10_{DEC} = A_{HEX}$
3D	-	Read EEPROM	Read the ADJREF register to determine the present OSCADJ settings (bits 0:4)
READ	-	4 bytes	$OSCADJ_{NEW}$ = OSCADJ + Steps
65	ADJREF	ADJ_OSC_WRI	Write to RAM and activate the new ADJREF register content.

5 EEPROM and RAM

5.1 Programming the EEPROM

Programming the EEPROM is done using an internal charge pump to generate the required programming voltage. The timing of the programming pulses is controlled internally. The programming time for a write operation is typically 12.5ms independent of the programmed clock frequency (ADJREF:OSCADJ). Waiting a minimum of 15ms per write operation before starting the next communication is recommended.

To program the EEPROM, the ZSSC313x must be set to Command Mode by the command START_CM $[72\ D1]_{HEX}$ and EEPROM programming must be enabled by the command EEP_WRITE_EN $[6C\ F7\ 42]_{HEX}$. Writing data to the EEPROM is done via the serial digital interface by sending specific commands (refer to section 4.1).

The WRITE_EEP command includes the address of the targeted EEPROM word and is followed by two data bytes. During EEPROM programming, the serial digital interface is disabled and no further commands can be recognized.

The COPY_RAM2EEP command writes the contents of the RAM mirror area to the EEPROM. This is to simplify the calibration process when the ZSSC313x is configured iteratively. The EEPROM signature, which is not mirrored in RAM, is generated, written to EEPROM, and returned to the interface output register. This copy operation includes 16 EEPROM write operations and therefore typically requires 200ms (recommended wait time 250ms).

The REFRESH_EEP command is available to refresh EEPROM content during calibration process. Particularly if unassembled tested dice (wafer product) are utilized, this refresh is mandatory to ensure proper function of EEPROM and data consistency for stored traceability data.

5.2 EEPROM and RAM Contents

The configuration of the ZSSC313x is stored in 20 EEPROM 16-bit words.

Calibration coefficients for conditioning the sensor signal via conditioning calculations and output limits are stored in 11 words. There are three words for setting the configuration of the ZSSC313x for the application. One register is used for storing the EEPROM signature, which is used in NOM to check the validity of the EEPROM contents after power-on. Three additional 16-bit words are available for optional user data.

After every power-on, the EEPROM contents are mirrored to RAM. After this read out, the contents of the RAM mirror are checked by calculating the signature and comparing it to the one stored in EEPROM. If a signature error is detected, the ZSSC313x changes to steady Diagnostic Mode (DM). DM is indicated by setting both analog outputs AOUT to the Lower Diagnostic Range (LDR). Subsequently the error code can be read out via I^2C™ or OWI.

The configuration of the device is done from the mirrored area in RAM, so the configuration words are subsequently transferred to the internal registers. The calibration coefficients for the conditioning calculations are also read from RAM. As a result, every change to the RAM mirror area impacts the configuration and behavior of the device after the next start of the measurement cycle.

After power-on, the contents of the RAM mirror area are determined by the EEPROM contents and can then be changed by specific commands writing to RAM. This new configuration can be activated by the START_CYC_RAMx commands or by the START_AD_x commands.

RAM/EEPROM Address	RAM/EEPROM Write Command	Default Configuration	Description Note: The MSB is given first if an address has more than one assignment.
Free Memory Available for Optional Use by User Applications (not included in signature)			
10_{HEX} (16)	- / $B0_{HEX}$	0000_{HEX}	Free user memory, not included in signature
11_{HEX} (17)	- / $B1_{HEX}$	0000_{HEX}	Free user memory, not included in signature
12_{HEX} (18)	- / $B2_{HEX}$	0000_{HEX}	Free user memory, not included in signature
13_{HEX} (19)	-/-		No customer access - IDT restricted use

Note: The contents of the EEPROM registers at delivery are not specified and can be subject to changes. Particularly with regard to traceability, the contents can be unique per die. Note that contents at delivery might not have a valid signature. Consequently the ZSSC313x would start in the Diagnostic Mode.

Note: All registers must be rewritten during the calibration procedure.

5.2.1 Traceabilty

IDT can guarantee the EEPROM contents for packaged parts only. On delivery of bare dice, the EEPROM content might be changed by flipped bits due to electrostatic effects, which could occur during the wafer sawing.

The ZSSC313X features three 16-bit registers reserved for user data: 10_{HEX}, 11_{HEX}, and 12_{HEX}. For example, these can be used for an ID number. There are no restrictions for the content of these registers; they can be read via I^2C™ at any time.

When using ZACwire™ communication (OWI),

- READ is possible if ZACwire™ communication is enabled.
- WRITE is possible if the EEPROM lock is disabled.
- WRITE is possible if an EEPROM error (wrong signature or multi-bit error) is detected.

During final test, IDT writes the following manufacturing data to these registers:

- **Register 10_{HEX}:** bits 15:0 = lot number part 1 (MSB section)
- **Register 11_{HEX}:** bits 15:5 = lot number part 2 (LSB section) / bits 4:0 = wafer number
- **Register 12_{HEX}** bits 15:8 = wafer x-position / bits 7:0 = wafer y-position

Table 5.2 Lot, Wafer, x-Position, and y-Position Number Calculation Procedure

```
temp      = reg0x10 * 2048 + (reg0x11&0xFFE0)/32;
lotNbr    = NumberConvert(temp, BASE); // BASE = 36
waferNbr  = reg0x11&0x1F;
xpos      = reg0x12&0xFF00)/256;
ypos      = reg0x12&0x00FF;
```

IDT recommends saving these data in the calibration log to identify the device in the event that RMA processing is needed.

Register 13_{HEX} is used by IDT to store logistic data and internal information. It can be written by IDT via test equipment only; the user cannot write data to this register.

5.2.2 EEPROM Error Correction

The EEPROM data are stored with HAMMING DISTANCE = 3, which means

- 100% detection and correction of 1-bit errors
- 100% detection of 2-bit errors

The detection of multi-bit errors (>2 bit) is processed at a lower detection rate.

5.3 Configuration Words

The data stored in EEPROM at addresses B_{HEX} to E_{HEX} determine the configuration of the ZSSC313x, as explained in the following tables.

Table 5.3 Configuration Word CFGAFE

Bit	CFGAFE - Configuration of Analog Front-End EEPROM/RAM Address B_{HEX} (11)	
15	*ZSSC3138* **BR**idge sensor channel e**X**tended **Z**ero **C**ompensation **POL**arity (offset compensation by analog front-end—refer to section 2.1) 0: negative – compensates positive offsets 1: positive – compensates negative offsets (Set 0 for ZSSC3131, 3135 and 3136.)	BRXZCPOL
14:10	*ZSSC3138* **BR**idge sensor channel e**X**tended **Z**ero **C**ompensation value (offset compensation by analog front-end—refer to section 2.1) Offset compensation is only active, if BRXZC ≠ 0 The offset compensation step depends on the selected input span. (Set to 0 for ZSSC3131, ZSSC3135, and ZSSC3136.)	BRXZC
9:6	**BR**idge sensor channel **GAIN** (a_{IN} - refer to section 2.1) 0100_{BIN}: 105 0111_{BIN}: 35 1010_{BIN}: 9.3 0101_{BIN}: 70 1000_{BIN}: 26.25 1011_{BIN}: 7 0110_{BIN}: 52.5 1001_{BIN}: 14 $11dd_{BIN}$: 2.8 *ZSSC3138* High Gain Mode: 0000_{BIN}: 420 0001_{BIN}: 280 0010_{BIN}: 210 0011_{BIN}: 140	BRGAIN
5	**A/D C**onversion **SLOW** mode Doubles A/D conversion time to improve conversion result quality (less noise, better linearity). Valid for all measurements. 0: disabled 1: enabled	ADCSLOW
4:3	**A/D C**onversion input **R**ange **S**hift (rs_{ADC} – refer to section 2.1) 00_{BIN}: $^1/_{16}$ → ADC range = [(–1/16 V_{ADC_REF}) to (+15/16 V_{ADC_REF})] 01_{BIN}: $^1/_8$ → ADC range = [(–1/8 V_{ADC_REF}) to (+7/8 V_{ADC_REF})] 10_{BIN}: ¼ → ADC range = [(–1/4 V_{ADC_REF}) to (+3/4 V_{ADC_REF})] 11_{BIN}: ½ → ADC range = [(–1/2 V_{ADC_REF}) to (+1/2 V_{ADC_REF})]	ADCRS

Bit	CFGAFE - Configuration of Analog Front-End EEPROM/RAM Address B_{HEX} (11)	
2:1	**A/D C**onversion **RES**olution (r_{ADC} - refer to section 2.1) Valid for bridge signal as well as for temperature measurement. 00_{BIN}: 13bit 01_{BIN}: 14bit *ZSSC3138* Digital Value Range Zooming (refer to section 2.2): 10_{BIN}: 15bit 11_{BIN}: 16bit If 15bit or 16bit are activated use CFGAPP:BROFFS to select segment to be used for bridge sensor signal. Conditioning calculation is done with zoomed 13bit or 14bit value, respectively (refer to section 2.2).	ADCRES
0	*ZSSC3138* High Sample Rate Mode (**AD C**onversion **ORD**er) 0: disabled (1-step conversion) 1: enabled (2-step conversion) *Note: Set to 0 for ZSSC3131, ZSSC3135, and ZSSC3136.*	ADCORD

Table 5.4 Configuration Word CFGAPP

Bit	CFGAPP - Configuration of Target Application EEPROM/RAM Address C_{HEX} (12)	
15:13	*ZSSC3138* Digital Value Range Zooming Offset (refer to section 2.2): Digital offset to raw bridge sensor value. *Note: Set to 000_{BIN} for ZSSC3131, ZSSC3135, and ZSSC3136.*	BROFFS
12	Count of Bridge Sensor measurements per special measurement in measurement cycle loop 0: 1 Bridge Sensor signal and 1 special measurement 1: 30 Bridge Sensor signal and 1 special measurement	BRCNT
11	*ZSSC3136* ROM check at power-on Start-up is increased approx. 10ms. 0: disabled 1: enabled	CHKROM
10	*ZSSC3135, ZSSC3136, ZSSC3138 only*: enable lower Sensor Short Check limit 0: limit = 1750 counts 1: limit = 1500 counts *Note: Set to 0 for ZSSC3131.*	CHKSSCL
9	*ZSSC3135, ZSSC3136, ZSSC3138* Sensor Connection and Short Check 0: disabled 1: enabled *Note: Set to 0 for ZSSC3131.*	CHKSENS
8	ZSSC3135, ZSSC3136, ZSSC3138 Temperature Sensor Check 0: disabled 1: enabled *Note: Set to 0 for ZSSC3131.*	CHKTS
7:6	**T**emperature measurement **GAIN** (refer to section 6): 00_{BIN}: 2.66 01_{BIN}: 4.0 10_{BIN}: 6.6 11_{BIN}: 7.33	TGAIN

Bit	CFGAPP - Configuration of Target Application EEPROM/RAM Address C_{HEX} (12)	
5:4	**T**emperature **M**easurement **M**ode 01_{BIN}: internal on-chip diode – correlated with zero point at ADJREF:TOFFS = 0 11_{BIN}: internal on-chip diode – correlated with zero point at ADJREF:TOFFS = 2 *ZSSC3135 and ZSSC3136 External Temperature Sensor* 00_{BIN}: external diode at pin IRTEMP 10_{BIN}: external voltage at pin IRTEMP	TMM
3	**C**o**N**ne**CT SENS**or internally to supply voltage VBR_T is connected to VDDA and VBR_B is connected to VSSA 0: disconnected 1: connected	CNCTSENS
2	*Reserved. Set to 0.*	-
1	A/D conversion **REF**erence voltage for Bridge Sensor signal (V_{ADC_REF} - refer to section 2.1) 0: $V_{ADC\_REF} = V_{VBR\_T} – V_{VBR\_B}$ 1: $V_{ADC\_REF} = V_{VDDA} – V_{VSSA}$	BRREF
0	**BR**idge Sensor **POL**arity (V_{IN_DIFF} - refer to section 2.1) 0: positive ($V_{IN\_DIFF} = V_{VBP} – V_{VBN}$) 1: negative ($V_{IN\_DIFF} = V_{VBN} – V_{VBP}$)	BRPOL

Table 5.5 Configuration Word ADJREF

Bit	ADJREF – Adjustment of Internal References EEPROM/RAM Address D_{HEX} (13)				
15:14	One-Wire Interface Mode (refer to section 3.4 for details)				IFOWIM
	IFOWIM	OWI Mode	Pin AOUT		
			OWI	Analog Output	
	00	OWIWIN	Start-up window	After start-up window	
	01	OWIANA	Start-up window	Enabled	
	10	OWIENA	Enabled	Disabled	
	11	OWIDIS	Disabled	Enabled	
13:10	Unique slave address for I^2C™ and OWI. address = 70_{HEX} + IFADDR Resulting address range is 70_{HEX} to $7F_{HEX}$. General address 78_{HEX} is always valid.				IFADDR
9	Enables triggering a reset if the Diagnostic Mode (DM) occurs 0: stop and DM 1: reset and startup Reset is executed after time-out of watchdog.				DMRES
8:6	Adjust zero point of temperature measurement				TOFFS
5	Enables bias current boost for analog front-end 0: disabled 1: enabled Activation is recommended for oscillator frequency > 3MHz.				BBOOST
4:0	Adjustment of internal oscillator frequency f_{OSC}, in the range of 2 to 4MHz				OSCADJ