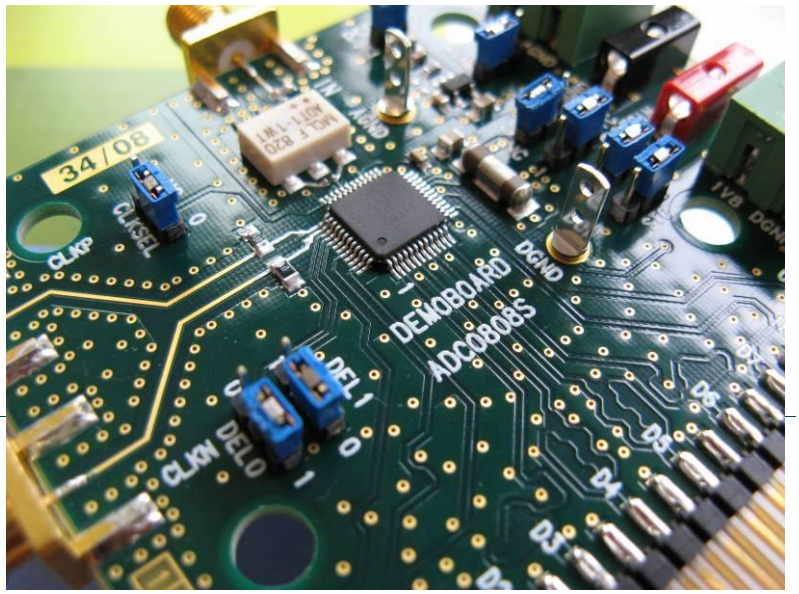
Quick Start

Demonstration Board for ADC0808S

Rev. 2.0 — 2 July 2012 **Quick Start**

Document information

Info	Content
Keywords	PCB2050-1, Demonstration board, ADC, Converter, ADC0808S
Abstract	This document describes how to use the demonstration board for the analog-to-digital converter ADC0808S.
Overview	



Revision history

Rev	Date	Description
2.0	20120702	Rebranded.
0.1	20081006	Initial version.

1. Quick start

1.1 Setup overview

Figure Fig 1 presents the connections to measure ADC0808S.

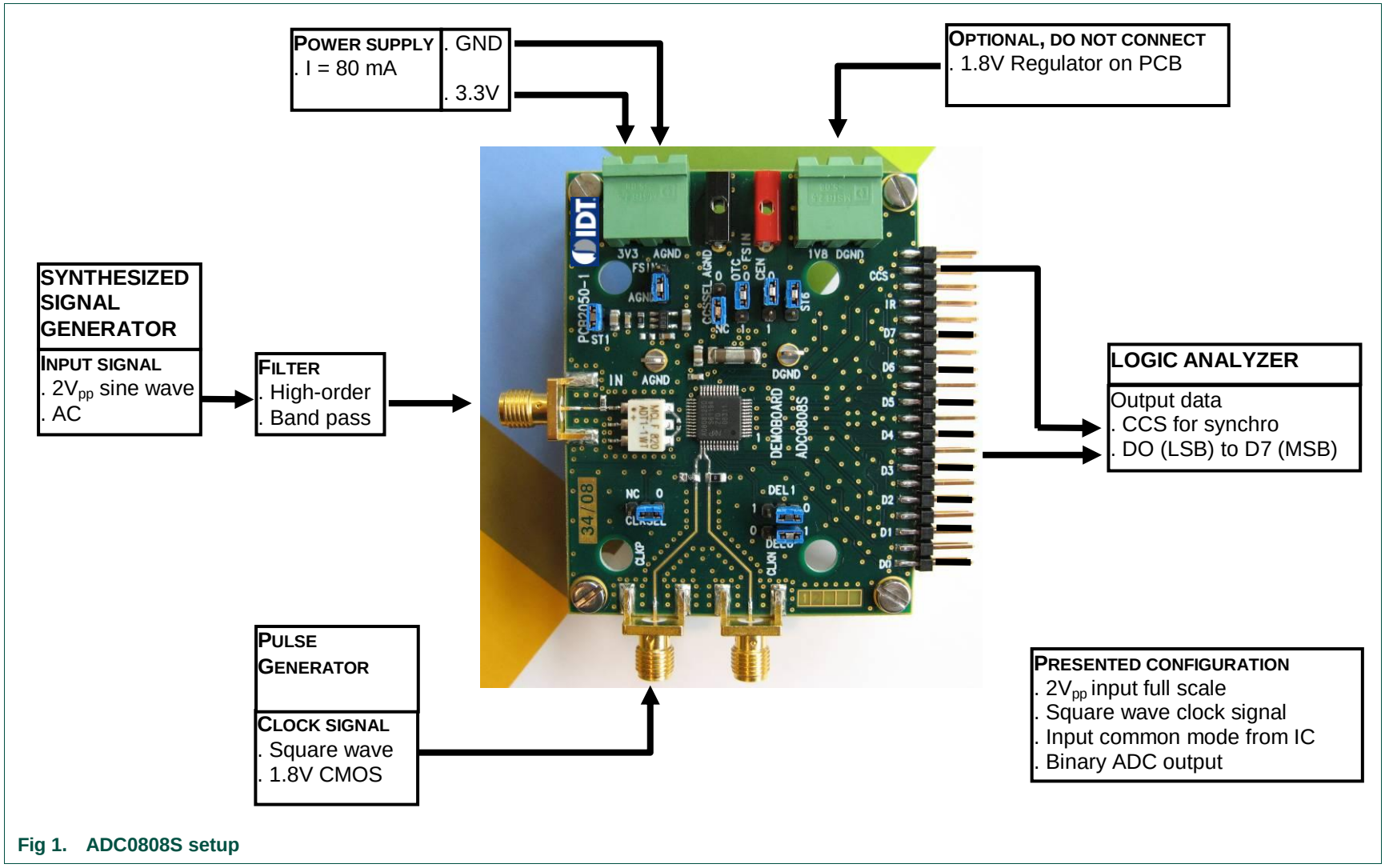
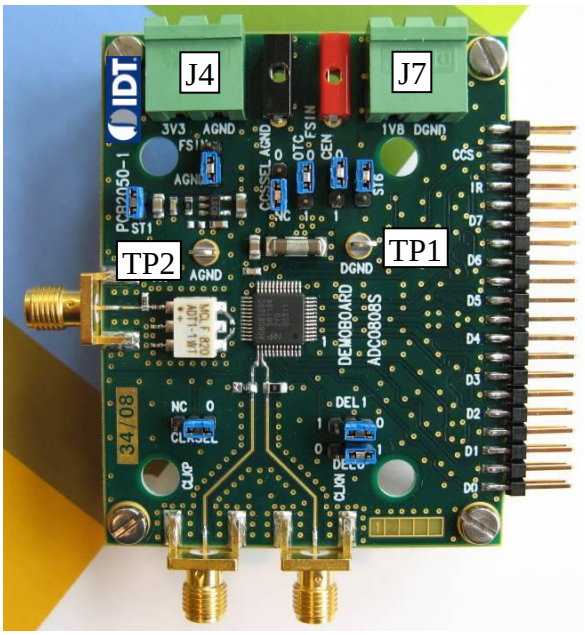


Fig 1. ADC0808S setup

1.2 Power supply

The board is powered with a single 3.3 V_{DC} power supply. A power supply regulator is used to supply all the circuitry on the board.

Table 1. General power supply

Name	Function	View
J4	+3.3V green connector – Power supply 3.3 V_{DC} / 100 mA.	
J7	Do not connect, optional. Internal 1.8V regulator. +1.8V green connector – Power supply 1.8 V_{DC} / 50 mA	
TP1	DGND test point – Digital ground	
TP2	AGND test point – Analog ground	

1.3 Input signals (IN, CLK)

The ADC0808S clock inputs are selectable between 1.8 V Complementary Metal Oxide Semiconductor (CMOS) or Low-Voltage Differential Signals (LVDS).

To ensure a good evaluation of the device, the input signal and the input clock must be synchronized together.

Moreover, the input frequency (Fi, MHz) and the clock frequency (Fclk, Msps) should follow the formula:

$$\frac{Fi}{Fclk} = \frac{M}{N}$$

,where M is an odd number of period and N is the number of samples.

Table 2. Input signals, CMOS Clock

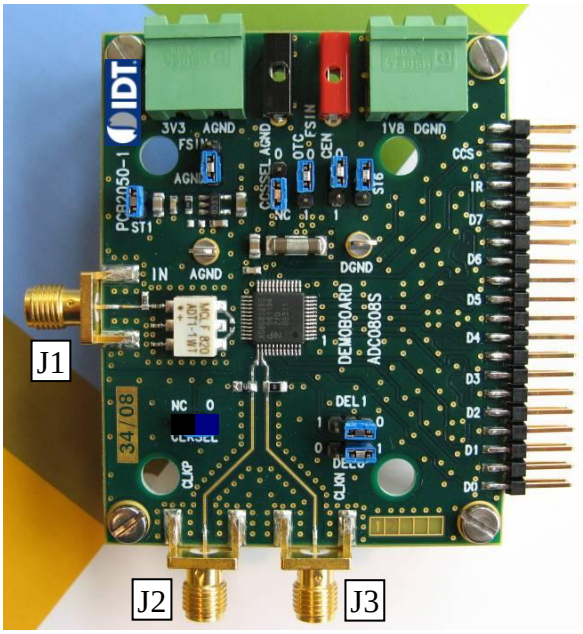
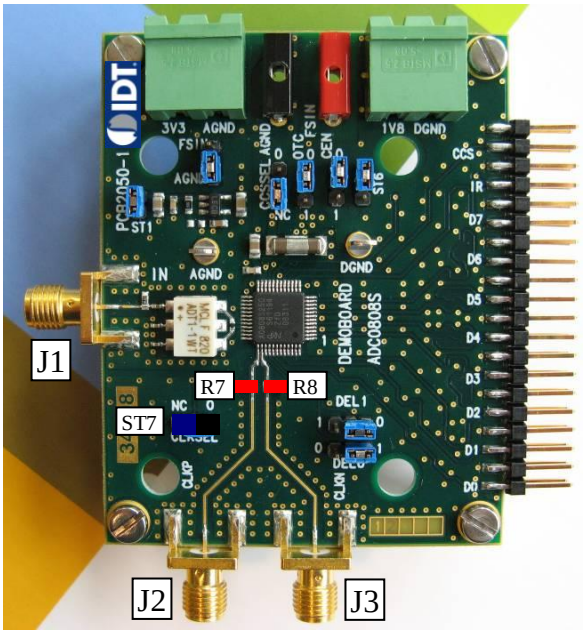
Name	Function	View
J1	IN connector – Analog input signal (50Ω matching)	
J2	CLKP connector – Single ended 1.8V CMOS clock input signal	
J3	CLKN connector – Grounded on that demo board	
ST7	Clock input format selection. 0: 1.8V CMOS	

Table 3. Input signals, LVDS Clock

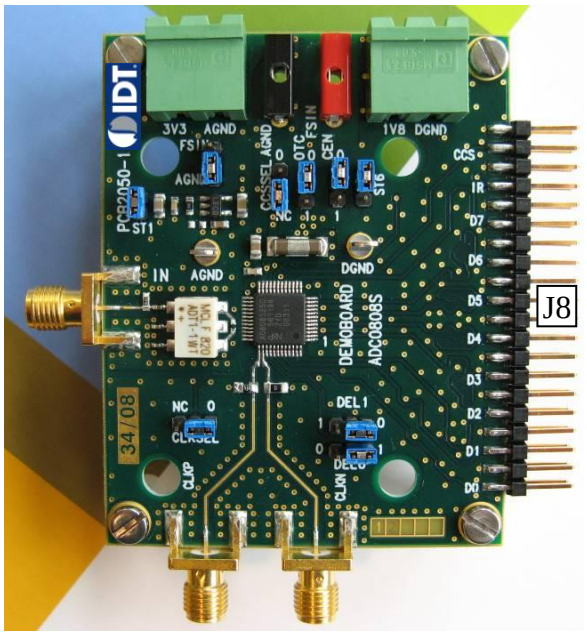
Name	Function	View
J1	IN connector – Analog input signal (50Ω matching)	
J2	CLKP connector – LVDS Clock input, 50 ohms must be soldered on R7 footprint.	
J3	CLKN connector – LVDS complementary Clock input, 50 ohms must be soldered on R8 footprint.	
ST7	Clock input format selection. NC: LVDS	

1.4 Output signals (D0 to D7, IR, CCS)

The digital output signal is available in binary, 2's complement.

A Complete Conversion Signal output (CCS) is provided by the device for the data acquisition.

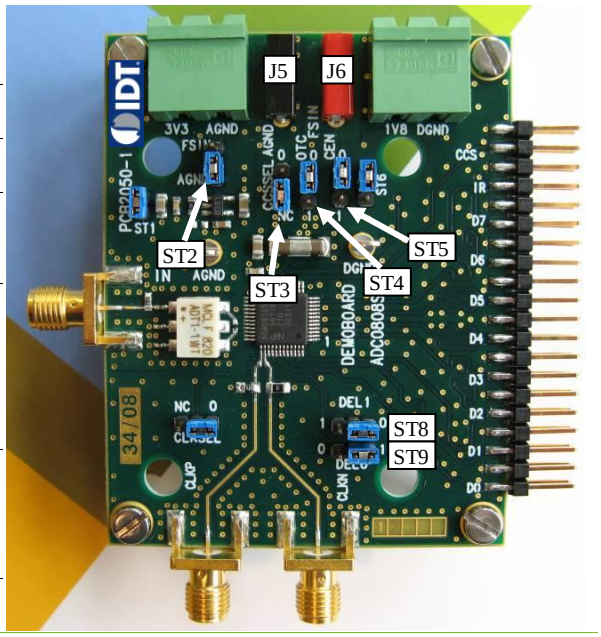
Table 4. **Output signals**

Name	Function	View
J8	Array connector – ADC digital output(D0 to D7), In Range output (IR) and Complete Conversion Signal (CCS)	

1.5 Configuration

The ADC0808S reference, output coding, timing and frequency of complete conversion signal can be adjusted thanks to PCB jumpers.

Table 5. **Configuration**

Name	Function	View
ST2	AGND: Internal reference selected FSIN: External reference from J5 and J6	
J5	External reference ground	
J6	External reference voltage	
ST3	NC: CCS output is at F_{clk} frequency 0: CCS output is at F_{clk}/2 frequency	
ST4 & ST5	Output format selection: OTC and CEN 00: binary 10: 2's complement X1: High impedance	
ST4 & ST5	Delay control of CCS edge, see datasheet.	

Notes