RC32434 Design Guide

Notes

This document is intended to reflect some of the design considerations that need to be applied when designing a system based on the RC32434. This document is intended to record subtle behaviors of the RC32434 that should be considered early in the design process to avoid lengthy debug time.

Document Revision History

November 17, 2003: Initial publication.

Hardware Recommendations

Board Reset from EJTAG Probe

The EJTAG specification requires the RST* pin on the EJTAG header to reset the board. Many ICE probes use the RST* pin (which is open drain output) to sense whether power is applied to the probe. When the EJTAG probe initiates a board reset by bringing RST* low, the signal is driven low solidly.

However, at the end of the reset procedure the EJTAG probe cannot drive the RST* signal back high because this pin is an open drain output. The EJTAG probe must rely on a pullup resistor supplied by the board.

Even with a resistor as small as 1000 ohms, it takes a full 100ns to pull this signal high even when it is only driving one load. If that single load is an EPLD, the signal tends to oscillate a bit as it crosses the Vih threshold for the EPLD. This causes the EPLD to register the deassertion and reassertion of the RST* signal multiple times. Because all of the IDT parts require continuous reset pulses in the order of 100ms or greater, this oscillation causes the part to fail reset in an unpredictable way.

Listed below are two methods to avoid this problem.

1. The reset signal from the ICE probe can be routed through the power/reset management IC. Generally, these ICs contain an input which initiates a reset of the circuit. The pulse width of this reset depends on the resistor/capacitor combination attached to the IC.

2. If the signal goes into an EPLD, the assertion of RST* can be used to initiate a cold reset of the processor and board circuit. But when RST* deasserts, a counter with a count length of greater than two microseconds should be used before deasserting the cold reset to the processor and board.

The 79EB434 board uses the first method.

Software Recommendations

Operation of UART in Polled Transmit Mode

The RC32434 provides one UART which is designed to be compatible with both the 16450 and the 16550. The 16550 is identical to the 16450 except that the 16550 provides a 16 byte FIFO on both receive and transmit sides.

The UART for the 16550 is enabled by setting bit 0 of the Buffer Control Register, BCR[0].

There are two modes in which users can program the UART:

- *Interrupt driven mode, when it is supported by the UART controller and the board design*
- *Polled mode.*

The RC32434 UART behaves in compliance with the 16550 specifications in the interrupt driven mode.

FIFOs were introduced in the 16550 to enable the 16 bytes of FIFOs to be filled (transmit) or emptied (receive) in a single execution of the interrupt handler, thereby reducing the load on the CPU. However, these FIFOs can be used in polled mode, although the benefit is less compared to the interrupt driven mode.

Typically, in the polled transmit mode, the Line Status Register (LSR) checks to see if it is appropriate for the software to write the next byte to the UART or the FIFO. The 16550 specifications state that LSR[5] can be guaranteed to be 1 when the Transmit Holding Register (THR) is empty, and LSR[5] can be guaranteed to be a 0 when THR is not empty. A non-empty THR implies at least one byte in the FIFO buffer. Therefore, writing a single byte to the transmit FIFO ought to result in LSR[5] returning a 0. This does not happen on the RC32434.

IDT recommends two possible procedures for ensuring the current operation of the RC32434 when it is used in polled transmit mode:

- Test LSR[6] bit instead of LSR[5] bit. LSR[6] bit, when set to 1 by the controller, indicates to the user that the transmit buffer as well as the THR is empty. This will allow the user to transmit one byte at a time in the polled mode.
- Set the DMA mode in the FIFO Control Register, FCR[3], to 1. This will activate the TXRDY interrupt signal when the transmit FIFO buffer is completely empty and will deactivate the TXRDY signal when the buffer is completely full. The state of the TXRDY signal can be probed by software through the Interrupt Controller. Register Group 5 (IPEND5) deals with UART channel 0. TXRDY Interrupt State can be read through the “Interrupt Pending Register” corresponding to the UART channel under consideration. Once a completely empty buffer condition is sensed by polling the Interrupt Pending Register, up to 16 bytes can be written to the transmit FIFO in a single attempt without worrying about the level of fullness of the buffer, etc.

Ethernet Controller Software Reset

The RC32434 ethernet controller can be reset manually by clearing the EN bit in the corresponding ETHINTFC register. When the EN bit is cleared, an Ethernet interface reset is generated and the RIP bit is set to indicate that an Ethernet reset is in progress. The reset may take several clock cycles to complete due to the crossing of multiple clock domains. When the reset has completed, the RIP is cleared and the Ethernet interface may be re-enabled by setting the EN bit.

However, if the MII clocks disappear or are not present during the Ethernet interface reset, the RIP bit will remain set, preventing the Ethernet interface from being reset until an MII clock is provided. The only other way to clear the RIP bit is to generate a cold_reset. The Ethernet PHY normally drives the MII clocks. Consequently, the behavior described above can be avoided by ensuring that any software which resets the RC32434 Ethernet controller does not reset the Ethernet PHY at the same time.

UART Mode

Do not change between UART 16450 and 16550 modes (bit [0] of the FIFO control register) and then flush the FIFOs while there are characters still in the FIFO TX buffer waiting to be sent. This may result in a UART transmit status malfunction. If this happens, the TE and THR bits in the UARTxLS register may be permanently cleared until the interface is reset. Characters can otherwise still be transmitted and the other status signals will continue to function.