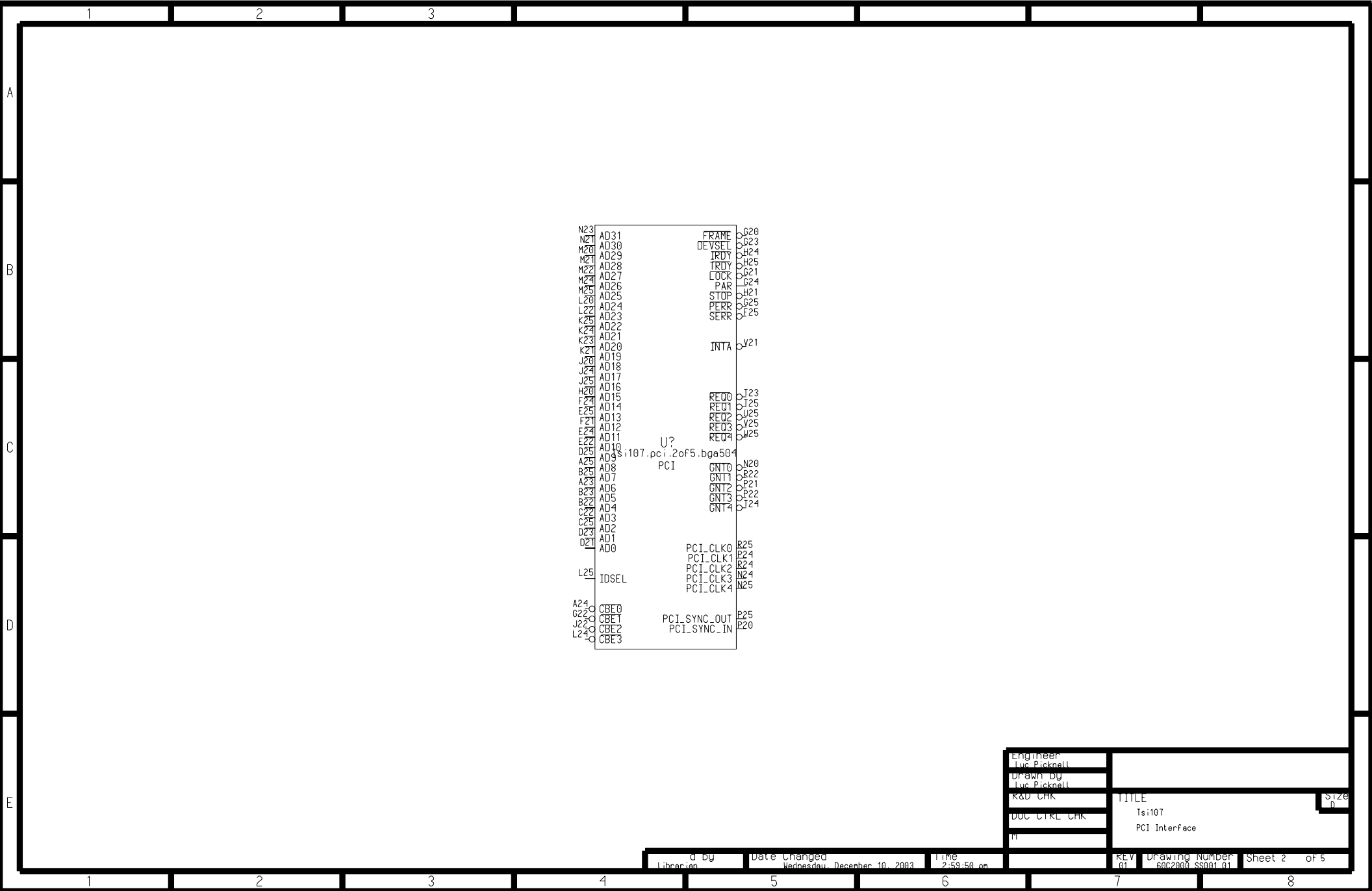


M6				CAS_DQM7	D11
L4	MDH0			CAS_DQM6	F12
L6	MDH1			CAS_DQM5	C2
K2	MDH2			CAS_DQM4	B3
K4	MDH3			CAS_DQM3	A10
K6	MDH4			CAS_DQM2	A11
J4	MDH5			CAS_DQM1	B1
J6	MDH6			CAS_DQM0	A2
H4	MDH7				C
H6	MDH8			RAS_CS7	B11
C8	MDH9			RAS_CS6	B10
G8	MDH10			RAS_CS5	F11
G6	MDH11			RAS_CS4	C10
F8	MDH12			RAS_CS3	E4
F6	MDH13			RAS_CS2	D5
E4	MDH14			RAS_CS1	C4
E6	MDH15			RAS_CS0	E6
B14	MDH16				C
D18	MDH17			SDBA0	A9
B18	MDH18			SDBA1	A8
E18	MDH19			SDMA0	A5
D18	MDH20			SDMA1	A6
C18	MDH21			SDMA2	B6
D18	MDH22			SDMA3	A7
D18	MDH23			SDMA4	C7
B18	MDH24			SDMA5	E7
F18	MDH25			SDMA6	B8
E18	MDH26			SDMA7	D8
E20	MDH27			SDMA8	E8
B20	MDH28	U?	Ts1:107.memory.1of5_bqa504	SDMA9	F8
B22	MDH29		Memory	SDMA10	D9
A22	MDH30			SDMA11	F9
H8	MDH31			SDMA12	E10
L4	MDL0			SDMA13	
L6	MDL1				A4
K4	MDL2			AS0	A13
K6	MDL3			FUE0	D10
J4	MDL4			RCS0	B9
J6	MDL5			RCS1	B5
H4	MDL6			RCS2	D7
H6	MDL7			RCS3	D4
G8	MDL8			SDCAS0	B4
G6	MDL9			SDRAS0	A3
C4	MDL10			WE0	A12
F4	MDL11			CKE	
G4	MDL12				C13
G6	MDL13			PAR_AR7	F13
F2	MDL14			PAR_ARG	D3
E2	MDL15			PAR_AR5	D1
F14	MDL16			PAR_AR4	A14
F18	MDL17			PAR_AR3	A15
A18	MDL18			PAR_AR2	C1
F18	MDL19			PAR_AR1	D2
B18	MDL20				D14
A18	MDL21			SDRAM_CLK0	D13
A18	MDL22			SDRAM_CLK1	E2
B18	MDL23			SDRAM_CLK2	E14
E18	MDL24			SDRAM_CLK3	
D18	MDL25				D12
D18	MDL26			SDRAM_SYNC_OUT	E13
F18	MDL27			SDRAM_SYNC_IN	
A20	MDL28				
C18	MDL29				
D20	MDL30				
A22	MDL31				

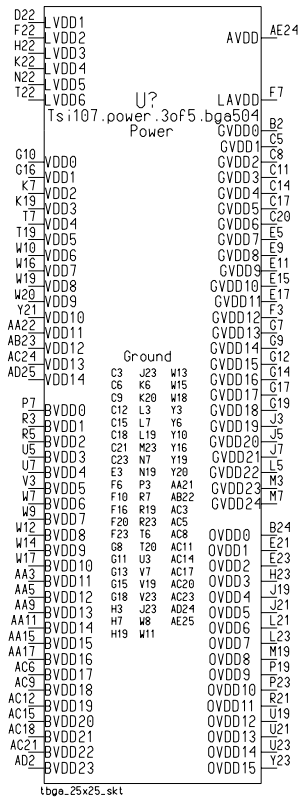
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Drawn By	Luc Picknell
R&D CHK	TI
DOC CTRL CHK	Ts1:107
MFG CTRL CHK	Memory Interface



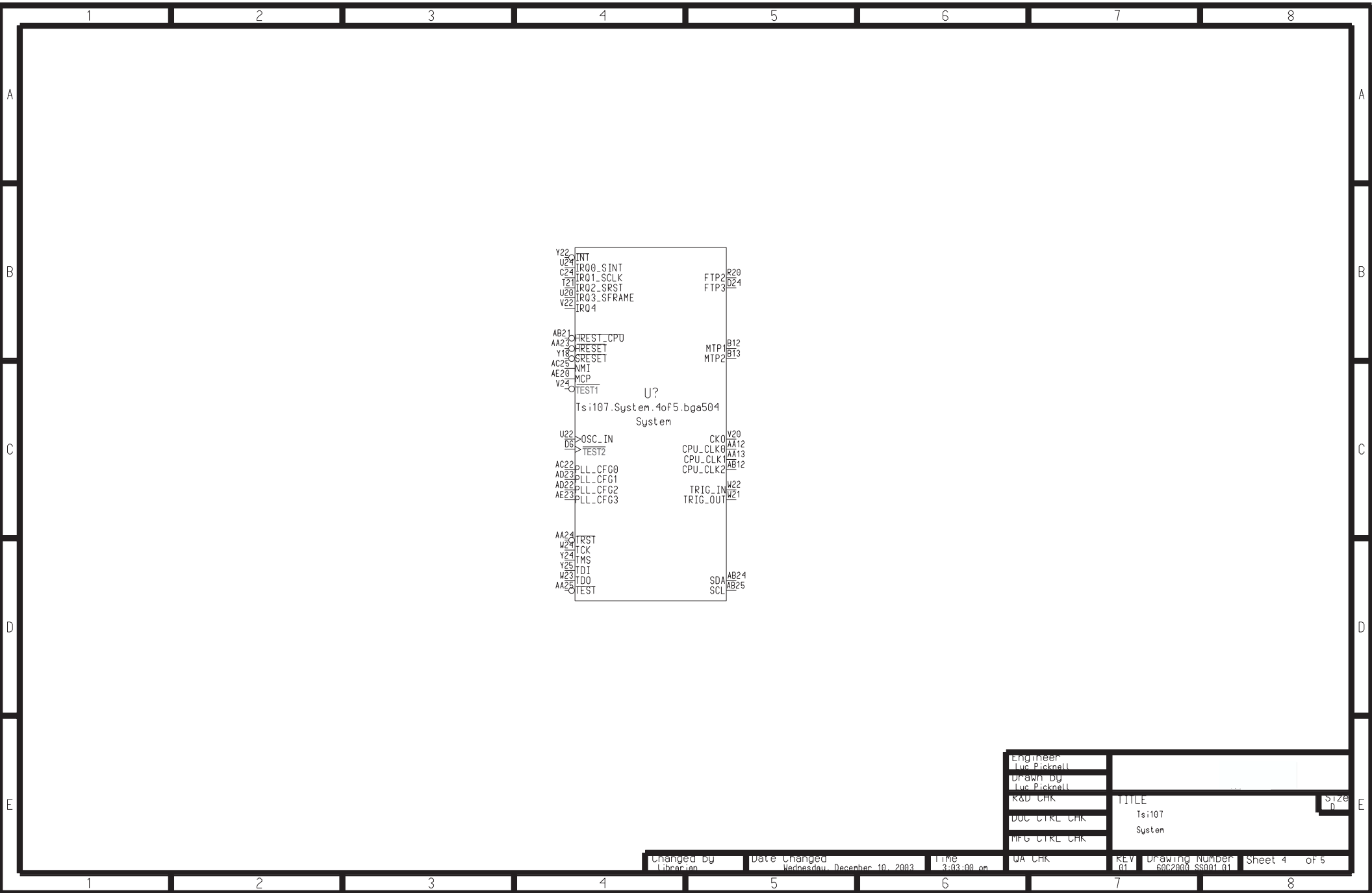
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N21	AD30	DEVSEL	G23
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M22	AD27	LOCK	G21
M23	AD26	PAR	G24
M24	AD25	STOP	H21
L20	AD24	PERR	G25
L22	AD23	SERR	F25
K23	AD22		
K24	AD21		
K25	AD20	INTA	V21
J20	AD19		
J21	AD18		
J22	AD17		
H20	AD16	REQ0	J23
F22	AD15	REQ1	J25
E25	AD14	REQ2	J25
F21	AD13	REQ3	J25
E24	AD12	REQ4	H25
E22	AD11		
D25	AD10	U?	
A25	AD9	PCI	
B25	AD8	GNT0	N20
A23	AD7	GNT1	J22
B23	AD6	GNT2	P21
B22	AD5	GNT3	P22
C22	AD4	GNT4	T24
C25	AD3		
D23	AD2		
D21	AD1		
L	AD0	PCI_CLK0	R25
		PCI_CLK1	E24
		PCI_CLK2	E24
		PCI_CLK3	N24
		PCI_CLK4	N25
L25	IDSEL		
A24	CBE0	PCI_SYNC_OUT	P25
G22	CBE1	PCI_SYNC_IN	P20
J22	CBE2		
L24	CBE3		

Engineer	Luc Picknell	
Drawn by	Luc Picknell	
R&D CHK		TITLE
DOC CTRL CHK		Ts1107
M		PCI Interface

Size D

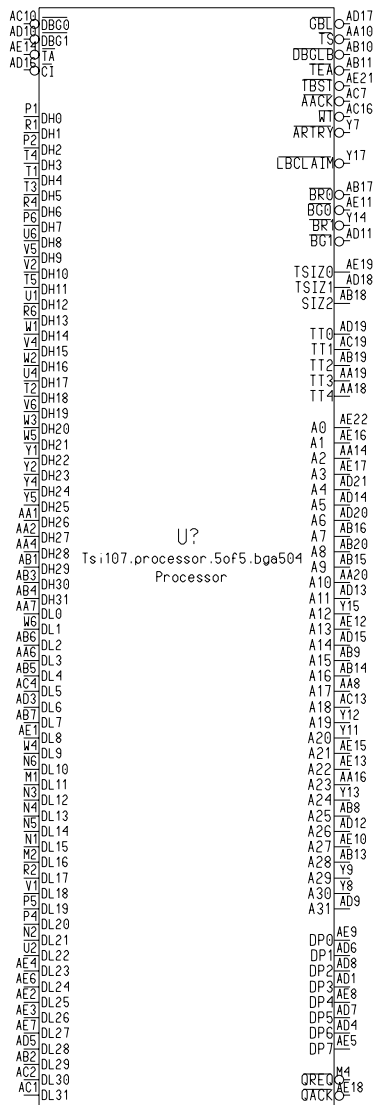


Engineer	Luc Picknell
Drawn By	Luc Picknell
R&D CHK	
DOC CTRL CHK	Tsi107
MFG CTRL CHK	Power Interface



Engineer	Luc Picknell	
Drawn By	Luc Picknell	
R&D CHK		TITLE
DOC CTRL CHK		Tsi107
MFG CTRL CHK		Systen

Changed By	Date Changed	Time	QA CHK	REV	Drawing Number	Sheet 4	of 5
Librarian	Wednesday, December 10, 2003	3:03:00 pm		01	60C2000_SS001_01		



Engineer  
Luc Picknett  
Drawn by  
Luc Picknett  
R&D CHK  
DUC CTRL CHK  
MFG CTRL CHK

Ts1107  
Processor Interface  
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