Renesas clock distribution products are used to condition, manipulate and distribute clock signals within a system, with or without the use of a phase-locked loop (PLL). These devices are well-suited for most applications where the input signal is of good quality, and the goal is to buffer, fan-out, divide, or multiplex the input signal. A single-output clock buffer is also useful for translating a clock from one signaling standard to another, such as LVCMOS-in to LVPECL-out.

As the industry leader in timing solutions, Renesas offers a rich portfolio of clock buffer, clock distribution and multiplexer solutions to meet the needs of virtually any application. Renesas has the largest portfolio of clock distribution devices that support differential signals. LVDS, LVPECL, HCSL, LVCMOS, CML, HSTL, SSTL are some of the most common I/O levels supported by these devices.

**Product categories**
- Fanout Buffers
- Zero-Delay Buffers
- Multiplexers

**Benefits**
- Low additive jitter/skew that lower system noise floor
- Programmable output clock type for design flexibility
- Wide operation voltage for design compatibility
- High integration reduces BOM cost, saves board space
- Re-use in different design base on built-in multiple OTP configuration

**Features**
- High-performance 2-20 output clock buffers
- Individually selectable output voltage 1.8V-2.5V-3.3V
- PCI Express buffers with Gen5 performance
- Programmable crystal load capacitance achieve high accuracy

**Typical Application Needs**
- Clock Dividers and Fanout Buffers
- Zero-Delay Buffers (ZDB)
- Multiplexers and Fanout Multiplexers
Buffer Summary by Functionality

LVCMOS
- Low Voltage
- Ultra Low Voltage

Differential
- LVPECL
- LVDS
- (LP-)HCSL
- SSTL
- CML
- HSTL

Configurable
- I2C Programmable
- Flexible Pin-Select

Standards
- PCIe
- JESD204B

Buffer Family Selection Guide

<table>
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<tr>
<th>SPB</th>
<th>9DB/9ZXL</th>
<th>8SLPV</th>
<th>8SLVD</th>
<th>8P34S</th>
<th>8T39S</th>
<th>8V79S6</th>
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<tbody>
<tr>
<td>I/O</td>
<td>LVCMOS</td>
<td>LPHCSL</td>
<td>LVPECL</td>
<td>LVDS</td>
<td>LVDS</td>
<td>Universal</td>
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<td></td>
<td>LVDS, LVPECL</td>
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<tr>
<td>Features</td>
<td>1<del>10 outputs, 2</del>20 outputs, OE</td>
<td>Single, dual functions and matched pinout</td>
<td>S/E, OE, 2 banks, XTAL I/F</td>
<td>Dual, Delay</td>
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<tr>
<td>fmax</td>
<td>200 MHz</td>
<td>100 MHz, 125 MHz</td>
<td>2 GHz</td>
<td>2 GHz</td>
<td>1.3-2.0 GHz</td>
<td>2 GHz</td>
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<tr>
<td>Supply</td>
<td>1.8V - 3.3V</td>
<td>1.8V - 3.3V</td>
<td>2.5V - 3.3V</td>
<td>2.5V</td>
<td>1.8V</td>
<td>2.5V, 3.3V, Mixed</td>
</tr>
</tbody>
</table>

To request samples, download documentation or learn more visit: renesas.com/buffers