JITTER ATTENUATORS WITH FREQUENCY TRANSLATION

IDT jitter attenuation with frequency translation products feature a PLL stage with VCXO technology to attenuate jitter and provide frequency translation. The output frequency from the PLL stage is then typically followed by a frequency divider.

A jitter attenuator is used to reduce the magnitude of jitter on a given timing signal. Jitter can be defined as the undesired deviation from an ideal periodic timing signal. Jitter may be observed in characteristics such as the frequency, phase, or amplitude of successive pulses. High levels of jitter can result in significant undesired system behavior in high-performance applications.

A frequency translator is used to convert the frequency of the input signal to the frequency required for the output signal. These devices typically consist of an oscillator or PLL, and a frequency divider.

A frequency translator circuit may be integrated with the jitter attenuator to simplify the circuit and minimize the BOM. IDT’s rich portfolio of jitter attenuators and frequency translators can address the needs of virtually any application.

Request samples and download software and documentation at www.idt.com/go/timing
Universal Frequency Translators (UFT)

Combine Flexibility with High Performance – The IDT UFT family is a programmable clock solution with the flexibility to apply virtually any input frequency and select virtually any output frequency. When used in the low-bandwidth frequency translator mode, the device can be used as a jitter attenuator to achieve precise frequency translation ratios. The devices’ high level of integration and low jitter eliminates the need for separate frequency translation, redundancy management, and jitter attenuation devices – empowering system designers to save cost and board area by consolidating these functions into a single device. Devices can power up with various pin selectable default configurations or be programmed through an I²C serial interface for additional flexibility after system power up.

Simply Solve Complex Timing Problems – The UFT family can use either a low cost crystal or up to four input reference clocks per PLL to generate any output frequency up to 1 GHz. Selections between the input references ensure reliable operation via input monitors, automatic hitless switching and holdover modes. In addition, capabilities such as gapped clock support inter-operates with OTN mappers and PHYs, and by allowing programmable loop bandwidth, different scenarios are enabled without changing board components.

New 3rd Generation Universal Frequency Translators – The IDT 8T49N28x family is generating eight different output frequencies with less than 300 femtoseconds RMS phase jitter over the standard 12 kHz to 20 MHz integration range. In addition, the devices offer significant flexibility in configuration and ease-of-programmability with IDT’s Timing Commander software, making it useful in a variety of sockets and modes of operation with minimal design effort.

The UFT family is ideal for high-performance optical networks, wireless base stations, and 100 Gigabit Ethernet (GbE) interface applications.

DEVELOPMENT TOOLS

Making Complex Configurations Simple

IDT Timing Commander is an easy-to-use Windows®-based software platform enabling system design engineers to configure, program and monitor sophisticated timing devices with an intuitive and flexible GUI.

UFT EVALUATION KIT

Features
- Stand-alone and evaluation board configuration
- Phase noise & power estimation
- PLL gain & phase transfer plots
- Input & output termination generator

BENEFITS:
- Fully programmable clock source adds flexibility to the design cycle
- High integration reduces BOM cost, saves board space
- Extremely low RMS jitter on all outputs for high-end communication applications
- Up to 4 clock inputs with automatic hitless switching produces a stable output frequency even when the primary input clock has failed

FEATURES:
- RMS phase jitter <0.3ps (12kHz to 20MHz)
- Accepts up to four LVPECL, LVDS, LHSTL, HCSL or LVCMOS input clocks ranging from 8kHz up to 875MHz
- Generates any output frequency from 8 kHz to 1 GHz (LVPECL / LVDS / HCSL), up to 250 MHz (LVCMOS)
- Registers programmable through I²C / SPI interfaces or via external I²C EEPROM
- On-die non-volatile memory allows device to be fully functional at power-up
- Gapped clock support inter-operates with OTN mappers and PHYs
TYPICAL APPLICATION: OPTICAL LINE CARD

- Universal Frequency Translators
- VCXO PLL Jitter Attenuators
- IDT Oscillator

IDT provides a broad portfolio of Jitter Attenuators with frequency translation, as well as other high performance Timing products to support a variety of networking applications, including 10GbE line cards.

Universal Frequency Translator Featured Products

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Core Voltage (V)</th>
<th>Input Frequency (MHz)</th>
<th>Input Type</th>
<th># Inputs</th>
<th># Outputs</th>
<th>Output Banks</th>
<th>Output Frequency (MHz)</th>
<th>Output Type</th>
<th>Phase Noise Typ RMS (ps)</th>
<th>Loop Bandwidth Range (Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8T49N285</td>
<td>2.5, 3.3</td>
<td>0.008 - 875</td>
<td>LVPECL, LVDS, LVHSTL, HCSL, LVCMOS</td>
<td>2</td>
<td>8</td>
<td>8</td>
<td>0.008 - 1000</td>
<td>LVPECL, LVDS, HCSL, LVCMOS</td>
<td>0.28</td>
<td>1.4 - 360</td>
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<tr>
<td>8T49N286</td>
<td>2.5, 3.3</td>
<td>0.008 - 875</td>
<td>LVPECL, LVDS, LVHSTL, HCSL, LVCMOS</td>
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<td>8</td>
<td>8</td>
<td>0.008 - 1000</td>
<td>LVPECL, LVDS, HCSL, LVCMOS</td>
<td>0.28</td>
<td>1.4 - 360</td>
</tr>
<tr>
<td>8T49N287</td>
<td>2.5, 3.3</td>
<td>0.008 - 875</td>
<td>LVPECL, LVDS, LVHSTL, HCSL, LVCMOS</td>
<td>2</td>
<td>8</td>
<td>8</td>
<td>0.008 - 1000</td>
<td>LVPECL, LVDS, LVCMOS</td>
<td>0.28</td>
<td>1.4 - 360</td>
</tr>
<tr>
<td>8T49N366I</td>
<td>2.5</td>
<td>0.008 - 710</td>
<td>LVCMOS, LVTTL, HCSL, LVHSTL, LVDS, LVPECL</td>
<td>7</td>
<td>6</td>
<td>3</td>
<td>0.98-1300</td>
<td>LVPECL, LVDS</td>
<td>0.333</td>
<td>10 - 580</td>
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<td>0.98-1300</td>
<td>LVPECL, LVDS</td>
<td>0.333</td>
<td>10 - 580</td>
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<tr>
<td>8T49N488I</td>
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<td>0.008 - 710</td>
<td>LVCMOS, LVTTL, HCSL, LVHSTL, LVDS, LVPECL</td>
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<td>8</td>
<td>4</td>
<td>0.98-1300</td>
<td>LVPECL, LVDS</td>
<td>0.333</td>
<td>10 - 580</td>
</tr>
</tbody>
</table>
VCXO PLL Jitter Attenuators

IDT voltage-controlled crystal oscillator (VCXO) jitter attenuator devices are synchronous jitter attenuation and frequency translation products featuring a VCXO-based PLL stage with either internal VCXO requiring only an external pull-able crystal, or with an external low frequency VCXO. This PLL stage is typically configured with low loop bandwidth to provide jitter attenuation. It can also accommodate numerous pre, feedback, and output divider combinations to allow for frequency translation. The output frequency from the VCXO PLL stage is then followed by a frequency multiplier.

The FemtoClock versions provide the capability to generate output frequencies up to 800 MHz with typical random phase-noise jitter of 1 ps RMS, while the NG versions can provide a maximum output frequency of up to 1.3 GHz and a typical random phase-noise jitter of less than 0.7 ps RMS.

VCXO PLL Jitter Attenuator Featured Products

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Abs. Pull Range Min. (ppm)</th>
<th>Core Voltage (V)</th>
<th>Input Frequency (MHz)</th>
<th>Input Type</th>
<th># Inputs</th>
<th># Outputs</th>
<th>Output Banks</th>
<th>Output Frequency (MHz)</th>
<th>Output Type</th>
<th>Phase Noise Typ RMS (ps)</th>
<th>Loop Bandwidth (Hz)</th>
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<tbody>
<tr>
<td>813N252i-02</td>
<td>±100</td>
<td>3.3</td>
<td>0.008 - 155.52</td>
<td>LVPECL, LVDS, LVHSTL, HCSL, SSTL</td>
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<td>2</td>
<td>2</td>
<td>25 - 312.5</td>
<td>LVPECL</td>
<td>0.65</td>
<td>7 - 45</td>
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<tr>
<td>813N252i-04</td>
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<td>3.3</td>
<td>0.008 - 155.52</td>
<td>LVPECL, LVDS, LVHSTL, HCSL, SSTL</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>25 - 312.5</td>
<td>LVPECL, LVDS</td>
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<td>8 - 75</td>
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<td>0.008 - 155.52</td>
<td>LVPECL, LVDS, LVHSTL, HCSL, SSTL</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>25 - 312.5</td>
<td>LVPECL</td>
<td>0.25</td>
<td>8 - 75</td>
</tr>
<tr>
<td>813N252i-02</td>
<td>±50</td>
<td>3.3</td>
<td>0.008 - 156.25</td>
<td>LVPECL, LVDS, LVHSTL, HCSL</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>19.44 - 622.08</td>
<td>LVPECL</td>
<td>0.675</td>
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<td>813N2532</td>
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<td>0.008 - 38.88</td>
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<td>2</td>
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<td>19.44 - 156.25</td>
<td>LVPECL</td>
<td>0.622</td>
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<tr>
<td>810N322i-02</td>
<td>±50</td>
<td>3.3</td>
<td>0.008 - 156.25</td>
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<td>2</td>
<td>2</td>
<td>2</td>
<td>19.44, 77.76, 155.52, 622.08</td>
<td>LVCMOS</td>
<td>0.624</td>
<td>14 - 52</td>
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<tr>
<td>810N252i-02</td>
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<td>3.3</td>
<td>0.008 - 155.52</td>
<td>LVPECL, LVDS, LVHSTL, HCSL</td>
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<td>2</td>
<td>2</td>
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<td>0.67</td>
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<td>810001-21</td>
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<td>3.3</td>
<td>15.609kHz - 74.324kHz</td>
<td>LVCMOS, LVTTL</td>
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<td>1</td>
<td>1</td>
<td>26.9750 - 148.5</td>
<td>LVCMOS, LVTTL</td>
<td>1.089</td>
<td>6 - 475</td>
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<tr>
<td>813078i</td>
<td>±50</td>
<td>3.3</td>
<td>10, 12.8, 15.36, 20, 30.72, 61.44, 122.88</td>
<td>LVPECL, LVDS, LVHSTL</td>
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<td>3</td>
<td>30.72, 38.4, 61.44, 76.8, 122.88, 155.6, 245.76, 491.52, 614.4</td>
<td>LVPECL</td>
<td>1.1</td>
<td>8.5 - 22.2</td>
</tr>
</tbody>
</table>

These products represent only a portion of IDT's FemtoClock portfolio. For information on additional devices, please visit www.idt.com/timing/vcxo.

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