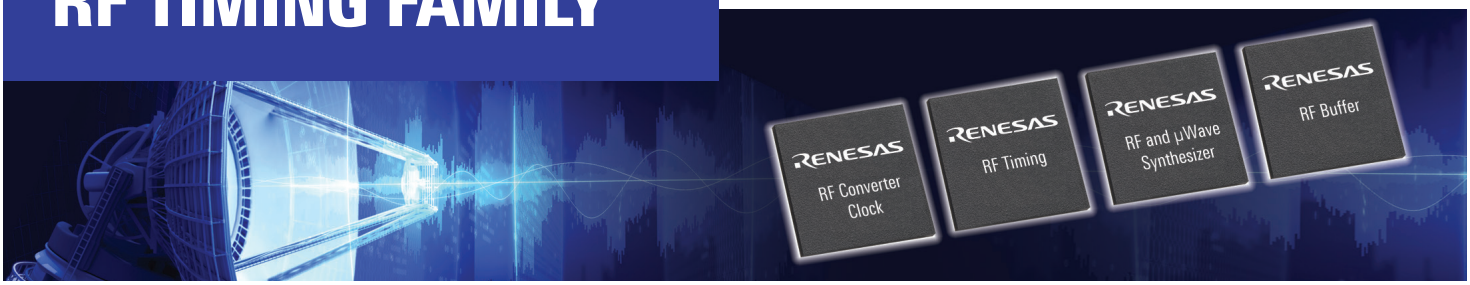
RENESAS
BIG IDEAS FOR EVERY SPACE

RF TIMING FAMILY



As part of its broad, market-leading timing portfolio, Renesas offers highly differentiated RF timing devices for applications where leading precision clocking, jitter attenuation, and low phase noise frequency generation are critical for system performance, such as wireless infrastructure 4G / 5G radio, communication systems, microwave, CATV, test and measurement equipment and industrial systems. Our broad portfolio of RF timing solutions delivers exceptional performance by combining our technology and technical innovations in compact packages.

Sampling clock generators offer leading phase noise and jitter for lowest radio EVM / EMR, excellent close-in phase noise for CPRI applications, high fanout for high-density radios, and JESD204B support for converter synchronization. These devices remove virtually all noise from input reference clock and some also support Synchronous Ethernet and IEEE 1588 synchronization for 5G and eCPRI applications.

RF and microwave synthesizers offer leading phase noise and spurious performance, low-power consumption and integrate wideband VCOs with frequencies supporting multi-carrier, multi-mode FDD and TDD base station radio card applications.

The industry's broadest buffer portfolio provides copies of RF clock signals with extremely low additive jitter and a wide range of optional features including phase delay adjustment, skew control, division capabilities, versatile input and output formats, and JESD204B support. Renesas RF buffers are available in a variety of fanout options.

For 5G massive MIMO and beamforming applications, our RF timing solutions also support extremely low phase skew drift in temperature to reduce occurrences of recalibration events in the radio paths and optimize actual data transmission.

Product categories

- RF and microwave synthesizers
- Jitter attenuators and sampling clock generators with JESD204B support
- RF buffers
- Radio synchronizers

Features

- Highly differentiated RF timing products
- Lowest clock phase noise and jitter
- Best spurious suppression
- Flexible frequency generation
- CPRI and eCPRI Synchronization synchronous Ethernet and IEEE 1588

Applications

Wireless Infrastructure

- Base transceiver station
- Distributed antenna system and repeaters
- Microwave (RF / IF)a
- High speed ADC / DAC / DUC / DDC clocking

Test and Measurement

- High-speed converter clocking
- Signal generator and spectrum analyzer
- Automated test equipment (ATE)

Military

- Tactical communication systems
- Radar

Wireless and Broadland Infrastructure

- Wireless and broadband
- infrastructure
- Broadband CATV
- Headend (CMTS), edge QAM
- Distribution nodes
- Cable modem, set-top box,
- DVR / PVR
- DOCSIS 3.1
- Satellite receivers and modems

RF TIMING FAMILY

Jitter Attenuation and Frequency Generation for ADC / DAC Reference Clocks

Renesas sampling clock generators address new radio designs including the latest 5G radio development, and continue to provide the industry's lowest phase noise clock signals. The jitter attenuation capability relies on an external VCXO and the RF frequency generation on an internal VCO. These devices generate multiple phase aligned high-frequency output signals. The dedicated low-noise architecture of the integer-N PLLs enables low EMR radio designs and increases the noise margin on the clock subsystem. These devices generate up to five clock frequencies from internal VCO(s) distributed to up to 18 low-skew differential outputs. An integrated pulse generator provides JESD204B-compliant SYSREF synchronization signals. The SYSREF outputs always synchronize to the incident rising clock edge. Outputs support symmetrical 100Ω (LVDS type) and LVPECL 50Ω termination with a configurable output amplitude up to 2000 mV differential.

Part Number	Application	Main Frequencies (MHz)	Outputs	Phase Noise
8V19N490A	CPRI / JESD204B	2949.12 and integer divisions	18	80fs (12 kHz to 20 MHz)
8V19N490-19	CPRI / JESD204B	2457.6 and integer divisions	18	80fs (12 kHz to 20 MHz)
8V19N490-24	CPRI / JESD204B	1966.08 and integer divisions	18	80fs (12 kHz to 20 MHz)
8V19N492	CPRI / JESD204B	2949.12 and integer divisions	15	80fs (12 kHz to 20 MHz)
8V19N470	CPRI	2949.12, 2457.6 and integer divisions	10	104fs (12 kHz to 20 MHz)
8V19N474	Ethernet	2500 and integer divisions	11	75fs (12 kHz to 20 MHz)

RF and Microwave PLL / Synthesizers

Renesas RF and Microwave PLLs integrate voltage-controlled oscillators (VCO) offering leading performance and an octave of frequency tuning range for multi-band local oscillator (LO) frequency synthesis up to 18 GHz. The wideband capability of these devices makes them ideal for applications where multiple frequencies are used or for reuse in different high-performance applications. Renesas RF PLLs offer low phase noise variation in temperature and operate up to 105°C case temperature, reducing the thermal constraints for the application.

Part Number	Grade	Input Frequency Range (MHz)	VCO Frequency Range (MHz)	Output Frequency Range (MHz)	FOM (dBc/Hz)	Output Power Range (dBm)	Package
8V97051L	GSM900	10 to 310	2200 to 4400	34.375 to 4400	-231	-4 to 7	32-VFQFN
8V97053L	GSM1800	10 to 310	2200 to 4400	34.375 to 4400	-231	-4 to 7	32-VFQFN
8V97003	5G	10 to 1600	5500 to 11000	172 to 18000	-237 (Integer) -231 (Fractional)	+14	48-VFQFN

RF Fanout Buffers

RF buffers extend the fanout of clock generators and RF synthesizer components. Typically driven by PLL components, RF buffers maintain the low phase noise and noise floor of the differential input signal. Each buffer provides exact copies of the input clock or data signal. Buffers have either a single or dual channels for driving clock and radio synchronization signals at the same propagation delay. IDT's fanout buffer portfolio contains buffers optimized for low additive phase noise, low output skew, low phase drift, deterministic phase delay and high frequency.

Part Number	Application	Output	Features	Frequency Max.
8V79S680	JESD204B	16 LVDS / LVPECL	Dual channel, Phase delay	3000 MHz
8T79S308	Universal	8 LVDS / LVPECL	Individual output enable	3000 MHz
8SLVP family	Universal 3.3V/2.5V single and dual buffers	Single 1:2 to 1:12 LVPECL Dual 1:2 to 1:8 LVPECL	Low additive phase noise	2000 MHz
8SLVD family	2.5V Universal single and dual buffers	Single 1:2 to 1:12 LVDS Dual 1:2 to 1:4 LVDS	Low additive phase noise	2000 MHz
8P34S family	1.8V Universal single and dual buffers	Single 1:2 to 1:12 LVDS Dual 1:2 to 1:8 LVDS	Low additive phase noise, low power	1200 to 2000 MHz

To request samples, download documentation or learn more visit: **idt.com/rftiming**

RENESAS

Renesas Electronics America Inc. | **renesas.com**
1001 Murphy Ranch Road, Milpitas, CA 95035 | Phone: 1-888-468-3774

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