Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA - 95054

PRODUCT/PROCESS CHANGE NOTICE (PCN)

PCN #: F0001-01 DATE: January 21, 2000

Product Affected: **72v2114Z** Product Family: FIFO

72v2101, 72v2111, 72v295, 72v2105, 72v263, 72v273,
72v283, 72v293, 72v2103, 72v2113, 72v3640, 72v3650
72v3660, 72v3670, 72v3680, 72v3690, 72v36100, 72v36110

Manufacturing Location Affected: Hillsboro, OR (Fab 4)

Date Effective: April 21, 2000

MEANS OF DISTINGUISHING CHANGED DEVICES:

- ■ Product Mark
- ☐ Back Mark
- ☐ Date Code
- ☐ Other

Contact: Dash Patel
Title: Product Assurance Manager
Phone # 408-330-1488
Fax #: 408-330-1450
E-mail: dasharath.patel@idt.com

Additional Data: Electrical parameters are unchanged

Samples: Available upon request

DESCRIPTION AND PURPOSE OF CHANGE:

- ■ Die Technology
- ■ Wafer Fabrication Process
- ☐ Assembly Process
- ☐ Equipment
- ☐ Material
- ☐ Testing
- ☐ Manufacturing Site
- ☐ Data Sheet

Minor mask change to improve manufacturing efficiency.
Change in stepping from 72v2114Z to 72v2114Y

RELIABILITY/QUALIFICATION SUMMARY:

Qualification and reliability data will be available upon request.

CUSTOMER ACKNOWLEDGMENT OF RECEIPT:

IDT records indicate that you require written notification of this change. Please use the acknowledgement below or e-mail to to grant approval or request additional information. If IDT does not receive acknowledgement within 30 days of this notice, it will be assumed that this change is acceptable.

Customer: _____ ☐ ***Approval for shipments prior to effective date.***

Name/Date: _____ E-Mail Address: _____

Title: _____ Phone# /Fax# : _____

CUSTOMER COMMENTS: _____

_____

RECD. BY: _____ DATE: _____

ATTACHMENT - I

PCN Summary Upgrade from stepping Z to stepping Y

PCN Type: Mask Change

Commodity FIFO

Due Date 5/1/00

Forecast or Execute Execute

Planned or Unplanned Planned

Data Sheet Change No Change

Detail of Change Change stepping from 72v2114Z to 72v2114Y

Stepping	Z	Y
Technology	CEMOS - 8	CEMOS - 8
# Meta Layers	2	
# Poly Layers	4	
Wafer Type	pprime	
Epitaxial Layer	none	S A M E
Crystal orientation	100 +/- 1 degree per SEMI STD	
Contact size	0.5 um	
Metal Via Size	0.6 um	A S
Passivation	8000A Nitride	
Metal 1 Composition	300A Ti; 1200A PVD TiN 100A CVD TiN; 4200A Al; 500A TiN	"Z"
Metal 1thickness/space	6300 A	
Minimum Metal 1 width/space	0.6/0.6 um	
Metal 2 Composition	300A Ti; 1000A PVD TiN 9500A Al; 340A TiN	S T E P P I N G
Metal 2 thickness	11140 A	
Minimum Metal 2 width/space	0.7/0.9 um	
Gate Material	140 A gate oxide 2500 A poly	
Minimum Gate Length	0.55 um	

Conversion Schedule (Estimated)

	Sample Availability	Production Shipments
72v2114Y	5/1/00	5/1/00

ATTACHMENT - II

Qualification Plan QFI-99-06

Test Vehicle: 72v2114Y **Expected Completion Date:** 5/1/00

	Qualification requirements	Expected Completion
	Samples / # fails	**Date**
Operating Dynamic Life test	77/0	5/1/00
1000 hours @ 135C. Vcc = 4.0 Volts		
ESD Human Body Model	12 / 0	5/1/00
ESD Charge device Model	12 / 0	5/1/00
Latch-UP	10 / 0	5/1/00
(tested to 1.5 X Vcc)		
Temperature Cycling	45 / 0	5/1/00
Electrical Characterization	10	5/1/00

Characterization Data:

The Y die step meets the current data sheet