



Integrated Device Technology, Inc.
6024 Silver Creek Valley Road, San Jose, CA 95138

PRODUCT/PROCESS CHANGE NOTICE (PCN)

PCN #: **I0909-01** DATE: **January 11, 2010**

Product Affected: **TSI310A-133CE, TSI310A-133CEY**

- Product Mark Top mark will show "Y" die revision
- Back Mark
- Date Code
- Other

Date Effective: **April 11, 2010**

Contact: PS Tow

Title: Director, Product Assurance

Attachment: Yes No

Phone #: (408) 284-8206

Fax #: (408) 284-1450

Samples: Available upon request

E-mail: pstow@idt.com

DESCRIPTION AND PURPOSE OF CHANGE:

- Die Technology
- Wafer Fabrication Process
- Assembly Process
- Equipment
- Material
- Testing
- Manufacturing Site
- Data Sheet
- Other

This PCN is to document wafer fab production from IBM Altis, France to IBM Burlington, USA. In relation to this change, polyimide material will be converted from Duramid 7510 to HD4004 for chemical consolidation and capacity improvement.

Attachment I details the qualification data for this change.

RELIABILITY/QUALIFICATION SUMMARY:

Refer to the attached qualification summary.

CUSTOMER ACKNOWLEDGMENT OF RECEIPT:

IDT records indicate that you require written notification of this change. Please use the acknowledgement below or E-Mail to grant approval or request additional information. If IDT does not receive acknowledgement within 30 days of this notice it will be assumed that this change is acceptable.

IDT reserves the right to ship either version manufactured after the process change effective date until the inventory on the earlier version has been depleted.

Customer: _____

Approval for shipments prior to effective date.

Name/Date: _____

E-Mail Address: _____

Title: _____

Phone # /Fax #: _____

CUSTOMER COMMENTS: _____

IDT ACKNOWLEDGMENT OF RECEIPT:

RECD. BY: _____

DATE: _____



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PCN Type: Fab Site and Material Change

Data Sheet Change: None

Detail of Change: This PCN is to document wafer fab production from IBM Altis, France to IBM Burlington, USA. In relation to this change, polyimide material will be converted from Duramid 7510 to HD4004 for chemical consolidation and capacity improvement.

Table 1 as shown below depicts the comparizon between old fab site and new fab site.

Description	Old Fab Site	New Fab Site
Wafer Fab	IBM Altis, France	IBM Burlington, USA
Die Revision	Z	Y
Fab Technology	0.25µm CMOS 6SF	0.25µm CMOS 6SF
# Poly Layers	1	1
# Metal Layers	5	5
Minimum Gate Length (µm)	0.25	0.25
Die Dimensions (mm ²)	7.8904	7.8904

Sample Availability: Now. Contact sales to request samples.



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Qualification Plan #: 80B6010_QR004_04

Test Vehicle: Device TSI310A built in 304 HPBGA, die size 7.89 mm² (device qual)
Package 580 HPBGA, die size 9.93 mm² (package qual)

Qualification Test Plan and Result:

Qual Type	Test Description	Test Method (Latest specs in effect)	Test Results SS / Rej
Device Qual	High Temperature Operating Life (Dynamic) (+125°C @ 1000 hours or equivalent)	Per IBM ASIC Design certification methodology	500 **
	ESD: Human Body Model @ 4000 Volts	EIA/JESD22-A114-A	4/0
	ESD: Machine Model @ 200 Volts	EIA/JESD22-A115-A	9/0
	ESD: Charged Device Model @ 1000 Volts	JESD22-C101	9/0
	Latch-up (+ - I and V stress, + - 100mA Trigger)	EIA/JESD78	6/0
Package Qual	Highly Accelerated Stress Test *(Unbiased, @ +130°C, 85%RH, 96 hours)	JESD22-A118	45/0
	Temperature Cycling *(-55°C to +125°C, 1000 cycles)	JESD22-A104-A	75/0
	High Temperature Storage Bake (+150°C, 1000 hours)	JESD22-A103-B	45/0

* Preconditioning per JESD22-A113 Level 3

** 1 failure after 3.089 Cum hours of stress testing @ 3.25V/140°C / 144 hours of stress test.

Failure attributed to Tungsten fill issue. Corrective action implemented. Continuous HTOL monitoring of the process reveals no failure and evidence of this failure mechanism.