Integrated Device Technology, Inc.
6024 Silver Creek Valley Road, San Jose, CA 95138

PRODUCT/PROCESS CHANGE NOTICE (PCN)

PCN #: **N1608-01** Date: August 18, 2016
Product Affected: 8T74S208A-01NLGI(8)

Date Effective: November 18, 2016

MEANS OF DISTINGUISHING CHANGED DEVICES:
- ■ Product Mark Change in ordering part#
- ☐ Back Mark
- ☐ Date Code
- ☐ Other

Contact: TSD Clock Team
E-mail: clocks@idt.com

Attachment: ■ Yes ☐ No

Samples: Samples are available now.

DESCRIPTION AND PURPOSE OF CHANGE:

- ☐ Die Technology
- ☐ Wafer Fabrication Process
- ☐ Assembly Process
- ☐ Equipment
- ☐ Material
- ☐ Testing
- ☐ Manufacturing Site
- ■ Data Sheet
- ■ Other - Die Revision Change

The device 8T74S208C-01 is a redesign of the 8T74S208A-01 that eliminates an output signal integrity issue during output enable. The redesign changed the internal timing of the output enable logic: instead of turning on outputs at the same time, the new output enable circuit turns on outputs one by one (one after the other). The increased output enable time is still within the original specification of the current 8T74S208A-01 silicon. The parameters power supply current, output power supply, propagation delay (input to any output) and output rise time are updated as a consequence of the redesign. All changed parameters are listed in the tables below.
The redesign only involved changes of metal layers (connection layers). Silicon and package technology was not modified.
IDT requests a transition from the 8T74S208A-01 to the 8T74S208C-01, alternatively, we are offering a last time buy of the 8T74S208A-01 by November 18, 2016.

RELIABILITY/QUALIFICATION SUMMARY:

There is no change in die technology/process.

CUSTOMER ACKNOWLEDGMENT OF RECEIPT:

IDT records indicate that you require written notification of this change. Please use the acknowledgement below or E-Mail to grant approval or request additional information. If IDT does not receive acknowledgement within 30 days of this notice it will be assumed that this change is acceptable.
IDT reserves the right to ship either version manufactured after the process change effective date until the inventory on the earlier version has been depleted.

Customer: _____ ☐ ***Approval for shipments prior to effective date.***

Name/Date: _____ E-Mail Address: _____

Title: _____ Phone # /Fax #: _____

CUSTOMER COMMENTS: _____

IDT ACKNOWLEDGMENT OF RECEIPT:

RECD. BY: _____ DATE: _____

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ATTACHMENT 1 - PCN #: N1608-01

PCN Type: Die Revision Change / Datasheet

Data Sheet Change: Yes

Detail of Change: The device 8T74S208C-01 is a redesign of the 8T74S208A-01 that eliminates an output signal integrity issue during output enable. The redesign changed the internal timing of the output enable logic: instead of turning on outputs at the same time, the new output enable circuit turns on outputs one by one (one after the other). The increased output enable time is still within the original specification of the current 8T74S208A-01 silicon. The parameters power supply current, output power supply, propagation delay (input to any output) and output rise time are updated as a consequence of the redesign. All changed parameters are listed in the tables below.
The redesign only involved changes of metal layers (connection layers). Silicon and package technology was not modified.
IDT requests a transition from the 8T74S208A-01 to the 8T74S208C-01, alternatively, we are offering a last time buy of the 8T74S208A-01 by November 18, 2016.

FROM: 8T74S208A-01

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
I_{DD}	Power Supply Current			41	49	mA
I_{DDO}	Output Supply Current	All Outputs are Enabled and Terminated		153	176	mA

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
tPD	Propagation Delay	IN, nIN to Qx, nQx	FSEL[1:0] = 00	420		620	ps
			FSEL[1:0] = 01	580		800	ps
			FSEL[1:0] = 10	680		920	ps
			FSEL[1:0] = 11	780		1050	ps
t_R/t_F	Output Rise/ Fall Time		20% to 80%		155	230	ps
			10% to 90%		245	350	ps

TO: 8T74S208C-01

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
I_{DD}	Power Supply Current			54	64	mA
I_{DDO}	Output Supply Current	All Outputs are Enabled and Terminated		155	182	mA

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
tPD	Propagation Delay	IN, nIN to Qx, nQx	FSEL[1:0] = 00	420		700	ps
			FSEL[1:0] = 01	580		880	ps
			FSEL[1:0] = 10	680		1080	ps
			FSEL[1:0] = 11	780		1180	ps
t_R/t_F	Output Rise/ Fall Time		20% to 80%		155	230	ps
			10% to 90%		245	370	ps

Table 1: Changes in Orderable Part#

Old Ordering Part Number	New Ordering Part Number
8T74S208A-01NLGI	8T74S208C-01NLGI
8T74S208A-01NLGI8	8T74S208C-01NLGI8

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ATTACHMENT 1 - PCN #: N1608-01

Qualification Test Plan and Result:

Qual Vehicle: 8T74S208C-01NLGI

Test Description	Test Method (Latest specs in effect)	Test Results (SS / Rej)
ESD: Human Body Model @ 2000V	JS-001-2012	3/0
ESD: Charged Device Model @ 500V	JESD22-C101	3/0
Latch-up	JESD78	6/0