Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA - 95054

PRODUCT/PROCESS CHANGE NOTICE (PCN)

PCN #: SR-0402-02 DATE: 3/3/04
Product Affected: IDT71V424S/L

Date Effective: 6/2/04

MEANS OF DISTINGUISHING CHANGED DEVICES:
- ☐ Product Mark
- ☐ Back Mark
- ■ Date Code "Y" die revision in date code
- ☐ Other

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Attachment:: ■ Yes ☐ No

Samples: Refer to page 2 for sample availability

DESCRIPTION AND PURPOSE OF CHANGE:
- ■ Die Technology
- ☐ Wafer Fabrication Process
- ☐ Assembly Process
- ☐ Equipment
- ☐ Material
- ☐ Testing
- ☐ Manufacturing Site
- ■ Data Sheet
- ☐ Other

This is an update to PCN SR0008-03 which documented the die revision change from Z to Y. The Z step was from IDT's Cmos 10 .28um technology, the Y step is Cmos 11.5 .18um technology. The The Y-step die revision is now ready for production release.

Customers may continue to order the current IDT p/n or may specify "Y" in the p/n (see attachment).

This die revision will also incorporate a data sheet change for the Isb limit. Refer to page 2 for details

RELIABILITY/QUALIFICATION SUMMARY:

Device qualification details shown on attachment verifies that there is no change to the device reliability

CUSTOMER ACKNOWLEDGMENT OF RECEIPT:

IDT records indicate that you require written notification of this change. Please use the acknowledgement below or E-Mail to grant approval or request additional information. If IDT does not receive acknowledgement within 30 days of this notice it will be assumed that this change is acceptable.
IDT reserves the right to ship either version manufactured after the process change effective date until the inventory on the earlier version has been depleted.

Customer: _____ ☐ ***Approval for shipments prior to effective date.***

Name/Date: _____ E-Mail Address: _____

Title: _____ Phone# /Fax# : _____

CUSTOMER COMMENTS: _____

IDT ACKNOWLEDGMENT OF RECEIPT:

RECD. BY: _____ DATE: _____

ATTACHMENT - PCN #: SR-0402-02

PCN Summary

PCN Type: Mask/Design Change for Die Shrink and Data Sheet change

Commodity Memory

Forecast or Execute Execute

Planned or Unplanned Planned

Data Sheet Change Isb limit

Detail of Change

Die Step Details

Die Revision (step)	Z	Y
Wafer Fab Technology	Cmos 10	Cmos 11.5
# Poly Layers	3	1
# Metal Layers	2	3
Minimum Feature Size	0.28 um	0.18 um
Die Dimensions (sq mils)	85k	57k

Data Sheet limit for Isb for all part#'s listed in this PCN will change as shown below
IDT71V424YS/L and IDT71V424S/L will change to 55mA (from 40mA)

Sample Availability: IDT71V424Y Now

Production Shipments: Customer shipments for this die revision will start June 02, 2004 unless specifically requested.

Product Details

Current IDT Part No.	Optional IDT Part No.	Current IDT Part No.	Optional IDT Part No.
IDT71V424L10PH	IDT71V424YL10PH	IDT71V424S12PH8	IDT71V424YS12PH8
IDT71V424L10PH8	IDT71V424YL10PH8	IDT71V424S12PHI	IDT71V424YS12PHI
IDT71V424L10PHI	IDT71V424YL10PHI	IDT71V424S12PHI8	IDT71V424YS12PHI8
IDT71V424L10PHI8	IDT71V424YL10PHI8	IDT71V424S12Y	IDT71V424YS12Y
IDT71V424L10Y	IDT71V424YL10Y	IDT71V424S12Y8	IDT71V424YS12Y8
IDT71V424L10Y8	IDT71V424YL10Y8	IDT71V424S12YI	IDT71V424YS12YI
IDT71V424L12PH	IDT71V424YL12PH	IDT71V424S12YI8	IDT71V424YS12YI8
IDT71V424L12PH8	IDT71V424YL12PH8	IDT71V424S15PH	IDT71V424YS15PH
IDT71V424L12PHI	IDT71V424YL12PHI	IDT71V424S15PH8	IDT71V424YS15PH8
IDT71V424L12PHI8	IDT71V424YL12PHI8	IDT71V424S15PHI	IDT71V424YS15PHI
IDT71V424L12Y	IDT71V424YL12Y	IDT71V424S15PHI8	IDT71V424YS15PHI8
IDT71V424L12Y8	IDT71V424YL12Y8	IDT71V424S15Y	IDT71V424YS15Y
IDT71V424L12YI	IDT71V424YL12YI	IDT71V424S15Y8	IDT71V424YS15Y8
IDT71V424L12YI8	IDT71V424YL12YI8	IDT71V424S15YI	IDT71V424YS15YI
IDT71V424L15PH	IDT71V424YL15PH	IDT71V424S15YI8	IDT71V424YS15YI8
IDT71V424L15PH8	IDT71V424YL15PH8	IDT71V424S12PHGI8	IDT71V424YS12PHGI8
IDT71V424L15PHI	IDT71V424YL15PHI	IDT71V424S15PHG	IDT71V424YS15PHG
IDT71V424L15PHI8	IDT71V424YL15PHI8	IDT71V424S15PHG8	IDT71V424YS15PHG8
IDT71V424L15Y	IDT71V424YL15Y	IDT71V424S15PHGI	IDT71V424YS15PHGI
IDT71V424L15Y8	IDT71V424YL15Y8	IDT71V424S15PHGI8	IDT71V424YS15PHGI8
IDT71V424L15YI	IDT71V424YL15YI	IDT71V424S12PHG	IDT71V424YS12PHG
IDT71V424L15YI8	IDT71V424YL15YI8	IDT71V424S12PHG8	IDT71V424YS12PHG8
IDT71V424S10PH	IDT71V424YS10PH	IDT71V424S12PHGI	IDT71V424YS12PHGI
IDT71V424S10PH8	IDT71V424YS10PH8	IDT71V424S10PHG	IDT71V424YS10PHG
IDT71V424S10Y	IDT71V424YS10Y	IDT71V424S10PHG8	IDT71V424YS10PHG8
IDT71V424S10Y8	IDT71V424YS10Y8	IDT71V424S10PHGI	IDT71V424YS10PHGI
IDT71V424S12PH	IDT71V424YS12PH	IDT71V424S10PHGI8	IDT71V424YS10PHGI8

ATTACHMENT - PCN #: SR-0402-02

Qualification Plan #: QS-0008-10R3
Test Vehicle: 71V416Y (Base device for 71V424Y)

Qualification Results

Package Type: TSOP-44

TEST DESCRIPTION	Sample Size / # Fails	Comments
High Temperature Operating Life (Dynamic) JESD22-A108, +125°C @ 1000 hours or equivalent	347/0	
Highly Accelerated Stress Test: JEDEC STD 22, Method A110, Biased, @+130°C, +85%RH, 3 Atm, 100 hours*	90/0	
Autoclave: EIA/JESD22-A102 @ 2 ATM, Saturated Steam @ 121°C, 168 hours*	90/0	
Temperature Cycling: JESD22-A104, Condition C, -65°C to +150°C, 500 cylces*	45/0	
High Temp Storage: JESD22-A103 +150°C, 1000 hours	77/0	
ESD: Human Body Model Mil-Std-883, method 3015	6/0	Rating: 3000V
ESD: Charged device Model JEDEC 22-101	6/0	Rating: 1000V
Latch-up EIA/JESD STD-78	30/0	

* Preconditioning per JESD22-A113B Level 3

Characterization of the IDT71V424S/L confirms that there is no change to the datasheet except as noted for the change to the Isb limits.