Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA - 95054

PRODUCT/PROCESS CHANGE NOTICE (PCN)

PCN #: SR0008-03 DATE: 8/21/00
Product Affected: 71V416S/L, 71V424S/L, 71V428S/L

Manufacturing Location Affected: N/A
Date Effective: 11/20/00

MEANS OF DISTINGUISHING CHANGED DEVICES:
- ■ Product Mark Y character on top mark
- ☐ Back Mark
- ☐ Date Code
- ☐ Other

Contact: Lakshmi Srinivasan
Title: Quality Engineering Supervisor
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Attachment:: ■ Yes ☐ No

Samples: Available on request

DESCRIPTION AND PURPOSE OF CHANGE:

- ■ Die Technology
- ■ Wafer Fabrication Process
- ☐ Assembly Process
- ☐ Equipment
- ☐ Material
- ☐ Testing
- ☐ Manufacturing Site
- ☐ Data Sheet
- ☐ Other

Die and Technology Upgrade. Current die revision "Z" (Cmos 10) will be replaced by die revision "Y" (Cmos 11.5)

RELIABILITY/QUALIFICATION SUMMARY:

Qualification is expected to be completed 11/10/00 and will be available on request.

CUSTOMER ACKNOWLEDGMENT OF RECEIPT:

IDT records indicate that you require written notification of this change. Please use the acknowledgement below or E-Mail to grant approval or request additional information. If IDT does not receive acknowledgement within 30 days of this notice it will be assumed that this change is acceptable.
IDT reserves the right to ship either version manufactured after the process change effective date until the inventory on the earlier version has been depleted.

Customer: _____ ☐ ***Approval for shipments prior to effective date.***

Name/Date: _____ E-Mail Address: _____

Title: _____ Phone# /Fax# : _____

CUSTOMER COMMENTS: _____

IDT ACKNOWLEDGMENT OF RECEIPT:

RECD. BY: _____ DATE: _____

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ATTACHMENT - PCN #: SR0008-03

PCN Summary
PCN Type: Mask/Design Change for Die Shrink

Commodity Memory

Forecast or Execute Execute

Planned or Unplanned Planned

Data Sheet Change No

Detail of Change

Die Revision	Z		Y
Wafer Fab Facility	Hillsboro, OR		Hillsboro, OR
Wafer Fab Technology	CMOS 10		CMOS 11.5
Wafer Size	8 inch		8 inch
Cell Type	4T		6T
# Poly Layers	3		1
# Metal layers	2		3
Minimum Feature Size	0.29 um		0.18 um
Die Dimension / K sq mils	85		57.7

Conversion schedule (Estimated)

	Sample Availability	Production Shipments
71V416S/L	9/25/00	11/10/00
71V424S/L	9/25/00	11/10/00
71V428S/L	9/25/00	11/10/00

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Qualification Plan

Test Vehicle		Expected Completion Date 11/15/00	12/15/00
71V416Y	Required Sample / # Fails	LOT #1	LOT #2
Operating Life Test: Dynamic @+135°C, Vcc=4V for 750 hours	116 / 0		
High Temp. Storage Life Test (Unbiased, 1000 hours @+150°C)	77 / 0		
Bake & Ballshear Test @ 200°C / 4 ball bonds per device	5 / 0		
Thermal Shock: (-65°C to +150°C, 100 cycles)	45 / 0		
Temperature Cycling: (-65°C to +150°C, 1000 cycles)	45 / 0		
HAST: (Biased, 100 Hrs. @+130°C, +85%RH, 3 Atm.)	45 / 0		
Autoclave:(Unbiased, 2 Atm Saturated Steam, +121°C, 168 Hrs)	45 / 0		
ESD Human Body Model	6 / 0		
ESD Charged Device Model	6 / 0		
Latch up: (Tested to 2X Vcc)	10 / 0		

Tests are completed for unshaded areas. Product released is based on qualification of initial lot.

Characterization Data: Characterization will be completed as part of product qualification and data available upon request. Characterization will verify that there is no change to exisiting datasheet parameters.