












Note: This is the ballmap when looking through the top of the package. This ballmap represents the PCB footprint for the Tsi564A.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	NO_BALL	VSS	VSS	VSS	VSS	VSS	VSS	SP6_TD_P	VSS	SP6_TC_N	VSS	SP6_TB_P	VSS	SP6_TA_N	VSS	VSS	VSS	VSS	VSS	VSS
B	VSS	VSS	VSS	VSS	VSS	VSS	VSS	SP6_TD_N	VSS	SP6_TC_P	SP_VDD	SP6_TB_N	VSS	SP6_TA_P	SP_VDD	VSS	VSS	S_CLK_1_P	S_CLK_1_N	VSS
C	VSS	VSS	VSS	VSS	VSS	VSS	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	VSS	VSS	SP_VDD	VSS	SP_VDD
D	VSS	SP_VDD	VSS	VSS	VSS	VSS	VSS	SP6_RD_N	VSS	SP6_RC_P	SP6_RREF	SP6_RB_N	VSS	SP6_RA_P	VSS	VSS	VSS	S_CLK_2_P	S_CLK_2_N	VSS
E	SP0_TA_N	SP0_TA_P	SP_VDD	SP0_RA_P	SP0_RA_N	VSS	VSS	SP6_RD_P	SP6_VTT	SP6_RC_N	SP6_AVDD	SP6_RB_P	SP_VDD	SP6_RA_N	VSS	VSS	VSS	VSS	VSS	VSS
F	VSS	VSS	VSS	VSS	SP_VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
G	SP0_TB_P	SP0_TB_N	SP_VDD	SP0_RB_N	SP0_RB_P	VSS	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	SP4_RD_P	SP4_RD_N	SP_VDD	SP4_TD_N	SP4_TD_P
H	VSS	SP_VDD	VSS	SP0_RREF	SP0_AVDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VSS	SP4_VTT	VSS	VSS	VSS	VSS
J	SP0_TC_N	SP0_TC_P	SP_VDD	SP0_RC_P	SP0_RC_N	VSS	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	SP4_RC_N	SP4_RC_P	SP_VDD	SP4_TC_P	SP4_TC_N
K	VSS	VSS	VSS	VSS	SP0_VTT	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VSS	SP4_AVDD	SP4_RREF	VSS	SP_VDD	VSS
L	SP0_TD_P	SP0_TD_N	SP_VDD	SP0_RD_N	SP0_RD_P	VSS	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	SP4_RB_P	SP4_RB_N	SP_VDD	SP4_TB_N	SP4_TB_P
M	VSS	VDD_IO	VSS_IO	VSS	VSS	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VSS	SP_VDD	VSS	VSS	VSS	VSS
N	VSS_IO	SP4_PWRDN	SP5_PWRDN	VDD_IO	N/C	VSS	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	SP4_RA_N	SP4_RA_P	SP_VDD	SP4_TA_P	SP4_TA_N
P	SP6_PWRDN	VDD_IO	SP7_PWRDN	N/C	VSS_IO	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VSS	VSS	VSS	VSS	SP_VDD	VSS
R	VSS_IO	N/C	N/C	VDD_IO	N/C	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
T	N/C	VDD_IO	N/C	N/C	VSS_IO	N/C	VSS	SP2_RA_N	SP_VDD	SP2_RB_P	SP2_AVDD	SP2_RC_N	SP2_VTT	SP2_RD_P	VSS	SP_IO_SP_EED[0]	N/C	VSS_IO	N/C	N/C
U	VSS_IO	INT_B	SP4_MODESEL	VDD_IO	SP6_MODESEL	VSS	VSS	SP2_RA_P	VSS	SP2_RB_N	SP2_RREF	SP2_RC_P	VSS	SP2_RD_N	VSS	SP_IO_SP_EED[1]	VDD_IO	I2C_DISABLE	VDD_IO	TMS
V	N/C	VDD_IO	SW_RST_B	N/C	VSS_IO	N/C	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP0_MODESEL	SP2_MODESEL	VSS_IO	TDO	TDI
W	VSS_IO	N/C	N/C	VDD_IO	N/C	VSS	SP_VDD	SP2_TA_P	VSS	SP2_TB_N	SP_VDD	SP2_TC_P	VSS	SP2_TD_N	VSS	SP0_PWRDN	SP2_PWRDN	I2C_SD	VDD_IO	TRST_B
Y	P_CLK	VDD_IO	HARD_RST_B	N/C	VSS_IO	VSS	VSS	SP2_TA_N	VSS	SP2_TB_P	VSS	SP2_TC_N	VSS	SP2_TD_P	VSS	SP1_PWRDN	SP3_PWRDN	VSS_IO	I2C_SCLK	TCK

Legend

 VSS and VSS_IO	 JTAG	 Serial RapidIO Interface 0
 VDD and VDD_IO	 SP_VDD and SPx_AVDD	 Serial RapidIO Interface 2
 Miscellaneous	 S_CLK_x	 Serial RapidIO Interface 4
 No Ball and No Connect (N/C)		 Serial RapidIO Interface 6

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Revision History

August 2009, 80B802A_PN002_02 -- No technical changes. Formatting was changed to reflect IDT.