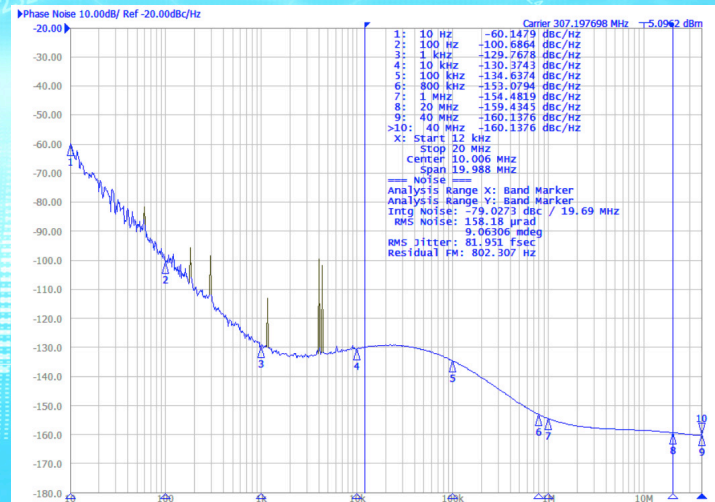
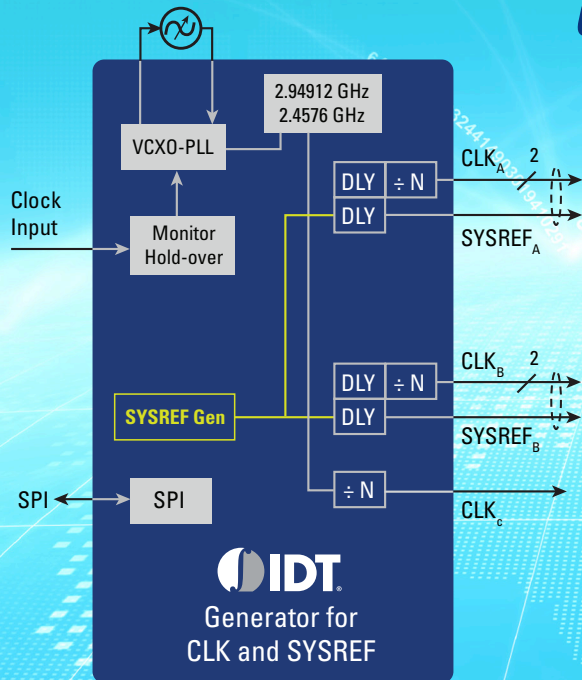


Generates JESD204B Compliant Clocks with Phase Noise < 100 fs RMS



FEATURES

- Flexible JESD204B timing source with single and dual VCO device options and a wide range of output frequency dividers
- Cleans input jitter from any digital clock source
- Meets stringent phase noise requirements of converters and high-speed PHYs
- Low phase noise clocks minimize converter errors, improve SNR figures, and improve bit error rates
- Meets blocker specifications in wireless radio applications
- Up to 3 GHz clock speed for RF converters
- Enables clock phase management

TARGET APPLICATIONS

- Wireless infrastructure radio and base-band clocking
- JESD204B converter clock and SYSREF signals
- 10/40/100 Gbps Ethernet line cards
- DOCIS/Cable TV head-end
- Radar
- Instrumentation, industrial and medical imaging

Industry-Leading Low Phase Noise Clocks

The 8V19N407/408 ultra-high-performance jitter attenuator and frequency synthesizer devices are ideal RF converter clocks enabling designers to generate pristine, low-phase clock signals in leading-edge high-speed communication applications. Key features are JESD204B compliance including SYSREF generation, input clock jitter attenuation, and flexible frequency and phase management on nine RF clock/SYSREF outputs. The integrated VCOs at 2.92 to 3.0, 2.4 to 2.5 and 1.9 to 2.0 GHz support multiple frequency plans. Output clock frequencies range from 25 MHz to 3 GHz. Universal LVDS/LVPECL outputs with configurable output amplitudes and flexible phase management ease system design. The devices work seamlessly with IDT's single and dual channel RF clock fanout buffers.

Part Number	Description
8V19N408Z	Dual VCO 2.94912 and 2.4 to 2.5 GHz clock jitter attenuator and frequency synthesizer
8V19N407Z-24	Single VCO 2.4 to 2.5 GHz clock jitter attenuator and frequency synthesizer
8V19N407Z-19	Single VCO 1.9 to 2.0 GHz clock jitter attenuator and frequency synthesizer

To request samples, download documentation or learn more, visit: idt.com/go/rf-clocks