



Feature Set and Performance Differences Between the 89HPES24N3 and 89HPES24N3A

Overview

The 89PES24N3A is second-generation, 24-lane 3-port PCI Express switching solution from IDT. The 89PES24N3A is pin-compatible with the IDT 89PES24N3 and offers an enhanced functional and performance feature set over the 89PES24N3. This document provides an overview of the key feature and performance differences between the two devices so that system designers can evaluate these differences and choose the device which best fits their system needs.

Feature Set and Performance Differences

The differences between the 89PES24N3 and the 89PES24N3A are grouped into two general areas, functional features and performance features. These differences are listed in Table 1 below.

| | 89PES24N3 | 89PES24N3A |
|--|------------------------------------|------------------------------------|
| Functional Features | | |
| PCI Express Base Standard Revision | 1.0a | 1.1 |
| Lane Reversal | Static | Automatic or Static |
| Peer-to-Peer Security (disable peer traffic) | NO | Per-port / Device |
| Legacy GPE Support for Hot Plug | NO | YES |
| SSID/SSVID Support (Windows logo requirement) | NO | YES |
| VGA 16-bit Decode (Windows logo requirement) | NO | YES |
| ISA Enable Support (Windows logo requirement) | NO | YES |
| Downstream Port Numbering | Port B = 1, Port C = 2 | Port B = 2, Port C = 4 |
| Configuration Space Base Address | Port B = 0x1000 Port C = 0x2000 | Port B = 0x2000 Port C = 0x4000 |
| Performance Features | | |
| Advertised Data Credits (Posted / Non-posted / Completion) | 204 / 30 / 204 | 416 / 64 / 416 |
| Advertised Header Credits (Posted / Non-posted / Completion) | 30 / 30 / 30 | 64 / 64 / 64 |
| Replay Buffer Descriptors | 15 | 32 |

Table 1 Summary of Differences between 89PES24N3 and 89PES24N3A

Functional Feature Differences

The functional feature differences are in five key areas:

- PCI Express Base Standard Revision — The 89PES24N3 is designed for compliance with revision 1.0a of the base specification while the 89PES24N3A is designed for compliance with revision 1.1.
- Lane Reversal — The feature set enhancements of the 89PES24N3A include support for automatic or static lane reversal. The added support for automatic lane reversal alleviates the need to take lane configurations into account at board layout time since lanes are configured during link training between link partners. The 89PES24N3 only supports static lane reversal.
- Peer-to-peer Security — The 89PES24N3A enables system designers to disable communication between the downstream ports of the device to enable implementation of system security measures. The 89PES24N3 does not support this feature.
- Legacy GPE Support for Hot Plug — The feature set of the 89PES24N3A includes support for a General Purpose Event for Hot Plug functionality. This enables systems to support legacy operation systems (e.g. Windows Server, 2003, etc.) that do not support PCI Express hot-plug.
- “Windows Logo” Requirements — The 89PES24N3A integrates the necessary functionality and features required for Windows Hardware Qualification Lab (WHQL) certification. Key feature enhancements over the 89PES24N3 include support for SSID and VSSID bits, ISA enable, and 16-bit VGA decode.
- Due to the additional features provided by the PESxxN3A device, the internal registers in this device are different from those in the PESxxN3 device. Properly written software or firmware which follows the enumeration and configuration procedures outlined by the PCIe specifications will not be impacted by this difference. Code that contains hard-coded values of various internal register locations or register contents will not be portable across the two devices, so some changes will be required in such code. Impact of this code can be minimized by writing portable code which will first check the revision ID of the IDT switch and then pick the appropriate set of hard-coded values to match the device.

Performance Feature Differences

The 89PES24N3A doubles the size of ingress buffers as compared to the 89PES24N3. This allows it to advertise twice the number of data and header credits for all flavors of transactions, which in turn allows a larger number of data packets to remain in flight across the datapath. Additionally, the 89PES24N3A incorporates an enhanced buffering architecture that combines the functions performed by the rate matching buffer with those of the replay buffer. This modification increases the effective size of the rate matching buffer function, compared to the 89PES24N3, and results in a high level of performance under all traffic patterns. With these enhancements, the 89PES24N3A is positioned to deliver the requisite performance for the most demanding server, storage, communications, and embedded applications including those which place a premium on performance at large payload sizes.

Additional Information on 89PES24N3 and 89PES24N3A

Additional product documentation and support collateral are available from the IDT web site (www.idt.com) and a portal within the company's myIDT secure information access domain. If you would like access to the secure information or are having any issues finding the required documentation or support for the 89PES24N3 or 89PES24N3A, please contact your local IDT sales representative or e-mail your issues and needs to ssdhelp@idt.com.