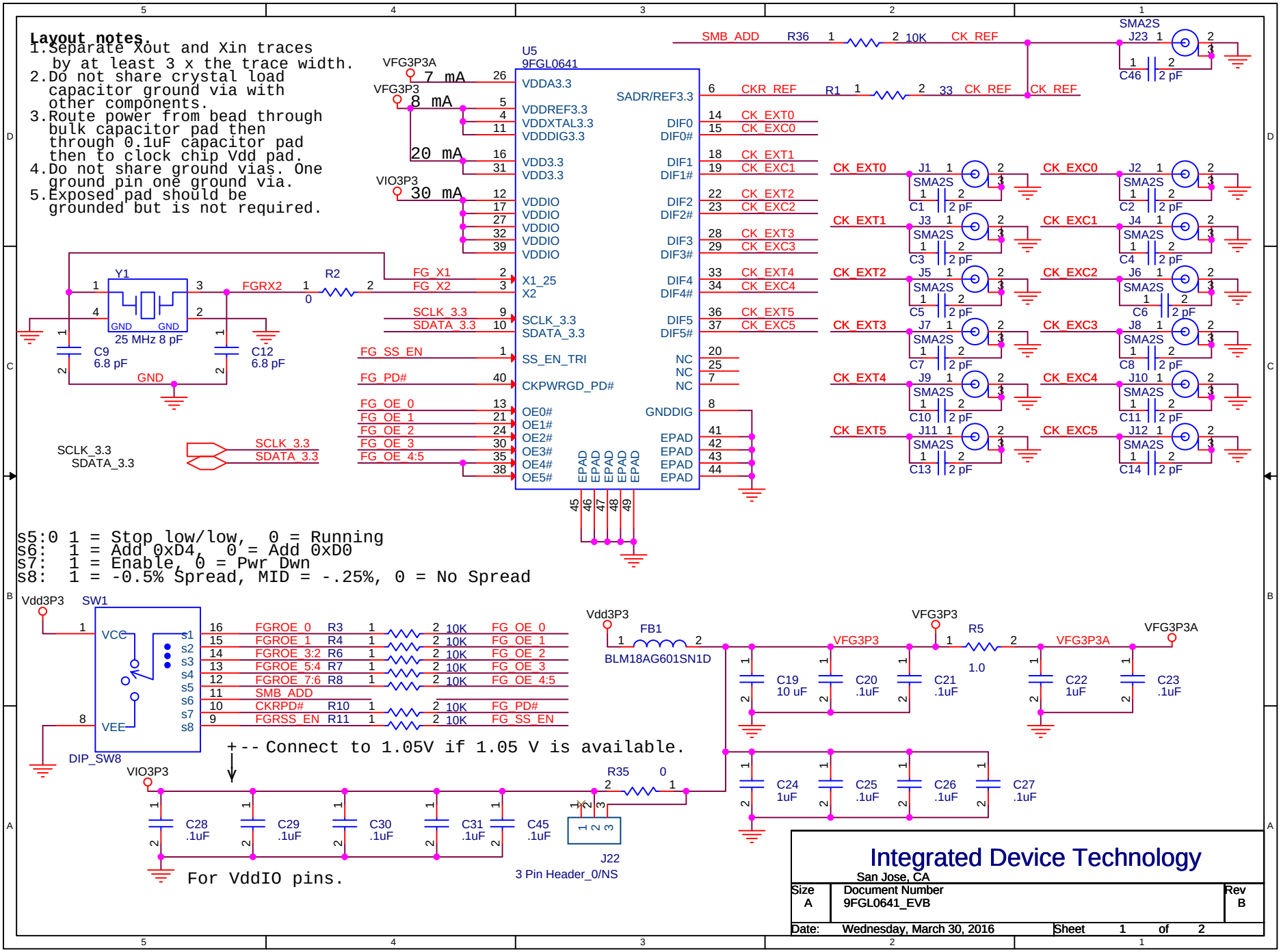
Layout notes.
1.Separate Xout and Xin traces by at least 3 x the trace width.
2.Do not share crystal load capacitor ground via with other components.
3.Route power from bead through bulk capacitor pad then through 0.1uF capacitor pad then to clock chip Vdd pad.
4.Do not share ground vias. One ground pin one ground via.
5.Exposed pad should be grounded but is not required.
U5
9FGL0641
VFG3P3A
7 mA
VFG3P3
8 mA
20 mA
VIO3P3
30 mA
VDDA3.3
VDDREF3.3
VDDXTAL3.3
VDDDIG3.3
VDD3.3
VDD3.3
VDDIO
VDDIO
VDDIO
VDDIO
VDDIO
SADR/REF3.3
DIF0
DIF0#
DIF1
DIF1#
DIF2
DIF2#
DIF3
DIF3#
DIF4
DIF4#
DIF5
DIF5#
NC
NC
NC
GNDDIG
EPAD
SMB_ADD
R36
10K
CK_REF
R1
33
CK_REF
CK_REF
SMA2S
J23
C46
2 pF
CK_EXT0
CK_EXC0
CK_EXT1
CK_EXC1
CK_EXT2
CK_EXC2
CK_EXT3
CK_EXC3
CK_EXT4
CK_EXC4
CK_EXT5
CK_EXC5
J1
J2
J3
J4
J5
J6
J7
J8
J9
J10
J11
J12
C1
C2
C3
C4
C5
C6
C7
C8
C10
C11
C13
C14
Y1
25 MHz 8 pF
GND
GND
GND
C9
6.8 pF
C12
6.8 pF
FGRX2
R2
0
FG_X1
FG_X2
X1_25
X2
SCLK_3.3
SDATA_3.3
SCLK_3.3
SDATA_3.3
FG_SS_EN
SS_EN_TRI
FG_PD#
CKPWRGD_PD#
FG_OE_0
FG_OE_1
FG_OE_2
FG_OE_3
FG_OE_4:5
OE0#
OE1#
OE2#
OE3#
OE4#
OE5#
SCLK_3.3
SDATA_3.3
s5:0 1 = Stop low/low, 0 = Running
s6: 1 = Add 0xD4, 0 = Add 0xD0
s7: 1 = Enable, 0 = Pwr Dwn
s8: 1 = -0.5% Spread, MID = -.25%, 0 = No Spread
Vdd3P3
SW1
DIP_SW8
VCC
VEE
s1
s2
s3
s4
s5
s6
s7
s8
FGROE_0
FGROE_1
FGROE_3:2
FGROE_5:4
FGROE_7:6
SMB_ADD
CKRPD#
FGRSS_EN
R3
R4
R6
R7
R8
R10
R11
FG_OE_0
FG_OE_1
FG_OE_2
FG_OE_3
FG_OE_4:5
FG_PD#
FG_SS_EN
+-- Connect to 1.05V if 1.05 V is available.
VIO3P3
C28 .1uF
C29 .1uF
C30 .1uF
C31 .1uF
C45 .1uF
For VddIO pins.
R35
0
J22
3 Pin Header_0/NS
Vdd3P3
FB1
BLM18AG601SN1D
C19 10 uF
C20 .1uF
C21 .1uF
VFG3P3
R5
1.0
VFG3P3A
C22 1uF
C23 .1uF
C24 1uF
C25 .1uF
C26 .1uF
C27 .1uF
Integrated Device Technology
San Jose, CA
Size A
Document Number 9FGL0641_EVB
Rev B
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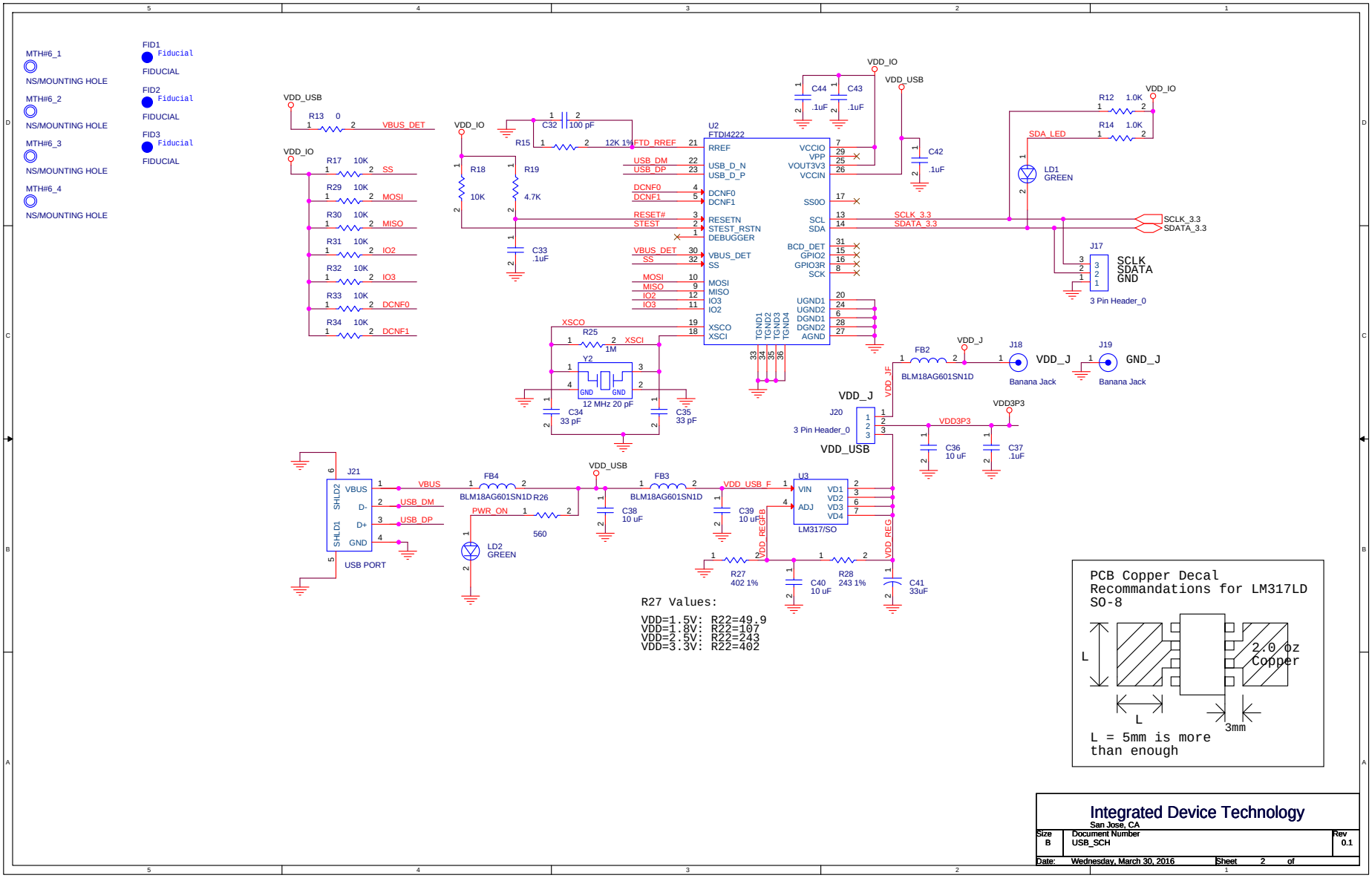

R27 Values:

VDD=1.5V: R22=49.9
VDD=1.8V: R22=107
VDD=2.5V: R22=243
VDD=3.3V: R22=402

PCB Copper Decal Recommandations for LM317LD SO-8

L = 5mm is more than enough

Integrated Device Technology San Jose, CA		
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