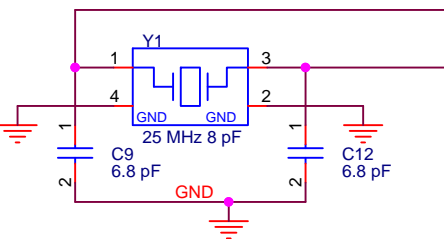


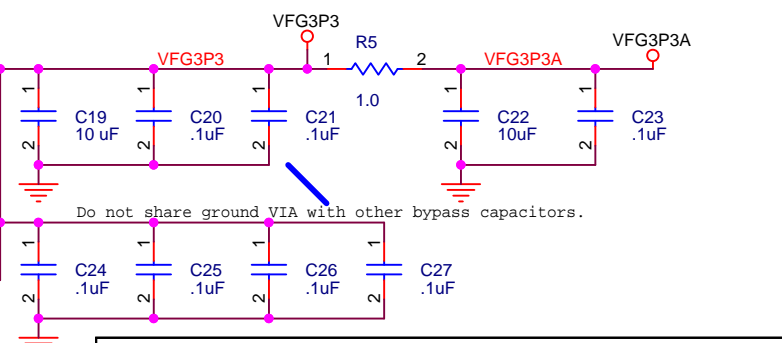
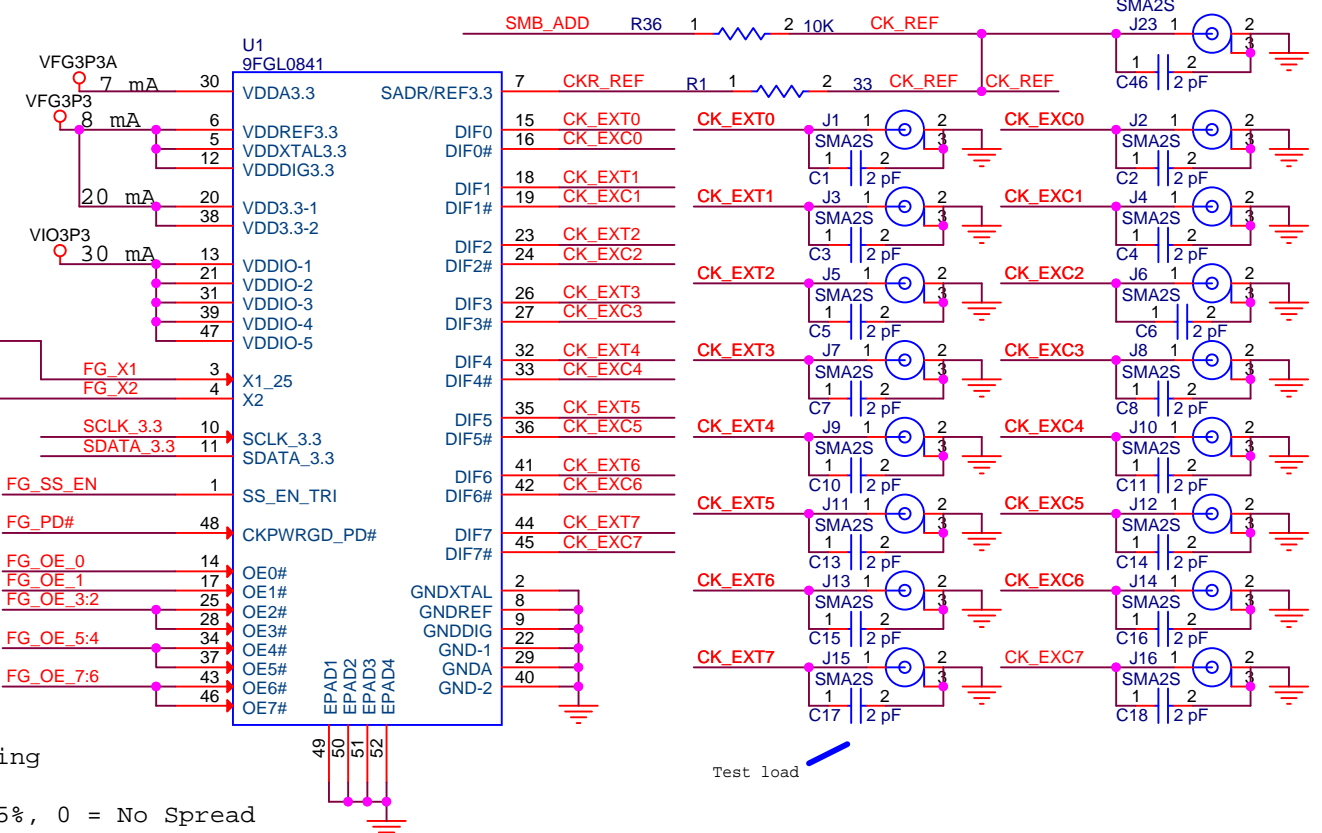
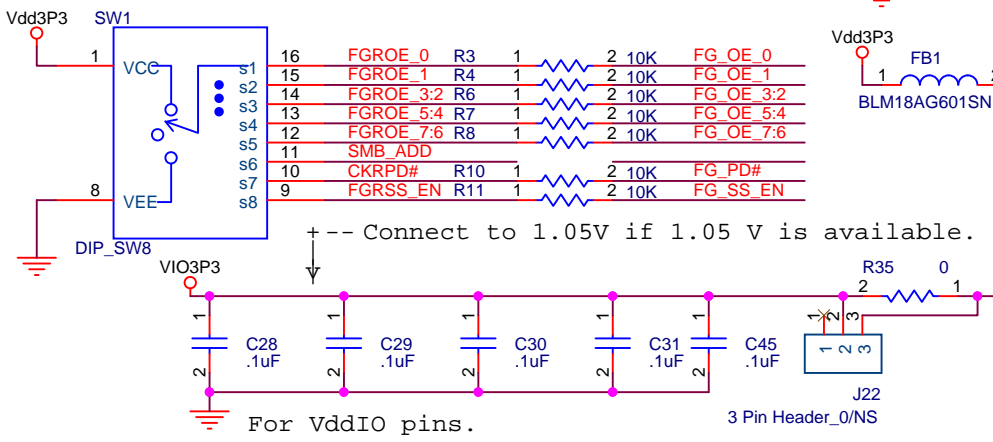
**Layout notes.**

1. Separate Xout and Xin traces by at least 3 x the trace width.
2. Do not share crystal load capacitor ground via with other components.
3. Route power from bead through bulk capacitor pad then through 0.1uF capacitor pad then to clock chip Vdd pad.
4. Do not share ground vias. One ground pin one ground via.
5. Exposed pad should be grounded but is not required.



SCLK\_3.3  
SDATA\_3.3

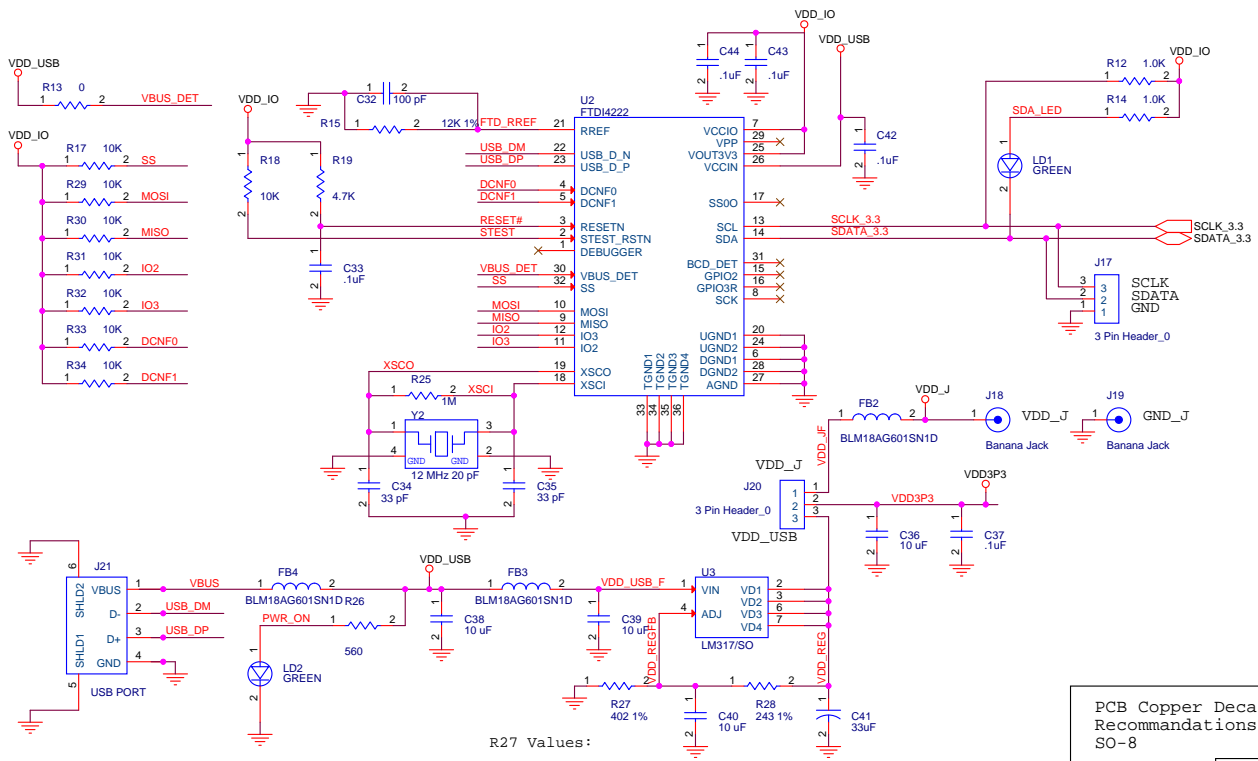
s5:0 1 = Stop low/low, 0 = Running  
s6: 1 = Add 0xD4, 0 = Add 0xD0  
s7: 1 = Enable, 0 = Pwr Dwn  
s8: 1 = -0.5% Spread, MID = -.25%, 0 = No Spread



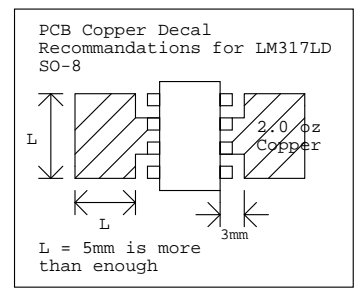
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- MTH#6\_1
  - NS/MOUNTING HOLE
  - MTH#6\_2
  - NS/MOUNTING HOLE
  - MTH#6\_3
  - NS/MOUNTING HOLE
  - MTH#6\_4
  - NS/MOUNTING HOLE
- FID1
  - FIDUCIAL
  - FID2
  - FIDUCIAL
  - FID3
  - FIDUCIAL



R27 Values:  
 VDD=1.5V: R22=49.9  
 VDD=1.8V: R22=107  
 VDD=2.5V: R22=243  
 VDD=3.3V: R22=402



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