



<- Leave Feed Back out floating.

CONFIGURATION SHOWN =
HIGH_BANDWIDTH, 133 MHz, SMBus ADDRESS=0xC2

VDD_IO May be 1.05 to 3.3 volts

85 Ohm Differential

HiBW BypM_LoBW# MODE
 Low PLL Lo BW
 Mid Bypass
 High PLL Hi BW

NOTE: PLL is OFF in Bypass Mode

Tri-Level Inputs		
SMB_A1	SMB_A0	Add
0	0	D8
0	M	DA
0	1	DE
M	0	C2
M	M	C4
M	1	C6
1	0	CA
1	M	CC
1	1	CE

NOTE: FERRITE BEADS =

Manufacture	Part Number	Z@100MHz	PkgSz	DC_res.	Current (Ma)
muRata	BLM21A601R	600	0805	0.30	600
TDK	MMZ2012S601A	600	0805	0.30	600
STEWART	HZ0805E601R	600	0805	0.30	600
AssocCmpTch	CBG0805-600-50	600	0805	0.30	600

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Revision history

Rev	Change	Title
0.1	First publication	9ZXL1950
0.3	Change R1 & R2 = 1.0 ohm.	

Size B	Document Number	Rev 0.3
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