

Description

The HXC44400 is a uni-directional Quad Channel PAM-4 CDR/Retimer. The chip can support both data rates of 56Gbps PAM4 and 28Gbps NRZ. The HXC44400 can be used in 200G QSFP56 and 400G QSFP-DD modules. The chip is optimized for Ethernet applications. It is in full compliance with OIF CEI-56G-VSR and CEI-56G-MR. The power consumption is typically 330mW per channel.

The HXC44400 has built-in programmable and adaptive equalization in both the receiver and transmitter paths to compensate for transmission line losses and inter-symbol interference.

Auto DC-offset calibration is implemented with auto phase calibration and the unique CDR/Retimer architecture enables independent receive and transmit CDR loop bandwidth optimization for increased Jitter Tolerance and reduced Jitter Transfer performance.

The device has a built-in, single 14GHz master VCO providing the oscillator output for each channel. In addition, the self-test functions such as a PRBS generator/checker, Jitter Tolerance, and Eye Open Monitor provide users with module-level diagnostics and function tests.

The HXC44400 also integrates an MCU for a programmable control, which could reduce BOM cost and enable better module design. The I2C interface is used to control the built-in MCU.

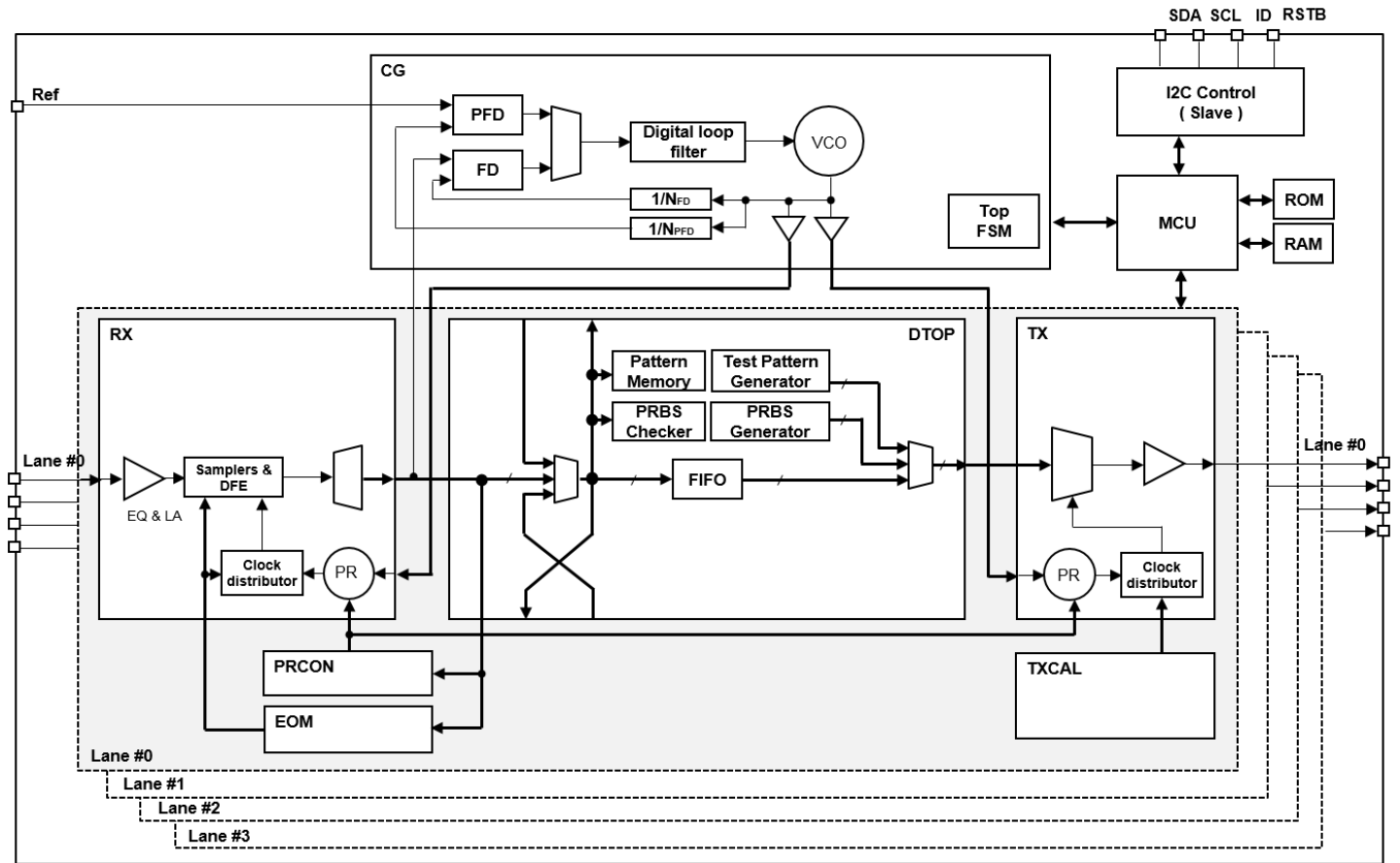
Typical Applications

- 200G QSFP56 Ethernet Transceivers
- 400G QSFP-DD Ethernet Transceivers
- Active optical Cables

Features

- Quad CDR/Retimer for transmitter or receiver
- Supports 56Gbps PAM4 and 28Gbps NRZ
- Output swing up to minimum 800mVpp with 7-bit resolution for output amplitude control
- Adaptive CTLE up to 10dB and DFE with 10 taps in receiver equalization
- Programmable 3-tap de-emphasis for a transmit
- Linearity compensation for output through a look-up table
- Independent, adaptive bandwidth control in RX CDR for optimum jitter tolerance
- Internal and automatic DC and phase offset calibrations
- Reference-less and Master channel-less operation
- On-chip testability: EOM, JTOL, PRBS generator/checker, user-defined pattern generator
- Embedded CPU with RAM/ROM and downloadable firmware
- I2C control interface (16-bit address and data)

Block Diagram



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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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