

## Description

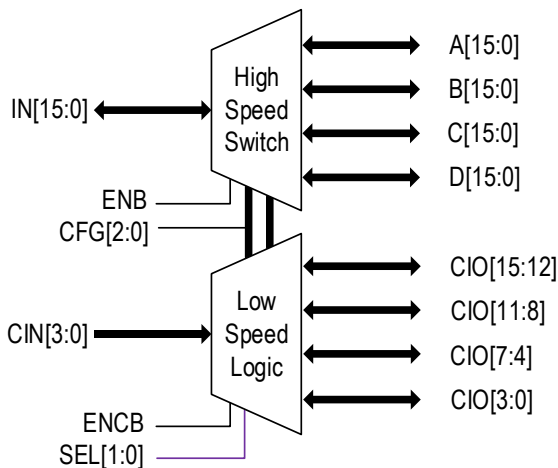
The MX0141KA0 is comprised of a high-speed 1:4 multiplexer (mux) path and a low-speed, multi-function control logic path.

The high-speed path consists of four passive switches that connect input port “IN” to four 16-bit output ports A, B, C, and D. The passive switches, which close selectively, form a bidirectional multiplexer.

The low-speed path consists of active multi-function IOs that can be configured in different modes. This path also can be configured as a unidirectional 1:4 mux with a 4-bit port width, 4:16 decoder, or 16-bit signals for port selection. The CIO pins can be used to drive Chip Enable pins of the NAND dies or the high-speed mux selector.

Both the high-speed and low-speed paths support SSTL\_12 and SSTL\_18 signaling.

**Figure 1. Block Diagram**



## Typical Applications

- SSD drive memory expansion or load reduction for both ONFI3/4 and TOGGLE NAND Flash system
- General purpose bus 1:4 multiplexer for high-speed, low-power product solutions

## Main Features

- 1:4 high bandwidth 16-bit bus multiplexer
- SSTL18 and SSTL12 signaling
- Supports ONFI 3.0, 4.0, 4.1 and Toggle NAND Flash
- 4 × 11 mm, 126-FCCSP package with 0.65/0.5mm ball pitch

## High-Speed MUX Features

- Bidirectional passive port switches
- Pull-up/Pull-down/Tristate/bus-hold for deselected ports
- Pin-to-pin output skew < 30ps (within a port)
- Pin-to-pin output skew < 10ps (Differential pairs)
- Propagation delay < 150ps
- Insertion loss < 1dB at 800MHz
- Bus holding, weak pull-down, or weak pull-up for deselected ports in different configurations via the CFG pins

## Low-Speed MUX/Control Logic Features

- 4-bit IN, 16-bit input/output logic targeted for Chip Enables or port selections
- Multiplexing or decoding
- Unidirectional, active multiplexing
- Multiple function selected via the CFG pins

**Table 1. High-Speed Path Characteristics**

Feature	High-Speed Path
Port speed	Up to 1600MT/s
Port size	16-bit
Direction	Bidirectional, IN ↔ A, B, C, or D
Control pins	SEL[1:0], ENB, ENCB, CIN[3:0], CIO[15:0]
Signaling through port	SSTL_12, SSTL_18

## Ordering Information

Orderable Part Number	Description and Package	MSL Rating	Shipping Packaging	Temperature
MX0141KA0AVW	4.0 × 11 mm, 126-FCCSP (AVW126)	3	Tray	0° to +85°C
MX0141KA0AVW8	4.0 × 11 mm, 126-FCCSP (AVW126)	3	Tape and Reel	0° to +85°C



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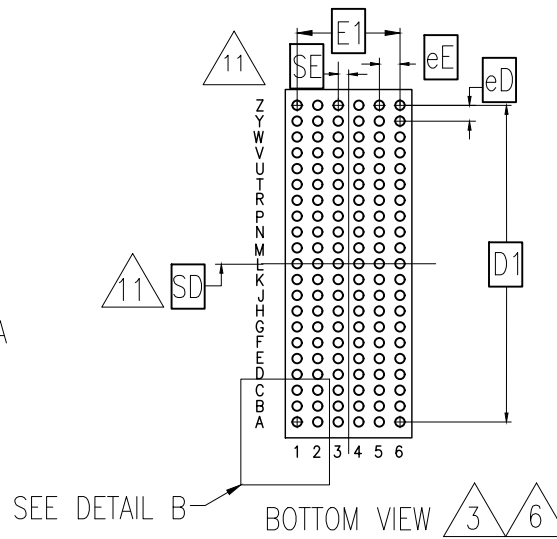
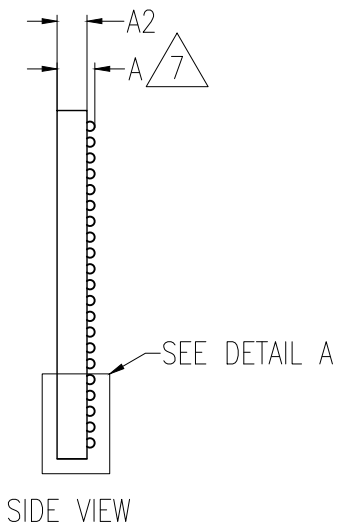
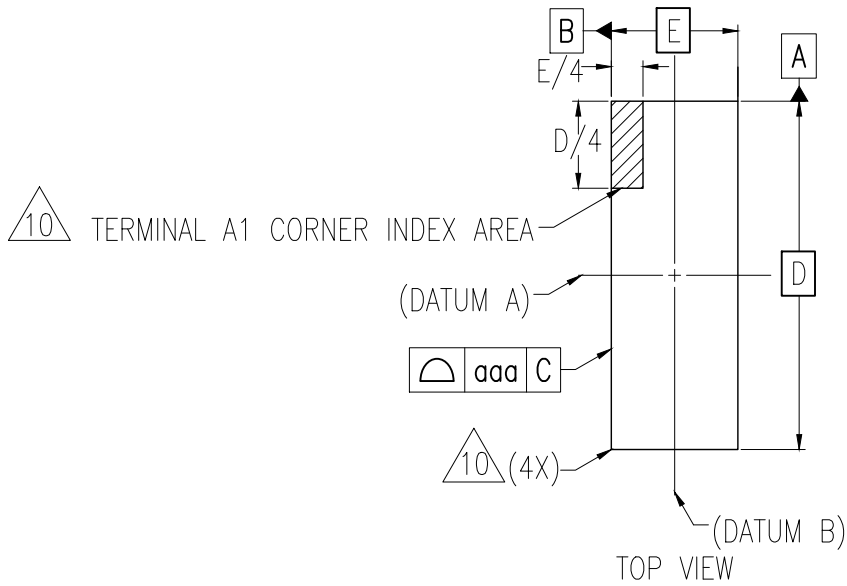
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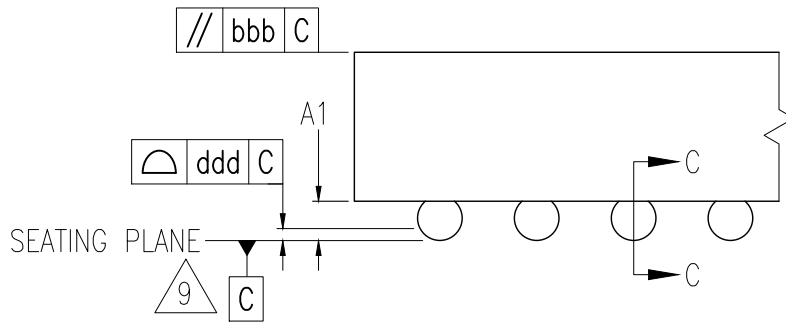
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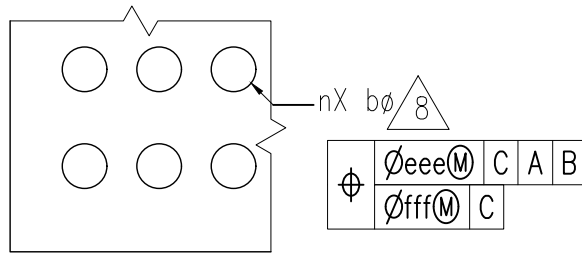
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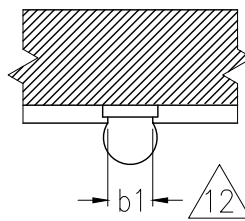


DETAIL A  
(ROTATED 90° CW)



DETAIL B

TYPE: SMD  
(SOLDER MASK DEFINED)



SECTION C-C

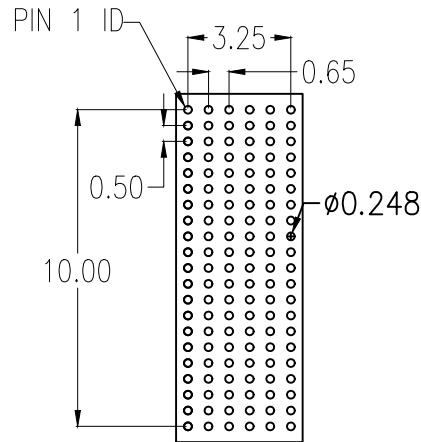
TABLE 1				
COMMON DIMENSIONS				
SYMBOL	V:VERY THIN PROFILE			NOTES
	MIN	NOM	MAX	
A	0.80	0.90	1.00	7
A1	0.15	—	—	9
A2	—	—	0.85	
b	0.27	0.32	0.37	
b1	0.20	—	—	13
eD	0.50 BSC			4
eE	0.65 BSC			4
NOTES	1, 2			

TABLE 2		
RECTANGULAR VARIATIONS		
VARIATION ►	AA	NOTES
SYMBOL ▼		
D BSC	11.00	2
E BSC	4.00	2
D1 BSC	10.00	2
E1 BSC	3.25	2
MD	21	
ME	6	
SD BSC	0.00	2
SE BSC	0.325	2
n	0	12
N	126	5
FOOTPRINT	1	12
NOTES	1	

TABLE 3	
TOLERANCE OF FORM AND POSITION	
SYMBOL	VALUE
aaa	0.15
bbb	0.20
ddd	0.08
eee	0.15
fff	0.05
NOTES	1, 2

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. SOLDER BALL POSITION DESIGNATOR PER JEP95, SECTION 3, SPP-020.
4. 'eD' AND 'eE' REPRESENT THE SOLDER BALL GRID PITCH CORRESPONDING TO THE D AND E DIRECTIONS RESPECTIVELY.
5. N REPRESENTS THE MAXIMUM NUMBER OF SOLDER BALLS FOR MATRIX SIZES MD, ME.
6. A FULLY POPULATED 14 X 19 MATRIX SIZE IS SHOWN FOR ILLUSTRATION ONLY.
7. DIMENSION "A" INCLUDES STANDOFF HEIGHT "A1", PACKAGE BODY THICKNESS AND LID HEIGHT, BUT DOES NOT INCLUDE ATTACHED FEATURES, e.g. EXTERNAL HEAT SINK. AN INTEGRAL HEAT SLUG IS NOT CONSIDERED AN ATTACHED FEATURE.
8. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM C.
9. PRIMARY DATUM C (SEATING PLANE) IS DEFINED BY THE PLANE ESTABLISHED BY THE CONTACT POINTS OF THREE OR MORE SOLDER BALLS THAT SUPPORT THE DEVICE WHEN IT IS PLACED ON TOP OF A PLANAR SURFACE.
10. THE CORNER A1 MUST BE IDENTIFIED ON BOTH THE BOTTOM AND TOP SIDES OF THE PACKAGE, THE IDENTIFICATION FEATURE CAN BE MADE USING INK OR METALIZED MARKINGS, IDENTATIONS, OR OTHER FEATURES. THE EXACT SHAPE OF EACH CORNER IS OPTIONAL.
11. DIMENSIONS 'SD' AND 'SE' ARE MEASURED WITH RESPECT TO DATUM A AND DATUM B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW 'SD' OR 'SE' = 0 WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, 'SD' = eD/2 AND 'SE' = eE/2.
12. SOLDERABLE SURFACE MAY BE DEFINED BY AN OPENING IN THE SOLDER RESIST LAYER (TYPE 1) OR BY THE SIZE OF A METALIZED PAD (TYPE 2). IT MAY BE ELLIPTICAL PROVIDED THE RATIO OF MAJOR TO MINOR AXES IS NO GREATER THAN 2/1 AND THE SURFACE AREA IS NO LESS THAN THE MINIMUM FOR A CIRCULAR PAD. FOR TYPE 2 DESIGNS, EXPOSED COPPER TRACES ARE PERMITTED OUTSIDE THE b1 PAD AREA.



RECOMMENDED LAND PATTERN DIMENSION  
(TOP VIEW)

NOTES:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
Feb 12, 2019	Rev 00	Initial release