WIRELESS POWER LDO TECHNICAL NOTE

WIRELESS POWER DIVISION NOV2019

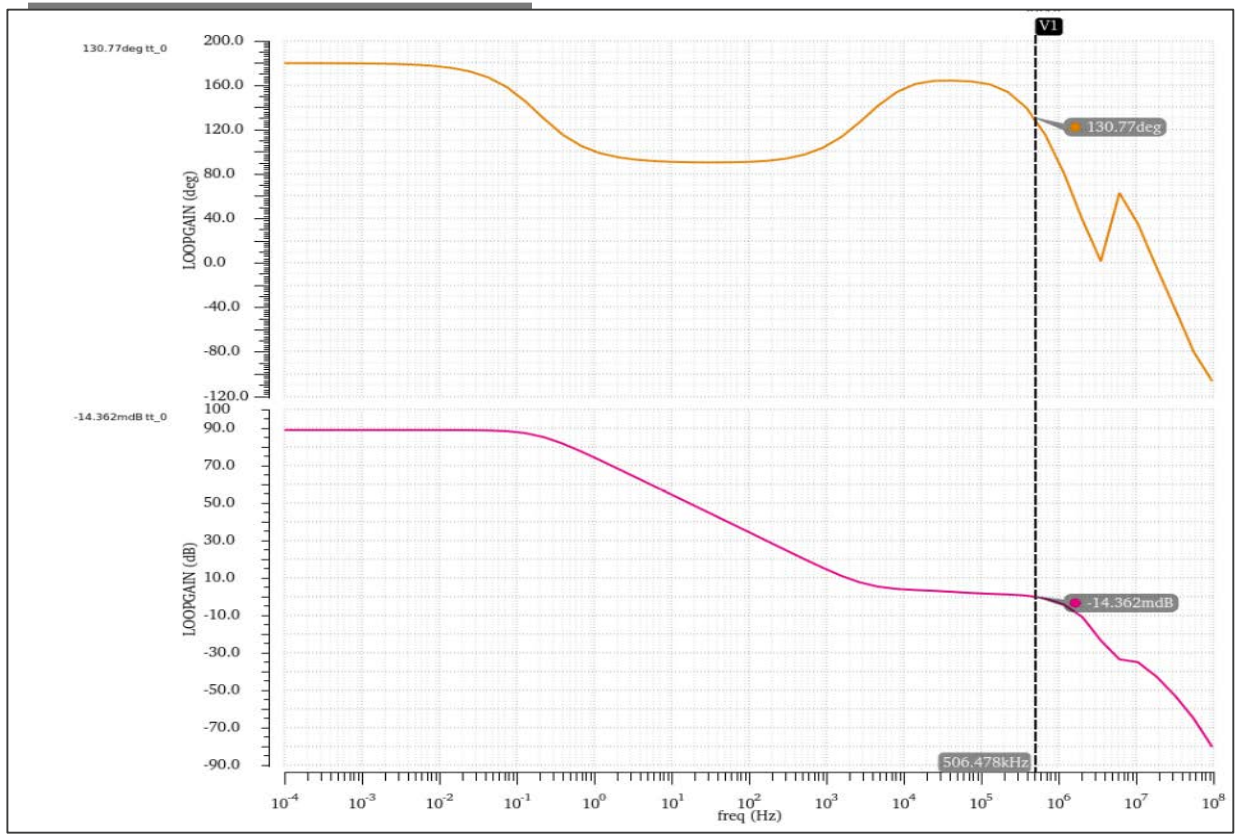
INTRODUCTION

The application note explains the behavior of the LDO stage, usually associated with the output of a wireless power receiver IC, when used with a downstream capacitor divider (CD) battery charger. The simulation results provide an explanation of the effect of CD operating frequency and output capacitance on the voltage droop from the voltage regulator.

LDO TOPOLOGY

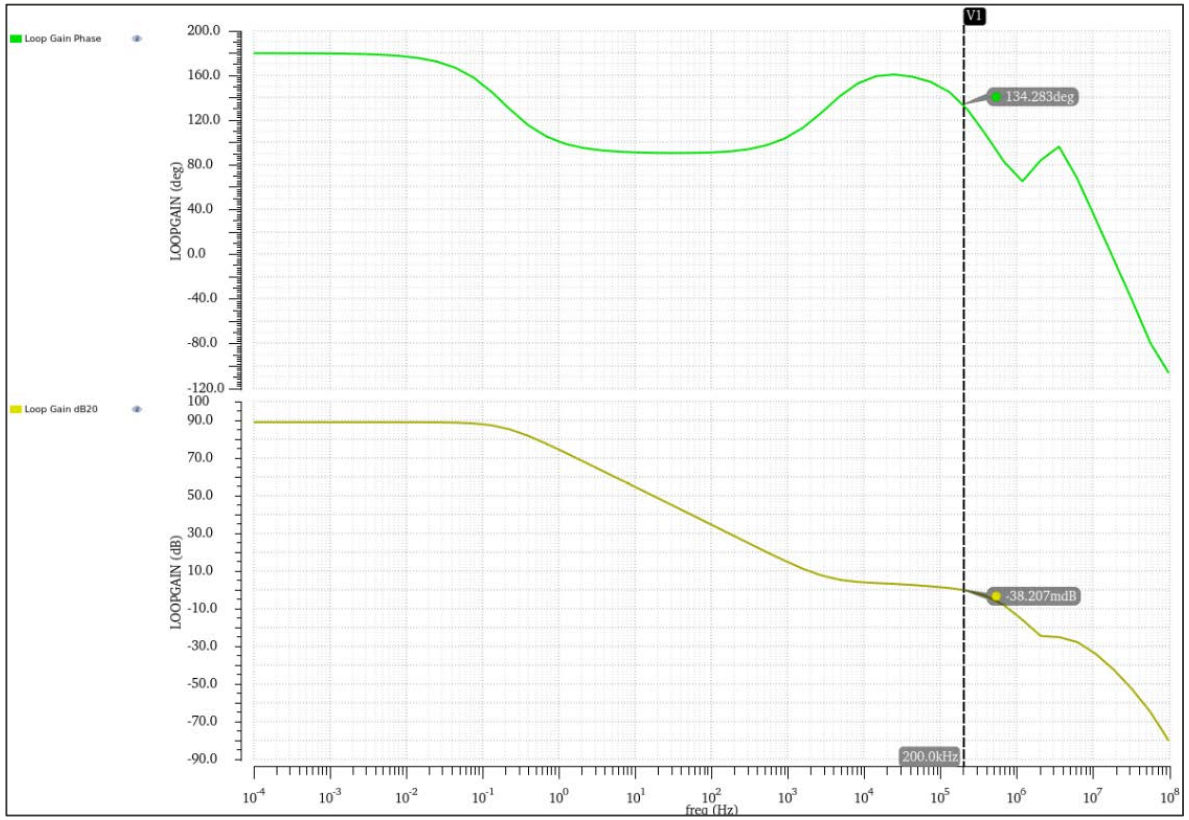
- The wireless power receiver has a Low Drop-Out (LDO) circuit to regulate the rectifier voltage to downstream devices.
- The LDO has multiple loops with internal compensation. The voltage loop includes a feedforward capacitor to extend the bandwidth and ensures a fast transient response.
- Multiple parameters will effect the unit gain bandwidth of the LDO
  - More output capacitors will reduce unit gain bandwidth
  - Light load current also reduce the unit gain bandwidth
  - Output voltage level change the V_{OUT} cap effective capacitance.
  - Higher voltage settings will further reduce the effective V_{OUT} capacitance which increases the bandwidth.

LOOP PLOT WITH V_{OUT}=18.8V, V_{IN}=18.9V I_{OUT}=1.6A



- Output capacitance 2x10uF. Effective Capacitance = 3uF.

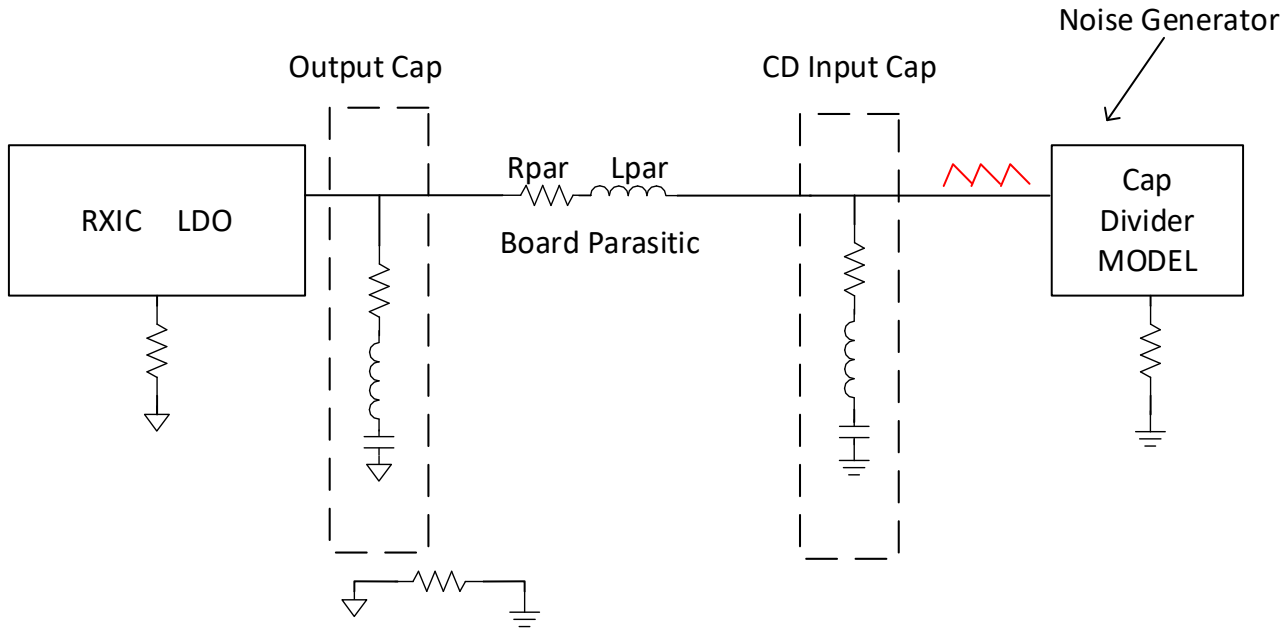
LOOP PLOT WITH V_{OUT}=18.8V, V_{IN}=18.9V I_{OUT}=1.6A



- Output capacitance 2x22uF. Effective Capacitance = 6uF.
- Bandwidth is reduced to 200kHz and there is almost 20dB attenuation at 1MHz frequency.

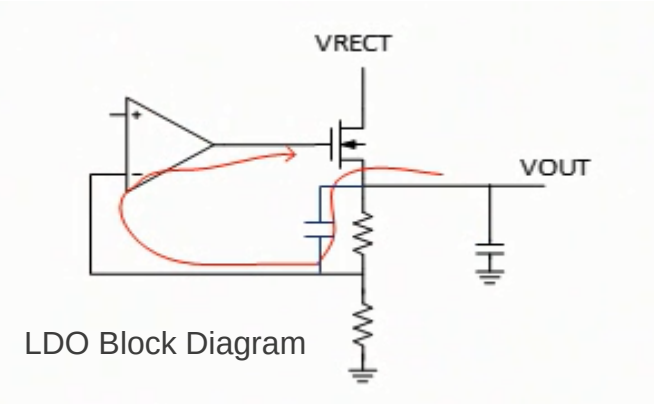
WITH CAP DIVIDER

- When the wireless power receiver is working together with a Cap Divider, depending on the load current profile, noise will be introduced in the voltage loop of the regulator.
- Below diagram is used to simulate this condition.
- Single phase 2:1 Cap Divider behavior model is used at the output of the regulator.

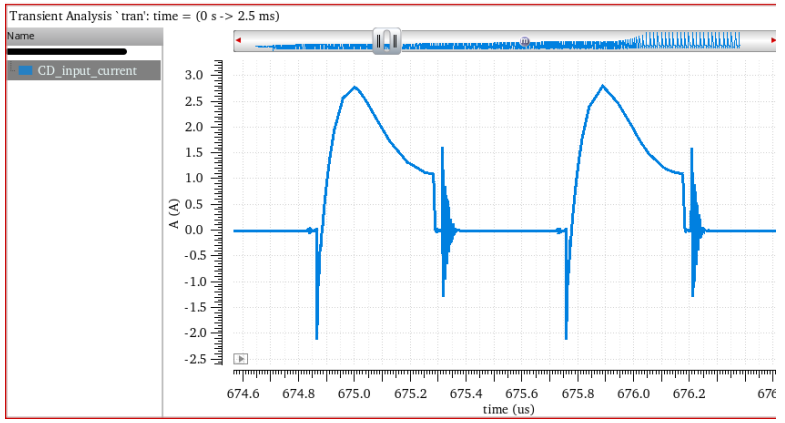


EXPLANATION OF THE NOISE EFFECT ON REGULATION

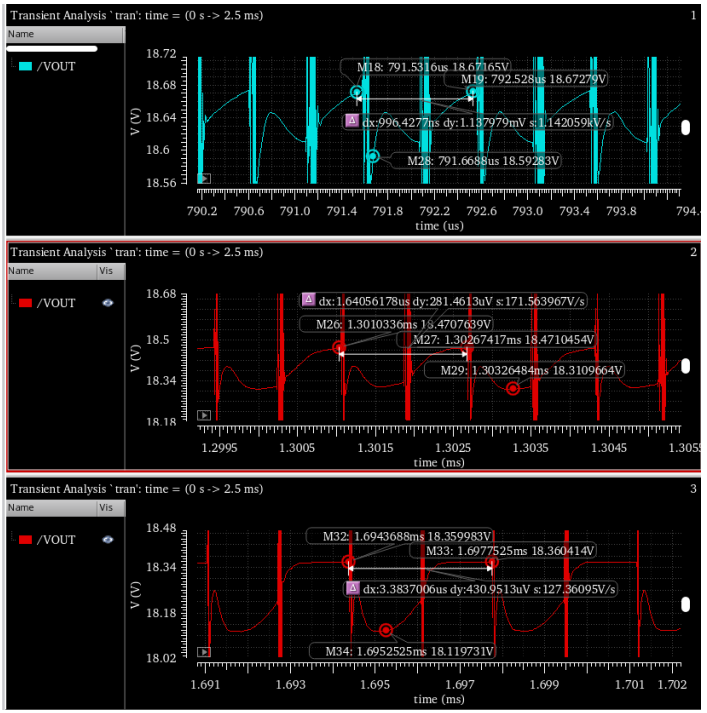
- LDO block diagram with feed forward cap showing on the right.
- For a single phase capacitor divider (CD) input current is presented to LDO output as an AC signal (see picture on the bottom right). For example:
  - CD load = 1.6A
  - LDO load = AC current between 0A and 2.5A instead of a DC current of 0.8A
- With low effective capacitance at the output, LDO will continuously see large current transients that cause some voltage spikes at VOUT.
- Similar to a DCDC converter, If the CD frequency is close or within the range of the wireless power receiver regulator UGB, the noise will be amplified and the regulation point will be affected. Control loop bandwidth should be much lower than switching frequency for the part to operate properly.
- Current ripple and CD operating frequency ultimately both induce droop in LDO regulation.



LDO Block Diagram



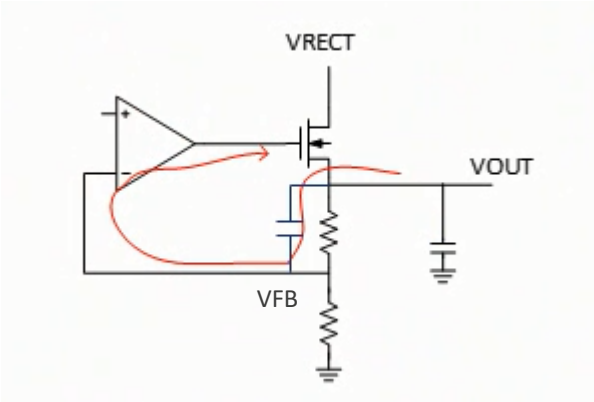
VOUT DROOP VS CD FREQUENCY



CD Frequency = 1MHz

CD Frequency = 600KHz

CD Frequency = 300KHz



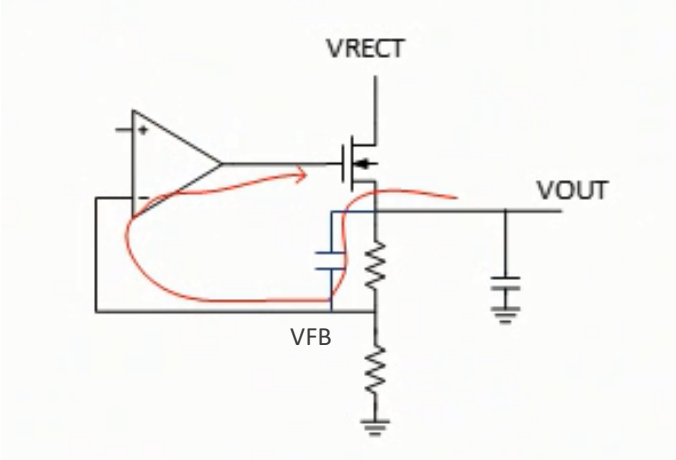
2x 25V 22uF cap on vout

Frequency	Output Voltage	Delta
300KHz	18.23V	-400mV
400KHz	18.25V	-380mV
500KHz	18.32V	-310mV
600KHz	18.37V	-260mV
700KHz	18.42V	-210mV
800KHz	18.51V	-120mV
900KHz	18.58V	-50mV
1MHz-1.4MHz	18.63V	0

For the table on the right: V_{RECT} = 18.73V, V_{OUT} is set to 18.63V

Delta represents output deviation from the set point (droop)

V_{FB} NODE WAVEFORMS C_{OUT}=2X22uF C_{EFF}=4.8uF



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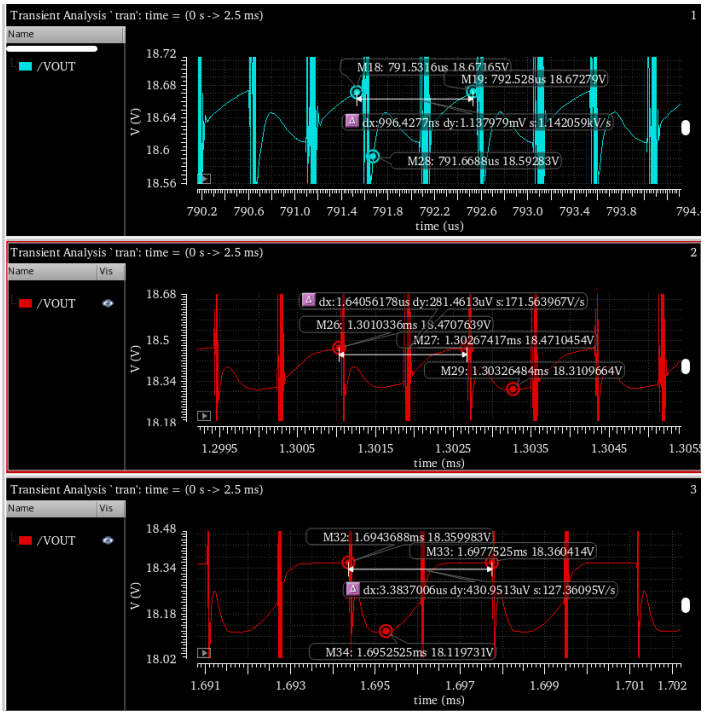
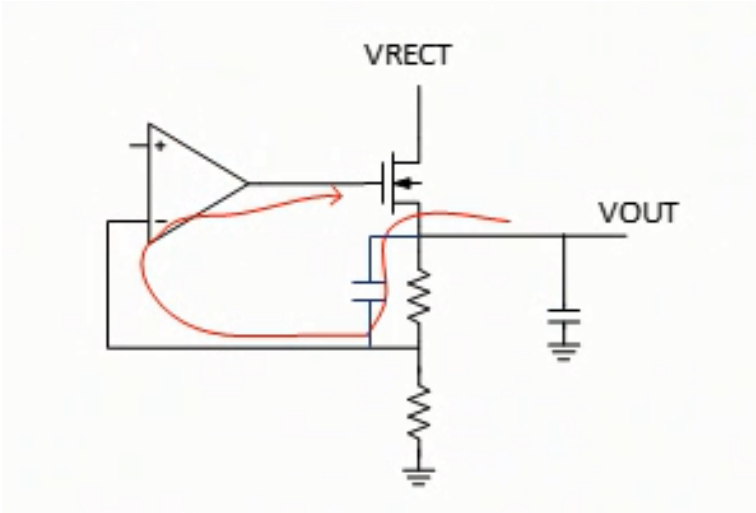


- At lower frequency the voltage ripple is higher (see right picture).
- If Cap Divider switching frequency is within the wireless power receiver regulator bandwidth the noise due to the current ripple will be amplified.
- Majority of noise from the output is transferred to the feed-back node via feed forward capacitor without any attenuation. Loop gain bandwidth is high such that it cannot filter out the ripple.

DESIGN RECOMMENDATIONS FOR CUSTOMERS

- VOUT droop is caused by CD frequency noise propagating into LDO control loop. The amplifier inside the LDO is a high gain and high bandwidth amplifier that can respond to low CD switching frequency.



- The impact of the CD switching noise is reduced by increasing the switching frequency and increasing COUT which reduces the amplitude of the current ripple and increases attenuation due to the bandwidth.
  - Baseline droop performance improves from 280mV (@600kHz) to 40mV (@900kHz CD switching) with 2x22uF capacitance at the output (see table in slide 8)

RATIONALE FOR DESIGN RECOMMENDATIONS

- From signal point of view, V_{OUT} cap works as a low pass filter.
  - The output capacitor sets the output pole. Increasing the V_{OUT} capacitor will reduce the unity gain bandwidth. For the same CD switching frequency, increasing V_{OUT} capacitance will provide more attenuation of CD noise.
  - Additionally, with increasing V_{OUT} capacitance, large signal current ripple will be filtered better.
- When CD operates at higher frequency the droop decreases for the following reasons:
  - CD noise happens outside of the loop bandwidth
  - We see higher attenuation of the injected noise at the 1MHz frequency compared with the 600KHz. It is equivalent to increasing the V_{OUT} capacitance.

FAQS

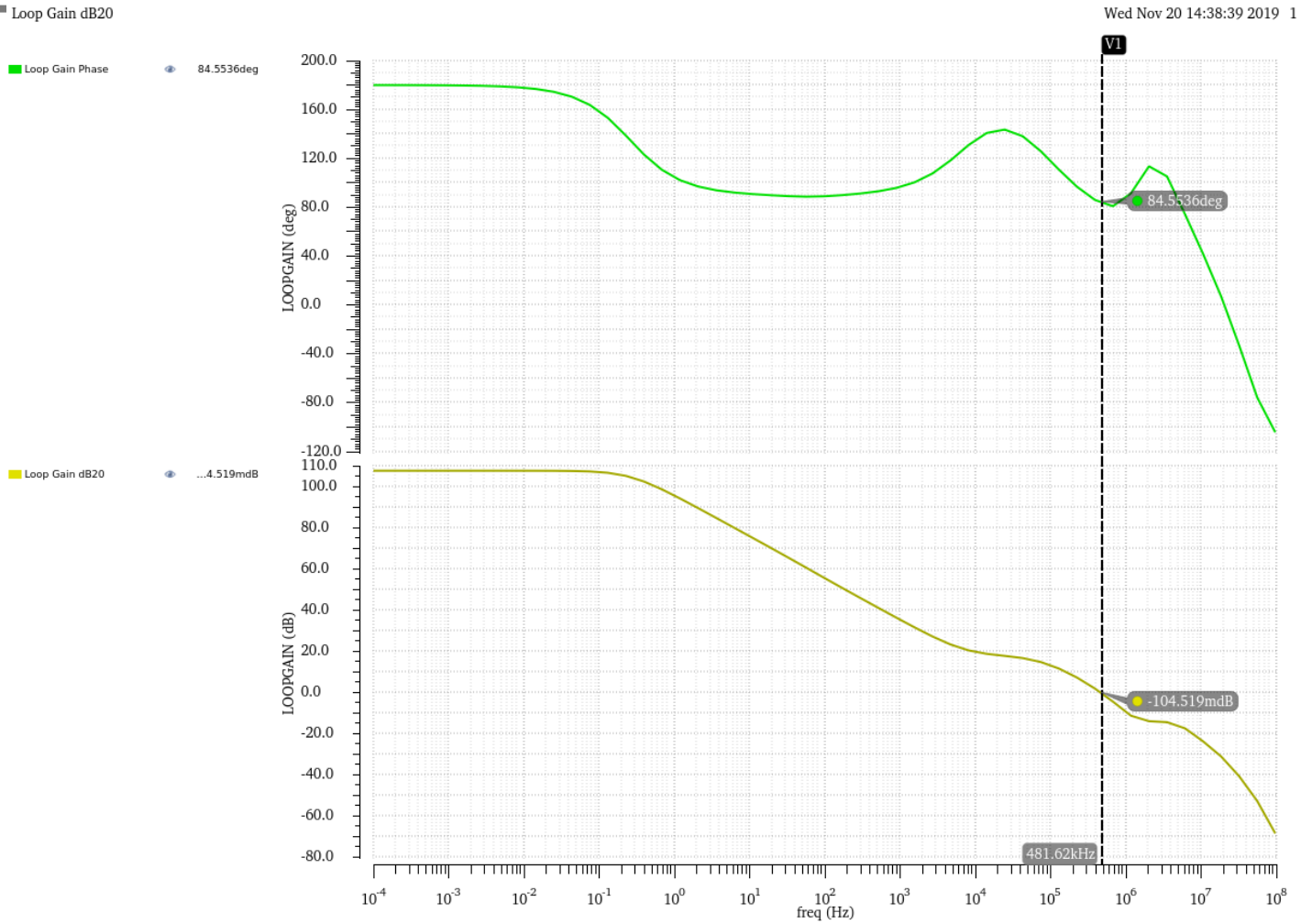
- **What is the frequency range of cap divider operation that impacts the regulator?**
  - Please see slide 8, if cap divider operating frequency is above 1MHz impact on the regulator output voltage is minimized
- **Is the MLDO output voltage/current peak to peak value that impacts the MLDO? If yes, what would be the range?**
  - Cap divider input current ripple which translated to the output of the regulator as voltage noise as well as the operation frequency can cause output droop if the frequency is close to or in the regulator's bandwidth. In slide 7 we can see the current profile and we observed in simulation that if the current peak is above 2.5A the output voltage starts to be impacted

FAQS

- **Is this droop due to di/dt of Iout ripple? Or dv/dt of the Vout ripple? If yes, then what would be the range that di/dt or dv/dt that impact the MLDO**
    - The combination of high current load level with current ripple/voltage noise and the CD switching frequency close to regulator's unity gain bandwidth can impact the output voltage.
- **Is there any special impact from cap divider, from layout point of view?**
    - There should be no major impact on CD since it is switching and it operates open loop without sensitive node like feedback point and reference node, but the board layout could affect the wireless power receiver regulator output.
- **What would be the min effective MLDO output capacitance value?**
    - Depends on the frequency. For 1MHz, the board V_{OUT} capacitance should be 4.8uF(effective after DC voltage de-rating) or higher.
    - At lower frequencies more bypass capacitance is needed as to reduce the regulator bandwidth below the switching frequency.

Backup – additional loop stability conditions

LOOP PLOT WITH V_{OUT}=9V, V_{IN}=9.1V I_{OUT}=1.2A C_{OUT}=6*22UF+2*10UF



LOOP PLOT WITH V_{OUT}=9V, V_{IN}=9.1V I_{OUT}=0.1A C_{OUT}=6*22UF+2*10UF